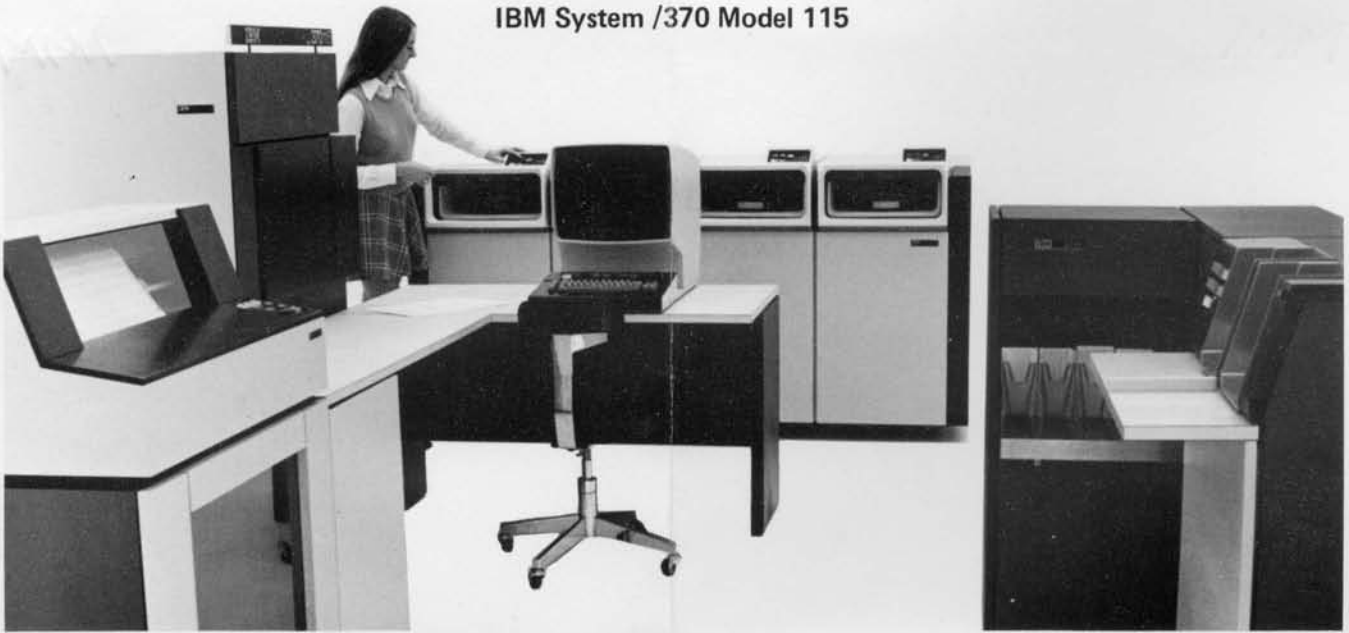


1111

370
115

IBM System /370 Model 115



Description

The Model 115 is a small scale, compatible member of the System /370 product line. It offers function and performance, that was previously unavailable to customers who at present have a System /360 Model 20, 22 or 25.

The Model 115 provides a logical growth into a /370 Model 125 especially for those customers who want to grow within the same machine concept. Both systems are functionally identical although the design details are different.

Depending on the instruction mix, the program structure and size, the instruction execution rate of the Model 115 is approximately 1.5 to 3 times faster than that of a System /360 Model 25 and 1 to 1.5 times faster than that of a System /360 Model 22.

The Model 115 consists of several independent sub-processors communicating with the Main Storage (MS) through the Main Storage Controller (MSC).

These subprocessors are:

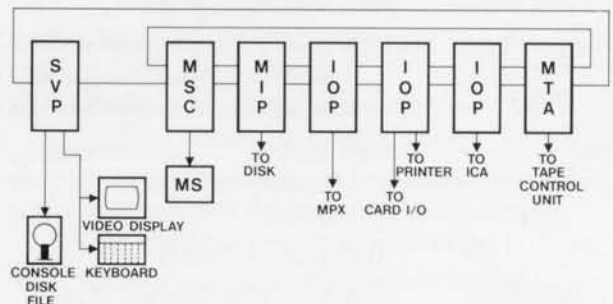
- **SERVICE PROCESSOR (SVP)**
performs microprogram loading into the other subprocessors' control storages, provides the link between operator and system, logs error conditions for later analysis and provides a service tool for system diagnostic.

- **MACHINE INSTRUCTION PROCESSOR (MIP)**
analyzes and executes machine language instructions.
- **INPUT / OUTPUT PROCESSOR (IOP)**
executes I/O commands and supervises data transfer between I/O devices and MSC.

The Magnetic Tape Adapter (MTA) connects the 3411/10 magnetic tape unit and control to the system.

The SVP, MIP, and IOPs are controlled by microprogram and have their own control storages, local storages, workregisters and arithmetic / logic units.

PRINCIPLE DATA FLOW



Note: The MPX and its IOP is mutually exclusive with native Card I/O, however, a RPQ is available to remove the exclusivity.

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The following devices can be attached natively:

Card I/O (MFCM)	2560	Mod. A1	500/91/91 cpm
		Mod. A2	310/65/65 cpm
Card I/O (MFCU)	5425	Mod. A1	250/60/60 cpm
		Mod. A2	500/120/120 cpm
Printer	3203	Mod. 1	600 lpm
		Mod. 2	1200 lpm
		Mod. 3	300 lpm
Console Printer	5213	Mod. 1	85 cps
Magnetic Tape	3411/10	Mod. 1	max. 4 drives/20 KB
		Mod. 2	max. 6 drives/40 KB
		Mod. 3	max. 6 drives/80 KB
Disk	3340	Mod.A2	2 spindles (basic)
		Mod.B1	1 spindle
		Mod.B2	2 spindles
Maximum is 4 spindles			
Disk Packs	3348	Mod. 035	approx. 35 MB
		Mod. 070	approx. 70 MB

The following attachment capabilities are also available:

ICA	up to 4 BSC lines and 8 Start/Stop lines
MPX	up to 32 subchannels
Data Rate:	Burst Mode 29 KB
	Byte Mode 19 KB

Compatibility

The Model 115 offers an entry into the System /370 family. It shares the full System /370 instruction set. System /360 Model 20 compatibility is available as a feature.

Technology

- Monolithic Systems Technology Type 1 (MST-1) and MST-1 dense are used for all logic circuitry.
- The Main Storage and all writeable control storages use MOSFET (metal oxide semiconductor field effect transistor) type technology.
- All local storages are built from HDB (high density buffer) modules.
- The system power is provided mainly by high frequency power supplies called TSRs (transistor switching regulators).

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Console System

The console system of the Model 115 replaces the conventional hardware console consisting of typewriter, rotary switches and many indicator lamps. It is controlled by the SVP microprogram and consists of:

- VIDEO DISPLAY UNIT
which can display 16 lines per 56 characters each on a cathode ray tube (CRT).
- KEYBOARD
Most of the keys are capacitive switching elements with a minimum of moving mechanical parts.
- Important INDICATOR LAMPS and SWITCHES are available for special functions.
- CONSOLE DISK FILE
This device
 - contains the micro control programs for the control storages of SVP, MIP, and the IOPs on a flexible diskette, and test, analysis and display programs as well.
 - stores log information on the diskette.

Service Processor (SVP)

The SVP is a microprogram controlled general purpose processor. The SVP serves as an interface between the operator (via keyboard, video display unit and optional console printer), the console disk file and the remaining system. A dedicated bus system allows the SVP to access any of the other subprocessors

- to load their control storages with the proper microprograms stored on the console disk file.
- to display messages on the CRT (Cathode Ray Tube) for operator communication and accept responses via the keyboard.
- to collect log data from the system to be stored on the console disk file for later reference by the customer engineer.
- to be used as a service tool to apply microdiagnostic programs to the remaining system hardware.

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Machine Instruction Processor (MIP)

The MIP analyzes and executes machine language instructions and provides the hardware - software interface for interrupts. Two different microprograms are contained in the IOP control storage of the MIP since it operates the direct disk attachment (DDA) and the instruction processing. The MIP consists mainly of an IOP with additional hardware logic and extended control storage. The most obvious difference in the logic design between the model 115 and Model 125 is the implementation of the MIP instead of the IPU.

Main Storage Controller (MSC)

The MSC is a hardware device without microprogram. It controls the main storage access of the other sub-processors. Each subprocessor requesting main storage service must specify this action in detail. The MSC selects the subprocessor to be serviced next according to a fixed priority scheme and performs and times the data transfer.

Input / Output Processor (IOP)

The IOP is controlled by microprogram. It provides the interface between the system and the I/O device. All IOPs have the same hardware design. However, each IOP is loaded with a different microprogram tailored to the specific task of the I/O devices attached. Specialized hardware logic (front ends) connect the I/O devices to the IOPs to accommodate the different I/O requirements with the uniform IOP design.

Storages

The Main Storage as well as control storages use MOSFET monolithic storage modules.

Main Storage is a non-destructive-readout storage with a cycle time of 480 nanoseconds per halfword access. It is available in 65 536 and 98 304 byte sizes. It is equipped with error check and correction circuits (ECC) to detect and correct single bit errors and detect multiple bit errors.

Control Storages are equipped with "Invert Bit" circuits, which correct single bit errors.



Maintainability

The following maintenance features are available for the Model 115:

■ SERVICE PROCESSOR (SVP)

The SVP has independent access to the other sub-processors via its dedicated bus system. Therefore it is an excellent service tool to test and check the hardware functions of the other subprocessors. The SVP itself is extensively hardware checked. So a well functioning processor is used to identify and locate troubles in the rest of the system.

- The SVP ensures check of control storages while loading the microprogram of the other subprocessors and monitors the other system components for errors arising during normal system operations. In case of error, the SVP gathers all necessary log data and stores them on the flexible diskette of the console disk file for later analysis.

- Upon CE request a log analysis program will analyse the stored data and present error reports to the CE via the video display.
- The SVP with keyboard and video display serves as CE panel by providing CE functions such as display and alter.
- It permits the CE to invoke and run diagnostic programs either with the system in stop mode or with In-Line Test programs (ILTs) concurrent with customer operations.

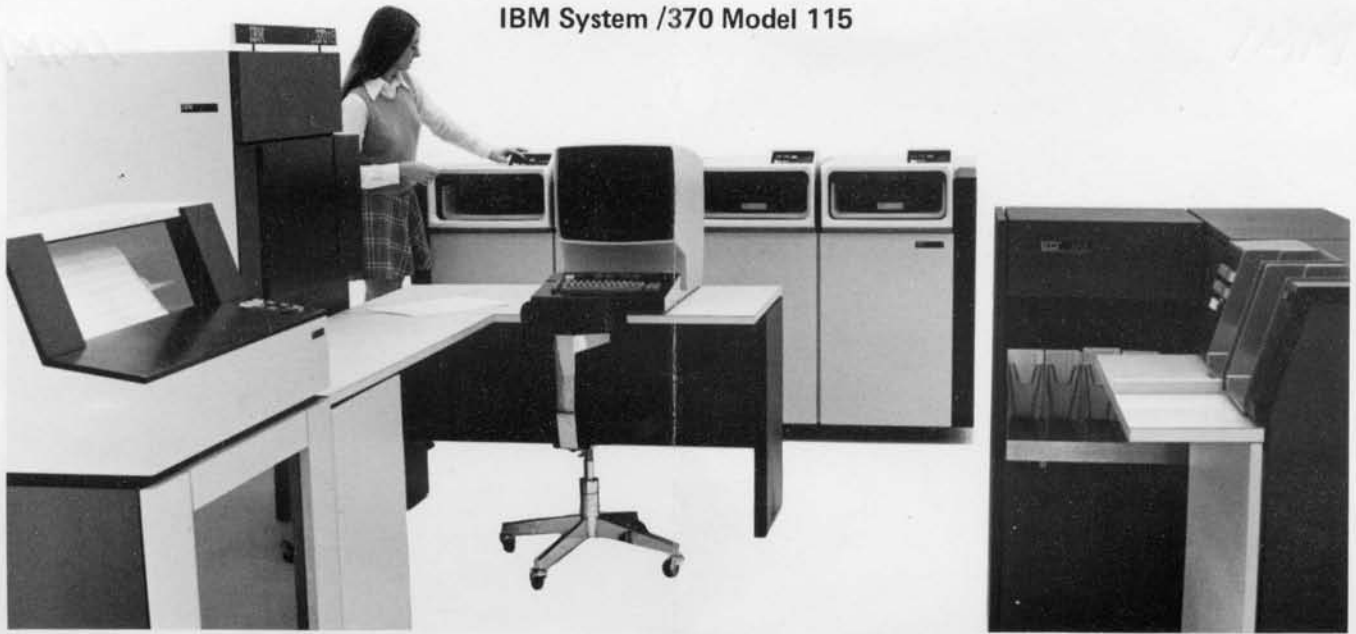
■ INCORPORATED MICROTTESTS

are part of the IOP control program. They monitor Card I/O operations and record marginal conditions during normal customer operations. These conditions are logged if an error occurs.

■ ERROR CHECKING AND CORRECTING (ECC)

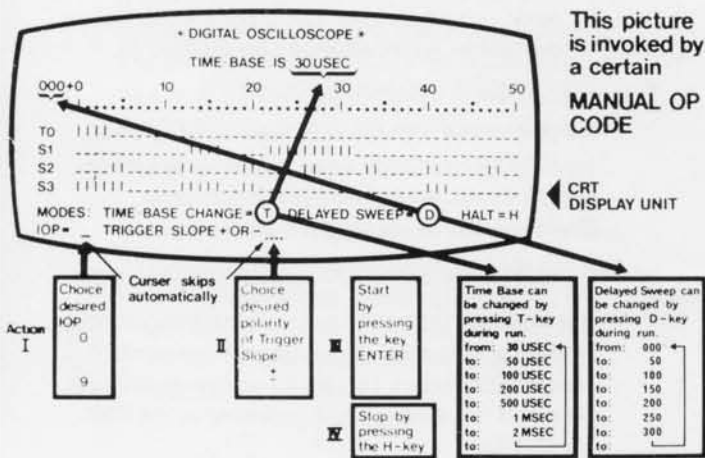
is a hardware feature of mainstorage, that automatically corrects single bit errors without performance degradation. Double bit and most multiple bit errors are detected and presented to the SVP for logging.

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■ DIGITAL OSCILLOSCOPE

The SVP together with the CRT can be used as a four-channel oscilloscope for MST-1 level signals in the I/O speed range. It offers stepwise variable time base, single and delayed sweep modes.



■ CE POWER TEST PANEL

provides an integrated voltmeter to check correct setting of voltages. Indicators identify failures in the power supplies, power sequence steps, thermal conditions or tripped Circuit Breakers.

■ LOG ANALYSIS PROGRAMS

are microprograms, that analyse the logged data stored on the console disk file. Results are presented to the CE on the video display showing parts to be replaced or actions to be taken.

■ MICRO DIAGNOSTIC PROGRAMS

exercise the hardware and diagnose errors. They display error reports on the CRT informing the CE about the parts to be replaced or the actions to be taken.

■ INLINE TESTS (ILTs)

can be invoked by the CE to run concurrent with customer operations. They test directly attached disks and ICA-lines working with Under Cover Modems. Error results will be logged.

■ ASCP

The Automatic System Checkout Program is a selfconfiguring system test. It is used to test the overall function of the system.

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System Diagnostic Support

- OLTs
On Line Tests are used to test the devices attached to the tape adapter and multiplexer channel, and also to test the 3340 disk drive and TP terminals.
- OLTEP
On Line Test Executive Program will be available as part of the operating system to run the OLTs concurrent with customer operation.
- OLTSEP
On Line Test Standalone Executive Program is a standalone control program to run the OLTs.
- EREP
The Environment Recording Edited Print program edits and prints data stored in the recorder file.
- SOSPP
The Standalone On Line Test Support Program provides the means to generate and maintain a complete and edited mastertape or disk file, used by OLTs and OLTEP/OLTSEP.


Standard CPU Features

System /370 Commercial Instruction Set
(including decimal instructions)

Store / Fetch Protection
Byte Oriented Operands
Time of day clock
Interval timer
Clock comparator and CPU timer
Program event recording
Monitor call
Extended control
Dynamic address translation
Channel indirect data addressing
Control registers
Extended I/O masking
Extended External masking
CPU / Channel Identification
Limited Channel Logout
I/O Error Alert

Optional CPU Features

Floating point instructions
External signals
Model 20 Emulator



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