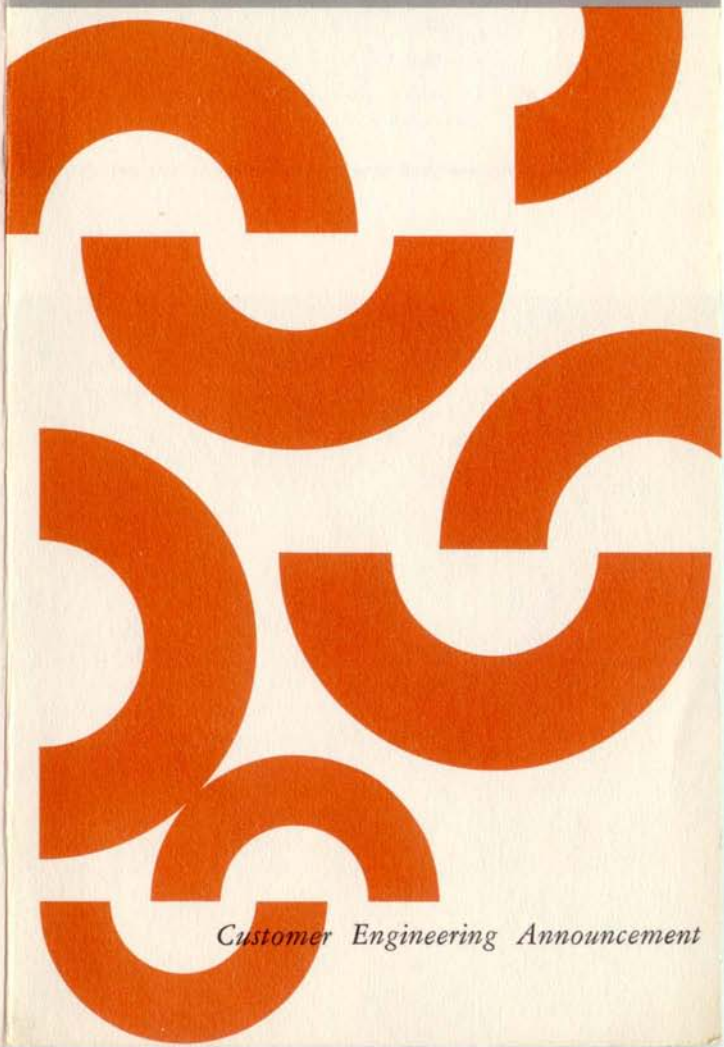
IBM 7094 Model II Data Processing System



Customer Engineering Announcement

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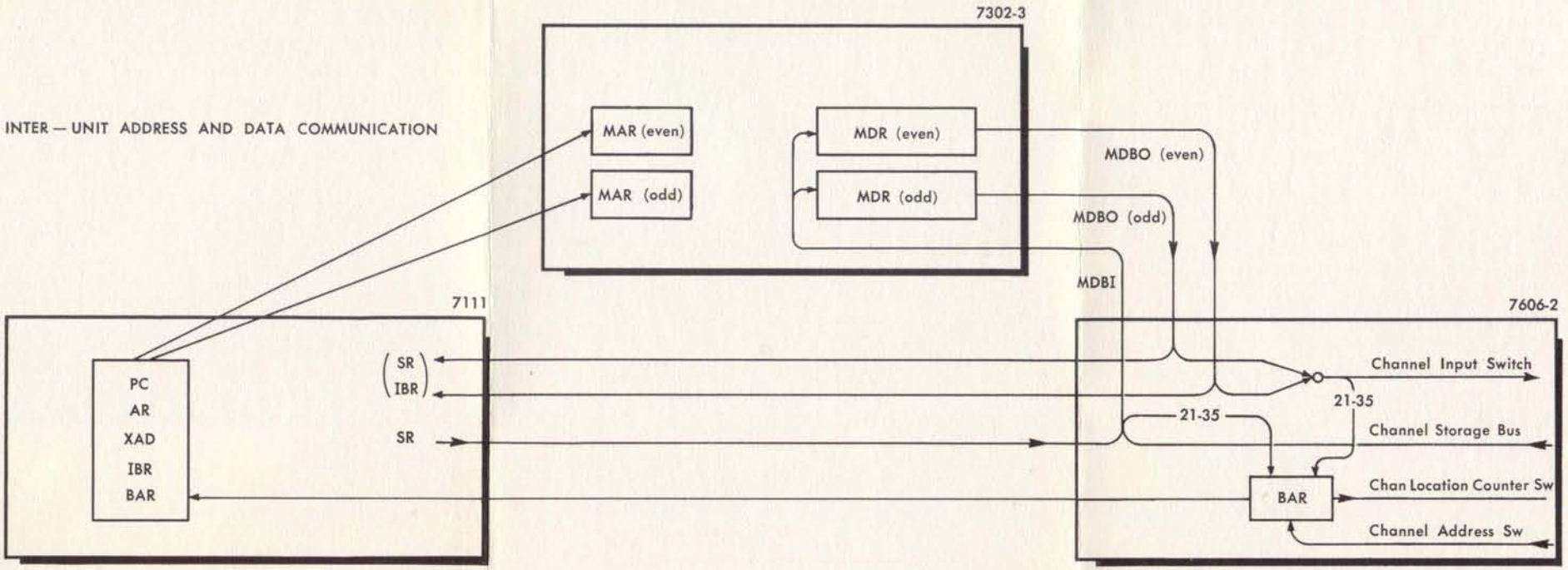

Customer Engineering Features

Four new diagnostic instructions have been added to provide diagnostic programming aids pertaining to the split memory and instruction overlap feature. These two new sets of instructions operate in conjunction with two corresponding toggle switches on the CE panel as follows:

1. The diagnostic switch aids in split memory diagnostics. When the switch is activated, address bits 3 and 17 in the CPU and channel are interchanged to locate memory positions 0-37,777$_8$ in one array and positions 40,000$_8$-77,777$_8$ in the other array. Two instructions provide a dynamic control over the switch to either enable or disable the diagnostic mode of operation. When the diagnostic switch indicates normal operation, both instructions have the effect of a NOP.

2. The overlap switch when activated prevents instruction overlap. The system can override the switch setting, however, by recognizing two instructions which either enable or disable overlapping. These two instructions have the effect of a NOP when the overlap switch is in the normal position.

7302-3 Core Storage

The new, air-cooled IBM 7302 Model 3 Core Storage provides two logically independent storage blocks of 16,384 words each. These two independent arrays can perform simultaneous fetches because each array has its own 14-bit Memory Address Register (MAR), 36-position Memory Data Register (MDR), and 36-position Memory Data Bus Out (MDBO). One Memory Data Bus In (MDBI) is located in the multiplexor and wired to both MDR's. Normal memory selection is under control of address bit 17 which is the lowest order address bit; memory selection in diagnostic mode is under control of address bit 3.

Two independent temperature-compensated supplies provide power necessary for the array drivers.

Installation and Conversion

The new IBM 7302-3 Core Storage replaces the present 7302, providing a dual 16K unit for the 7094-II.

A 7111 Instruction Processing Unit replaces the existing 7110 Instruction Processing Unit; a minimal change will be installed in the field on the 7606 Multiplexor (conversion to 7606-2), 7109 Arithmetic Sequence Unit, and 7151 Model 2 Console. All other units of the 7094 system are unaffected.

The 7094-II provides direct program compatibility with the 7090/7094 Systems but at substantially increased internal processing speeds.

New circuitry packaged on single, double and STAN-PAC cards achieves increased internal speeds.

A reduction in internal cycle time of the CPU and memory has been made from 2.0 to 1.4 microseconds.

New internal data paths have been added to augment instruction control, routing, and memory addressing.

Instruction Overlap is improved over that of the 7094 by the use of a dual memory technique; two logically independent memories of 16K 36-bit words are provided by the new IBM 7302-3 Core Storage. Organization of the memory referencing circuits allows two words to be addressed, one word from the *even* memory, and the other word from the *odd* memory; thus two words (not necessarily from sequential locations) can be fetched from the two memories, or one word can be fetched while another is being stored. In the fastest mode of operation, all I times are eliminated except for the I time of the initial instruction; i.e., all instructions are fetched during II time (IBR I time) which overlaps E or L time. This *extended sequence overlap* continues until a memory address conflict occurs or a sequence of instructions is encountered which, by the nature of their execution, must block overlap. The Instruction Backup Register (IBR) now plays an even more powerful lookahead function in decoding, execution control, and memory addressing.

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