370
3032

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3032 PROCESSOR

Description

The 3032 Processor is a large scale system designed with virtual storage capabilities. It consists of:

- A system console (3036) for operation, control and display of the system
- A power distribution unit (3027) to control distribution of customer supplied input power from the motor generator to the system
- A coolant distribution unit (3027) to provide a closed loop distilled water circulating system for cooling

The Processor (P) consists of an Instruction Pre-Processing Function (IPPF), an Execution E-Function, a Processor Storage Control Function (PSCF), Processor Storage, Retry and Maintenance Function, and Channels.

The IPPF fetches instructions and prepares them for execution by the E-Function. The IPPF also determines priority and makes fetch requests for instructions and operands.

The E-Function executes the instructions prepared by the IPPF and is capable of processing an instruction every cycle. The E-Function is primarily controlled by micro-programming within the control storage.

The PSCF processes all requests to store data into or fetch data from Processor Storage. Logical storage addresses are converted into real storage addresses for addressing Processor Storage. The PSCF also provides for execution of the Invalidate Page Table Entry (IPTE) instruction.

The Processor Storage is an integrated monolithic non-destructive readout storage. The storage technology is the MOSFET type. The Processor Storage is available in capacities of 2, 4 and 6 megabytes. The storage operates in a four-way interleave mode and a double word data width. The Pocessor Storage Control Function contains the Dynamic Address Translation (DAT), Translation Lookaside Buffer (LTB), high speed buffer, address array, storage protect, and channel buffers.

The control storage consists of 4K-72 bit words of Reloadable Control Storage (RCS) for control of channel and director operations, 2K-108 bit words of Reloadable Control Storage (RCS) in the E-Function and 64K times 5 bits of FET storage for each of the 2 console processors.

Retry and Maintenance Function
Detection of certain types of machine errors results in a retry of the processing function and a logout of the condition encountered.

CHANNELS

The basic 3032 Processor Complex includes one group of 6 integrated channels. A second group can be added to provide 6 additional channels. Each group provides 1 byte multiplexer and 5 block multiplexer channels. As an additional feature, the first block multiplexer channel of each group can be fitted with the highspeed 2 byte wide interface.

Logical function is microprogram controlled and uses 4K words of Reloadable Control Storage (RCS), 32K bytes of Bump Storage, 16 words of data local storage and 48 words of UCW storage.

COMPATIBILITY

The 3032 is upward program compatible with current System/360 and System/370, without extensive reprogramming with the following exceptions:

- Programs using machine-dependent data
- Programs using model dependent features or devices not available on this system
- Programs that depend on validity of data after system power has been turned off and restored
- Programs using ASCII bit (PSW bit 12)

TECHNOLOGY

The 3032 Processor uses the following Monolithic Systems.

Technologies:

- HDB/HDB-F
- MST 1
- MST 2
- MST 4
- MST 4 E
- MST E
- MSTA

The Reloadable Control Storage (RCS) and the high speed buffer use Advanced Bi-Polar Monolithic Technology.

The processor storage of the 3032 Processor employs MOSFET (Metal Oxide Semiconductor Field Effect Transistor) technology.

PERFORMANCE

The 3032 Processor is capable of an instruction execution rate significantly greater than the System/370 158-3. The high performance achieved can be attributed to:

- *The high speed and reliability of the technologies*
- *A Processor cycle of 80 nanoseconds*
- *A 32 K byte high speed buffer storage*
- *Multiple instruction and operand buffers*
- *Overlap of instruction and execute cycles*
- *Four way interleaved high performance processor storage*

A System/370 Extended Facility, when used with MVS System Extensions, provides significant additional throughput enhancements for MVS.

MANTAINABILITY

Maintenance of the 3032 Processor is enhanced through the use of the following facilities:

- *Extensive error checking and indicators.*
- *A system console with two stations: one for the operator and the other for maintenance. If either station experiences failure other than power, its functions can be performed by the other. The console processor and support console are used to display significant control and status latches/triggers. Also provides capability to dynamically retrieve and manipulate log and trace data.*
- *The last 12 logs per channel group, the last 12 events including trace and/or processor logs and 1K bytes of power messages are recorded.*
- *Logout analysis program for resolution of intermittent failures.*
- *Environmental Recording, Edit and Print Program (EREP)*
- *Processor microdiagnostics*
- *Functional tests under control of the Diagnostic Monitor (HDM)*
- *Power controlled by the Service Support Facility*
- *Marginal checking of processor logic*
- *A device using a magnetic disk cartridge to load microdiagnostics via a dedicated path.*
- *Retain/370 with data bank facility*
- *ON-Line Tests (OLTs) for I/O units are run under OLTEP for concurrent I/O maintenance.*
- *OLT's are run off-line under OLTSEP*
- *System Test/370 which is self-configuring*
- *Functional packaging of the processor logic.*

AVAILABILITY

The high availability of the 3032 Processor is attained through automatic recovery techniques which permit deferred maintenance.

Instruction Retry will, for most instructions (except Execute, Diagnose, Read Direct (RDD), Write Direct (WRD), and Test and Set (TS), completely re-execute the instruction following an error condition provided the retry threshold is not exceeded.

Channel Recovery is achieved through repetitive hardware retry and refresh of microcode instructions. Additional retry techniques are provided through software recovery support.

Error Correcting Code (ECC) will correct single bit storage data failures without interruption of the system.

Multiple bit storage errors can be deferred through software recovery using page refresh or deletion.

The Recovery Management Support (RMS) supplements hardware executed automatic retry facilities. RMS assesses the software condition and either reconstructs or selectively terminates the task.

One megabyte increments of processor storage can be configured off-line, enabling the system operations to continue.

STANDARD FEATURES

- *System 370 Universal Instruction Set*
- *Byte-Oriented Operands*
- *Direct Control*
- *Interval Timer*
- *TOD Clock and Clock Comparator*
- *CPU Timer*
- *Program Event Recorder (PER)*
- *32 K Byte High Speed Buffer*
- *Extended Control Mode*
- *Dynamic Address Translation (DAT)*
- *Storage Configuration Control*
- *Dual Purpose Console with Service Support Facility and CRT Display*
- *6 Channels*
- *Floating Point*
- *Extended Precision Floating Point*
- *External Signal*
- *Conditional Swapping*
- *PSW Key Handling*
- *2 MB Storage*
- *System/370 Extended Facility.*

OPTIONAL FEATURES

- *Block Multiplexer Two Byte Channel Interface*
- *6 additional channels*
- *Channel to Channel Adapter*
- *Two megabyte increments of storage to a maximum of 4 additional megabytes.*

CE CARIER PATH

This is a DP Product.