IBM Field Engineering

Theory of Operation

2870 Multiplexer Channel

(60,000 and 70,000 Series)

SY27-2300-1

PREFACE

This manual presents the fundamental concepts and operational principles for the 2870, 2870A, and 2870B Multiplexer Channels. The machine type suffix letters are determined by the system attachment and channel serial numbers. The channel designations are:

System/360 models (not including the Model 195)
2870 Ser. No. 60,000 and 60,002-69,999
2870A Ser. No. 60,001 and 70,000 Series

System/370 models (including the System/360 Model 195)
2870B 70,000 Series

The information contained herein relates principally to the 2870A as a basis for data presentation. When the 2870 differs slightly from the description provided for the 2870A series machines, the difference is shown in parentheses with an asterisk (*). For example, the 2870 has eleven (*seven) levels of priority. It is assumed that the reader has a basic knowledge of the System/360 and System/370 fundamentals of operation and standard I/O interface.

Because Engineering Changes may periodically obsolete portions of this manual, the latest level logic diagrams should be used as the final authority.

Note: References in this manual to COD (Channel Operation Diagram) and IOP (I/O Operation) diagrams relate to diagrams contained in Field Engineering Diagrams Manual, IBM 2870 Multiplexer Channel (60,000 and 70,000 Series), SY27-2301.

Additionally, references to flowcharts (FCXXX) also appear throughout the text of this and other chapters; these relate to the autocharts contained in Volume 1 of the 2870 ALD's.

Manuals associated with this publication are:
Field Engineering Diagrams Manual, IBM 2870 Multiplexer Channel, SY27-2301.
Field Engineering Maintenance Manual, IBM 2870 Multiplexer Channel, SY27-2302.

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SY22-6915 (dated September 20, 1972)
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Changes are periodically made to the specifications herein; any such changes will be reported in subsequent revisions or Technical Newsletters.

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ILLUSTRATIONS

ABBREVIATIONS

AC	Alternating Current
Adr	Address
Atn	Attention
BCU	Bus Control Unit
BI	Bus In
BO	Bus Out
CAW	Channel Address Word
CB	Circuit Breaker
CC	Chain Command
CCW	Channel Command Word
CDA	Chain Data Address
CE	Customer Engineer
Chan	Channel
Chk	Check
CIDA	Channel Indirect Data Address
Clk	Clock
COD	Channel Operation Diagram
Cmnd	Command
CPU	Central Processing Unit
CSW	Channel Status Word
Ctr	Counter
Ctrl Chk	Control Check
CU	Control Unit
Cyc	Cycle
DA	Data Address
EC	Engineering Change
EPO	Emergency Power Off
FLT	Fault Locating Test
Gnd	Ground
HIO	Halt I/O
IDA	Indirect Data Address
IDAL	Indirect Data Address List
IDALW	Indirect Data Address List Word
ILI	Incorrect Length Indication L
I/O	Input or Output
IOP	I/O Operation Diagram
IPL	Initial Program Load
k	Kilo
LDA	Load Data Address
LS	Local Storage
LSAC	Local Storage Address Check
LSAM	Local Storage Address Modify
LSAR	Local Storage Address Register
LW	Last Word
MCBC	Main Channel Byte Count
MCW	Maintenance Control Word
ms	Millisecond
MS	Main Storage
MSC	Multiplex Subchannel
ns	Nanosecond
Op	Operation
PCI	Program Controlled Interruption
Prgm Chk	Program Check
PS	Power Supply
Rd Bkwd	Read Backward
Reg	Register
Req	Request
Reqd	Required
Resp	Response
SA	Service Aid
SAB	Storage Address Bus
Sim	Simulate
SIO	Start I/O
SLI	Suppress Length Indication
SLT	Solid Logic Technology
SS	Singleshot
SSC	Selector Subchannel
Sta In	Status In
Sta Mod	Status Modifier
Store	Storage
Svc Out	Service Out
TB	Terminal Board
TCH	Test Channel
Tf	Turn Off
Tgr	Trigger
TIC	Transfer In Channel
TIO	Test I/O
Tn	Turn On
UA	Unit Address
UABO	Unit Address Bus Out
UCW	Unit Control Word
usec	Microsecond

INTRODUCTION TO CHANNELS

- Channels process I/O operations between control units and central processors.
- Two types of channels are used with System/360: selector channels for high-speed I/O devices, and multiplexer channels for low and medium speed devices.
- Selector channels operate in burst mode only, while multiplexer channels can operate in multiplex or burst mode.
- In multiplex mode, a multiplexer channel can operate more than one I/O device at a time.

Channels control the transfer of data between input/output (I/O) devices and the central processing unit (CPU). Channels are connected to the CPU and main storage and, via the I/O interface, with control units (Figure 1-1). The channel relieves the CPU of the burden of communicating directly with I/O devices and permits CPU operations to proceed concurrently with I/O operations.

The System/360 has two types of channels: multiplexer and selector. A multiplexer channel can operate in either multiplex mode or burst mode, depending on the device. Selector channels operate only in burst mode. In multiplex mode, the channel facilities are shared by a number of concurrently operating I/O devices. Multiplex mode causes all I/O operations to be split into short intervals of time during which only a segment of information is transferred over the I/O interface. In burst mode, one device monopolizes the I/O interface and stays connected to the channel for the duration of an operation. Normally, high-speed devices operate in burst mode only and are attached to a selector channel, while low and medium-speed devices may operate in either mode and are attached to multiplexer channels.

Within a channel, the facilities for sustaining an I/O operation with a device or control unit are termed a subchannel. The subchannel consists of the channel storage or registers used to record the address, data, count, and any status or control information associated with an I/O operation. The mode in which a channel operates depends on the number of subchannels it has.

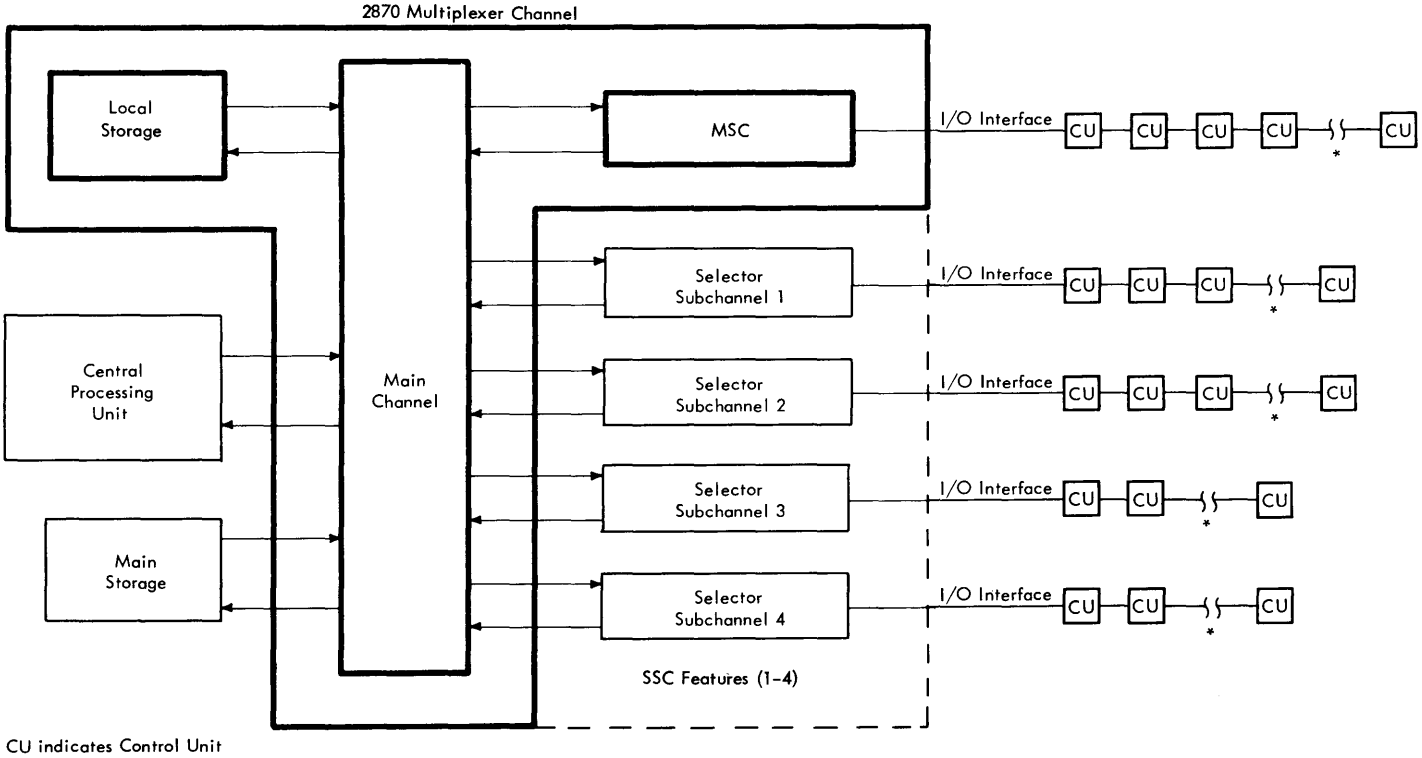


Figure 1-1. 2870 Multiplexer Channel with Selector Subchannel Features

A selector channel has one subchannel and always forces an I/O device to operate in burst mode. Multiplexer channels contain multiple subchannels and can operate in either multiplex or burst mode. In multiplex mode, the number of devices that may operate concurrently depends on the number of subchannels within the channel. However, only one I/O device at a time can operate in burst mode on a multiplexer channel.

2870 MULTIPLEXER CHANNEL

- Allows low- and medium-speed I/O control units and devices to be attached to IBM System/360 Model 65, 67, 75, and Model 90 series processors.
- The basic 2870 has 192 subchannels and one I/O interface, and can operate as many as 192 I/O devices concurrently.
- As many as four selector subchannel features, each with an I/O interface, can be added to the basic 2870.
- Each selector subchannel can have 16 I/O devices attached, but can only operate one device at a time.

The IBM 2870 Multiplexer Channel is a high-performance data multiplexing channel for processing I/O operations between a CPU and I/O devices. The 2870 can be attached to an IBM System/360 Model 65 processor without modification. However, an address prefixing feature must be installed on both the 2870 and the CPU to allow operations with an IBM System/360 Model 67 duplex system, a CPU/BCU interface feature is required for attachment to a Model 75, and a different CPU/BCU interface feature is required for attachment to processors of the Model 90 series. These features are described in Chapter 4 of this manual.

The basic 2870 has one I/O interface (multiplex or burst mode) capable of attaching as many as eight control units (Figure 1-1). Within the basic 2870, there are 192 subchannels which can control 192 I/O devices. Any number of the 192 I/O devices can be operating concurrently (multiplex mode) on the I/O interface at a maximum aggregate data rate of 110 kilobytes. That is, portions of various messages can be transmitted over the interface in an interleaved fashion to or from different I/O devices. If either the 2870 or an I/O control unit forces a burst mode operation on one of the subchannels, that subchannel monopolizes the I/O interface and can transfer data at a maximum rate of 110 kilobytes. Each subchannel is identified by the unit address of the device assigned to it. Either the CPU or an I/O control unit can access a particular subchannel by presenting to the 2870 the device address associated with that subchannel. It is important to note that there are no shared subchannels in the 2870.

In the 2870, multiplexing is accomplished by splitting I/O operations into short intervals of time during which only a segment of information is transmitted over the interface. A multiplexed data transfer can involve a single data byte or multiple bytes. To qualify as multiplex mode, a multibyte data transfer must not last more than 64 microseconds. Any operation that takes more than 64 microseconds is considered a burst mode operation. In the 2870, multiplexing is a device-demand type operation. That is, after the 2870 initiates an I/O operation with a device, the 2870 depends on the I/O control unit to request data or status transfers. The 2870 does not poll the control units.

As many as four selector subchannel features can be added to the basic 2870. Each selector subchannel feature adds one burst mode I/O interface to the 2870, and can have as many as eight control units attached. Each selector subchannel can address as many as 16 I/O devices, but all operations occur in burst mode and only one device at a time can operate with a selector subchannel. The first three selector subchannels have a maximum data rate of 180 kilobytes and the fourth has a maximum data rate of 100 kilobytes. The selector subchannels can be used to enter fault locating tests (FLT's) into the CPU.

A 2870 with four selector subchannel features has a total of 196 subchannels and can address as many as 256 I/O devices. However, because there are only 196 subchannels available, the maximum number of I/O devices that can operate concurrently is 196.

The 2870 Multiplexer Channel is packaged in its own frame and uses 30-ns and 10-ns (for local storage) solid logic technology (SLT) circuits. Power for the channel is supplied by seven mid-pac regulators (six for the basic 2870 and one additional regulator if any selector subchannels are added). A CE console allows both the selector and multiplex subchannels to be operated and tested off-line. A power control panel allows power sequencing to be locally or remotely controlled, and provides facilities for marginal checking of the channel. A customer usage meter is also provided on the power control panel to record channel running time.

Data Transfer Rate

- The basic 2870 Multiplexer Channel has a maximum aggregate data rate of 110 kilobytes per second.
- Selector subchannel features 1-3 have a maximum data rate of 180 kilobytes per second.
- Selector subchannel feature 4 has a maximum data rate of 100 kilobytes per second.
- Each selector subchannel feature added reduces the maximum aggregate data rate of the multiplex subchannels.

The 192 subchannels of the basic 2870 make it possible for the 2870 to operate as many as 192 I/O devices concurrently, on a single I/O interface, at a maximum aggregate data rate of 110 kilobytes per second. That is, portions of various messages can be transmitted over the interface, in an interleaved fashion, to and from different I/O devices. However, if either the channel or the control unit forces a burst mode operation on one of the multiplex subchannels, the maximum data rate is 110 kilobytes and that subchannel monopolizes the I/O interface.

A total of four selector subchannels can be connected to the 2870. The first three selector subchannels have a maximum data rate of 180 kilobytes per second, and each reduces the maximum aggregate data rate of the multiplex subchannels by 22 kilobytes. The fourth selector subchannel has a maximum data rate of 100 kilobytes, and reduces the aggregate data rate of the multiplex subchannels by 14 kilobytes. Figure 1-2 shows the maximum data rates of the 2870 with various combinations of subchannels. However, because programming for both the system and the channel affects the maximum data rate the 2870 can sustain, these data rates represent the ideal maximum for the channel.

Major Units of the 2870

- The 2870 Multiplexer Channel's circuitry can be divided into four functional areas: main channel, local storage, the multiplex subchannel, and the selector subchannels.
- To eliminate confusion with the 192 multiplex subchannels, the channel circuitry called the multiplex subchannel (in ALD's) is abbreviated as MSC.
- Main channel's circuits perform the housekeeping, control, and main storage operations of the 2870.
- Local storage is used to retain data, status, and control information for the I/O devices attached to the channel.
- The MSC consists of registers and control circuits used by the multiplex subchannels to transfer information and control signals between main channel and the multiplex I/O interface.
- The selector subchannels consist of the registers and control circuits used to gate and buffer data and control information over the selector I/O interfaces.

As shown in Figure 1-1, the 2870 can be divided into four functional areas: main channel, local storage, the MSC, and selector subchannels. Main channel and local storage provide the storage, the registers, and the control sequences necessary for both the multiplex and selector subchannel I/O operations. The MSC is the shared data path used by the multiplex subchannels to communicate with devices on the multiplex I/O interface. Each selector subchannel contains the registers necessary to control data transfer operations with one device at a time.

Main Channel

The main channel contains a clock, an adder, registers, control sequences, and a priority circuit (Figure 1-3). Main channel operates with local storage to provide the storage, the registers, and the control sequences necessary to support both the

Multiplex Subchannels (kilobytes)	Selector Subchannel 1 (kilobytes)	Selector Subchannel 2 (kilobytes)	Selector Subchannel 3 (kilobytes)	Selector Subchannel 4 (kilobytes)	Total 2870 Data Rate (kilobytes)
110	0	0	0	0	110
88	180	0	0	0	268
66	180	180	0	0	426
44	180	180	180	0	584
30	180	180	180	100	670

Figure 1-2. Maximum Byte Data Rate

multiplex and selector subchannel operations. Main channel performs such housekeeping functions for the subchannels as: updating command addresses, data addresses, and counts. All communications with CPU and main storage are handled by main channel. Main channel performs the housekeeping, control, and data handling functions of the 2870 as follows:

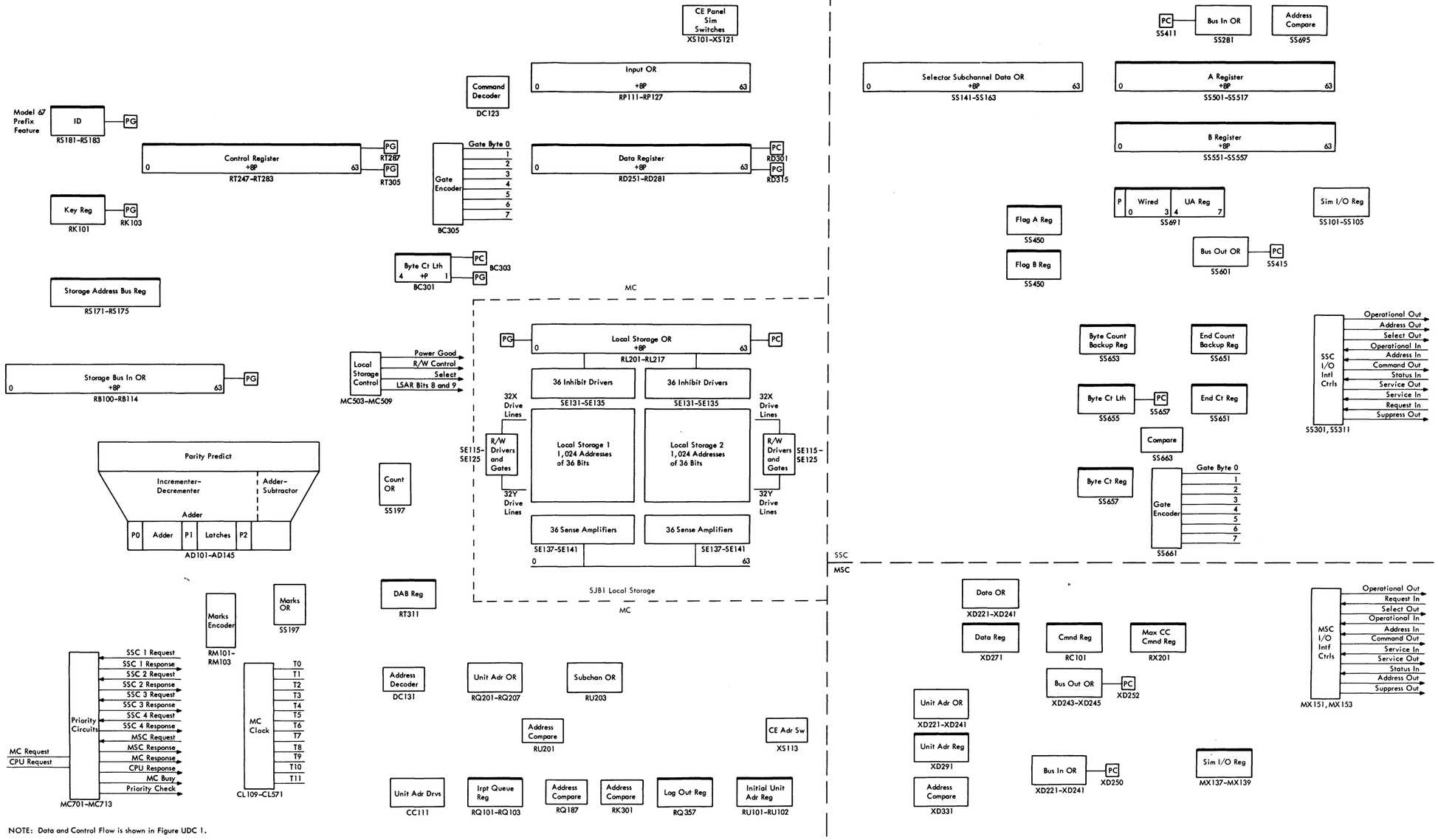
1. Receives I/O instructions and unit addresses from the CPU and selects the proper subchannel and device to execute the instructions.
2. Directs the flow of control information and data between the subchannels and main storage.
3. Maintains and updates addresses and counts used in I/O operations.
4. Contains a priority circuit to control which unit has access to the main channel's controls and registers if two or more requests are received at one time.
5. Controls the formation of a CSW when an operation terminates.
6. If a logout is required, main channel forms the log words and places them into local storage.

Main channel receives I/O instructions and unit addresses from CPU and controls the selection of the subchannel and device to execute the instructions. For example, a start I/O instruction causes the main channel to: select the addressed subchannel, fetch the CAW and first CCW involved, and select the addressed device. Once a data transfer type I/O operation is started, main channel is used for all data transfers between main storage and the 2870 and for all multiplex subchannel data transfers (I/O interface and main storage). The difference between multiplex and selector subchannel data handling is that a multiplex subchannel must use main channel and local storage for each byte of data transferred across the multiplex I/O interface, while selector subchannels only use main channel and local storage for main storage transfers (doublewords).

During data handling operations, main channel also updates the data address and count associated with the operation. For a multiplex subchannel, the count is updated for each byte transferred and the data address is updated on each main storage transfer (doubleword). For selector subchannels, the data address and count are only updated by main channel when a main storage cycle is performed. The data address updates are necessary to be sure that data is stored in the correct main storage location. The count field is decremented to ensure that the operation ends when the specified amount of data has been transferred (count = 0).

To control which unit has access to main channel's control sequences and registers, main channel contains a circuit called "priority." The priority circuit assigns a rank to all units that desire access to main channel, and allows access only by rank. If a high-ranking unit such as a selector subchannel desires access at the same time as a low-ranking unit such as CPU, access is granted to the selector subchannel. Only one unit can have access at a time. Selector subchannels are assigned two levels of rank depending on the type of operation they wish to perform. The order of rank is called priority and is assigned as follows:

1. Selector Subchannel 1 Primary Request -- the selector subchannel is performing a data transfer operation with a device and has either read in or gated out a doubleword of data. Main channel is needed to perform a main storage data store or fetch and to update the data address and count (held in local storage) for the operation.
2. Selector Subchannel 2 Primary Request -- same as 1.
3. Selector Subchannel 3 Primary Request -- same as 1.
4. Selector Subchannel 4 Primary Request -- same as 1.
5. Multiplex Subchannels Interface -- the multiplex I/O interface has service in or status in active from an I/O control unit. This indicates that a device is demanding service for either a data or status cycle with its subchannel.
6. Selector Subchannel 1 Secondary Request -- the selector subchannel activates this request when it needs main channel's circuits to:
    a. Fetch the next CCW from main storage for a chained operation.
    b. Assemble a CSW at the termination of an I/O operation.
    c. Fetch one or two doublewords of data from main storage at the beginning of a write operation.
7. Selector Subchannel 2 Secondary Request -- same as 6.
8. Selector Subchannel 3 Secondary Request -- same as 6.
9. Selector Subchannel 4 Secondary Request -- same as 6.
10. Main Channel Priority Request -- this request line is activated by main channel to its own priority circuit when:
    a. CPU issues a start I/O, test I/O, or halt I/O instruction to the channel.
    b. A multiplex subchannel is reselecting its I/O device on the multiplex I/O interface and needs a CCW or a doubleword of data.
11. CPU Priority Request -- the CPU is responding to an interrupt request issued by the 2870. A CSW is to be stored into main storage.



NOTE: Data and Control Flow is shown in Figure UDC 1.

Figure 1-3. Major Units of the 2870

Note that the selector subchannels are assigned priority in order of their numbers. The overall priority assignment reflects the urgency of service requirements. A selector subchannel cannot afford to be held up too long when it has a tape write operation going and needs more data. Therefore, selector subchannel data refill requests have highest priority (1-4). At the beginning of a write operation, the selector subchannel has time because the tape unit has not started, and this request has much lower priority (6-9). Each operation only ties up main channel for part of its sequence and other operations are allowed to break in. An operation such as a multiplex subchannel's data transfer will use main channel many times (for each data byte, and for all doubleword transfers with main storage). Each time the subchannel requires a data transfer, a priority request is made. When priority is granted, the data transfer and update operations are performed and main channel is released.

Main channel also contains eleven trigger sequences that are used to control such operations as: data handling, chaining, and CSW formation. Each time a subchannel requests priority to perform an operation, main channel's priority response to that subchannel is used to gate the subchannel's signal lines to main channel. The subchannel and its signal lines determine which trigger sequence is performed. The triggers are defined in Chapter 3 of this manual.

If an error occurs, during an operation and a logout is required, main channel forms three doublewords of log information and a CSW. This logout information is then placed in local storage. If the 2870 is in automatic mode and the log-on-machine-check switch (on the CE console) is on, the three log words and CSW are transferred to main storage.

Local Storage

To operate many I/O devices concurrently, information concerning each device and the operation it is performing (including being idle) must be stored in the channel. In the 2870, this information storage is provided by the local storage unit (Figure 1-3).

Local storage in the 2870 consists of two SJB 1 units in parallel; each SJB 1 has a capacity of 1,024 words (36 bits). This gives the 2870 a local storage of 1,024 doublewords (72 bits). A read or a write cycle requires 500 nanoseconds, and a read/write cycle requires 1 usec. To facilitate main channel operations, multiple read cycles can be performed before a write cycle is required.

All the 1,024 available addresses are assigned. For each of the 256 possible I/O devices that can be attached to the 2870, four local storage words (72 bits), called unit control words (UCW's), are assigned. The local storage address for each of these groups of UCW's is the unit address of the device (and its subchannel) to which they pertain. Main channel determines which UCW of the group is to be accessed by adding two modifier bits to the unit address. The UCWs are defined in a separate section.

MSC

As previously defined, a subchannel is the channel storage and registers used to store the address, data, count, and any status or control information associated with an I/O operation. This is the meaning a programmer applies to the term subchannel when he issues a test I/O instruction to a device and CPU receives a condition code which indicates that the subchannel is busy and cannot accept another operation at this time. In a channel such as the IBM 2860 Selector Channel, this subchannel information is actually held in the channel registers. In the 2870, the addresses, data, count, and status or control information for the 192 devices attached to the multiplex I/O interface are stored in local storage until needed. When an operation for a multiplex device is required, the device address is presented (by either CPU or the device), the subchannel information is read from local storage to main channel's registers, and the operation is performed. As explained previously, each multiplex operation is split into short segments (unless a burst mode operation is forced) and each segment only uses main channel for a short period of time. Because main channel interleaves I/O operations for as many as 196 subchannels (including main storage operations for the selector subchannels), the registers and control sequences of main channel are considered shared.

To distinguish the portion of the 2870 circuits used only by the 192 multiplex subchannels to communicate with devices on the multiplex I/O interface, this group of registers, latches and gating ORs is called "the multiplex subchannel" in ALDs. To help eliminate confusion, the multiplex subchannel (circuits) is abbreviated as MSC, and the channel information concerning a device on the multiplex I/O interface is spelled out: multiplex subchannel.

The MSC consists of: a bus in OR, a unit address OR, a unit address register, a unit address compare circuit, a data OR, a data register, a bus out OR, a command register, a multiplex chained command-command register, and a simulate I/O register (Figure 1-3). These registers and ORs are used by the multiplex subchannels as a shared data and control path. That is, the multiplex subchannels (one at a time) use these registers and their control latches to transmit information in an interleaved

fashion between different I/O devices and main channel. The MSC also contains the circuits necessary to control the multiplex I/O interface.

Selector Subchannels

The selector subchannels are module additions to the basic 2870 that permit the channel to control as many as 16 high-speed I/O devices (up to 180 kilobytes) on each of the four possible selector subchannel I/O interfaces. However, each selector subchannel I/O interface can only have a maximum of eight I/O control units attached. As stated before, only four selector subchannels can be added to the 2870 and all operations occur in burst mode. For each of the 16 possible I/O devices that can be attached to a selector subchannel, a set of four UCW's are assigned.

The selector subchannels each have: two data registers (A and B), a byte counter, end count registers, two flag registers (A and B), a unit address register, and the necessary circuitry to control its own I/O interface (Figure 1-3). The selector subchannels transfer data to or from the I/O interface one byte at a time, and to or from the main channel data register (ultimately to or from main storage) in doublewords. The byte count registers control the gating of the selector subchannel data registers for read, write, or status operations. The end count registers ensure that an I/O operation ends on the correct number of bytes. The unit address register and an address compare circuit are used to ensure selection of the correct I/O device for an operation.

The selector subchannels use main channel registers and sequences to control main storage (doubleword) data fetch or store operations, or to form a CSW when an I/O operation terminates. To initiate an operation with main channel, the selector subchannel raises its priority request line. When priority is granted by main channel, the selector subchannel's signal lines determine which main channel sequence is to be performed (data transfer or CSW). These main channel sequences for the selector subchannel are also controlled by the UCWs assigned to the device involved. This is done because the selector subchannels store data, count, and control information for up to 16 bytes of data, but all main storage addresses and the major count portion of the control information for an operation are stored in the device's UCWs (in local storage). Therefore, when a selector subchannel completes a doubleword data transfer, main channel and local storage are used to fetch or store a doubleword of data in main storage, and update the data address and count. The UCWs are described in a separate section.

I/O Device Addressing

- Device address is referred to as unit address by the channel.
- The I/O device address is composed of channel address and unit address.
- The channel has a maximum addressing capability of 256 devices.

A unique address identifies each I/O device attached to a system. This address is specified by an eleven-bit binary number which appears in each I/O instruction. There are two parts to the address: the channel address, which specifies the channel to which the address applies, and the device address, which specifies the particular subchannel and device on the channel. The three high-order bit positions of the eleven bit address number contain the channel address, and the eight low-order bit positions contain the device address. The device address is referred to as unit address by the 2870. A maximum of 256 devices (0-255) can be addressed by the 2870. Of these 256 possible devices, 192 devices controlled by the multiplex subchannels, and each of the four possible selector subchannel features has a capacity of 16 devices. Addresses that specify non-operational selector subchannels or devices are invalid. A component in the system is not operational when it is either not provided or has been switched to test mode.

The following addresses are reserved for the selector subchannel features:

P 0 1 2 3 4 5 6 7	Bit Positions
X 1 1 S S X X X X	Address Bits

Bit positions 0 and 1 must be 1 to denote selector subchannel operations.

Bit positions 2 and 3 designate the particular selector subchannel to be used.

SS

00 -- Selector Subchannel 1

01 -- Selector Subchannel 2

10 -- Selector Subchannel 3

11 -- Selector Subchannel 4

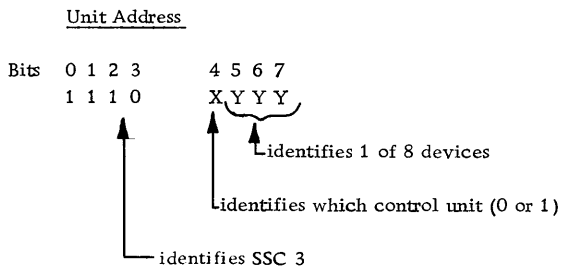
Bit positions 4-7 may be 0s, or 1s, and they define the device address.

Note that the high-order bit positions of a selector subchannel device address must be one. Do not confuse this addressing scheme with the shared UCW concept used on some other multiplex channels. On the 2870, there are no shared UCWs.

If the 2870 unit addressing system is converted to hex, the devices are attached as follows:

1. The 192 multiplex subchannels and their associated devices operate over the multiplex I/O interface and have addresses "00" through "BF."
2. Selector subchannel 1s I/O interface is used to communicate with devices addressed "C0" through "CF."
3. Selector subchannel 2s I/O interface is used to communicate with devices addressed "D0" through "DF."
4. Selector subchannel 3s I/O interface is used to communicate with devices addressed "E0" through "EF."
5. Selector subchannel 4s I/O interface is used to communicate with devices addressed "F0" through "FF."

In the 2870, the addressing scheme for selector subchannels also places a restriction on control unit addressing. Only two control units, such as the 2803, which are addressed by the five high-order bits (bits 0-4) of the device address can be attached to a selector subchannel. Because the selector subchannel addressing involves the four high-order bits (bits 0-3) only the fifth bit (bit 4) is left to determine the control unit address. This means that these control units can only be designated as unit 0 or unit 1 on the selector subchannel interfaces. However, this restriction only affects the control units, and sixteen 2400 tape units can be attached to a selector subchannel I/O interface (eight units to each control unit) as follows:



Interface

For the 2870, the following interfaces are defined:

CPU Interface
BCU Interface
I/O Interface
Selector Subchannel
Local Storage

CPU Interface

The interconnections between the CPU and the 2870 are defined as the CPU interface (Figure 1-4). This interface with its associated controls is classified in three groups: operation lines, diagnostic lines, and fault locating test (FLT) controls.

Operation Lines: The operation lines (Figure 1-4) provide the only control required during normal program operation and are used in all modes to furnish this information to the 2870. The operation lines are defined in the Interface Definitions section.

Diagnostic Lines: The diagnostic lines (Figure 1-4) are used by the CPU to assume diagnostic control of the 2870. These lines check the validity of the channel checking functions. The diagnostic lines are defined in the Interface Definitions section.

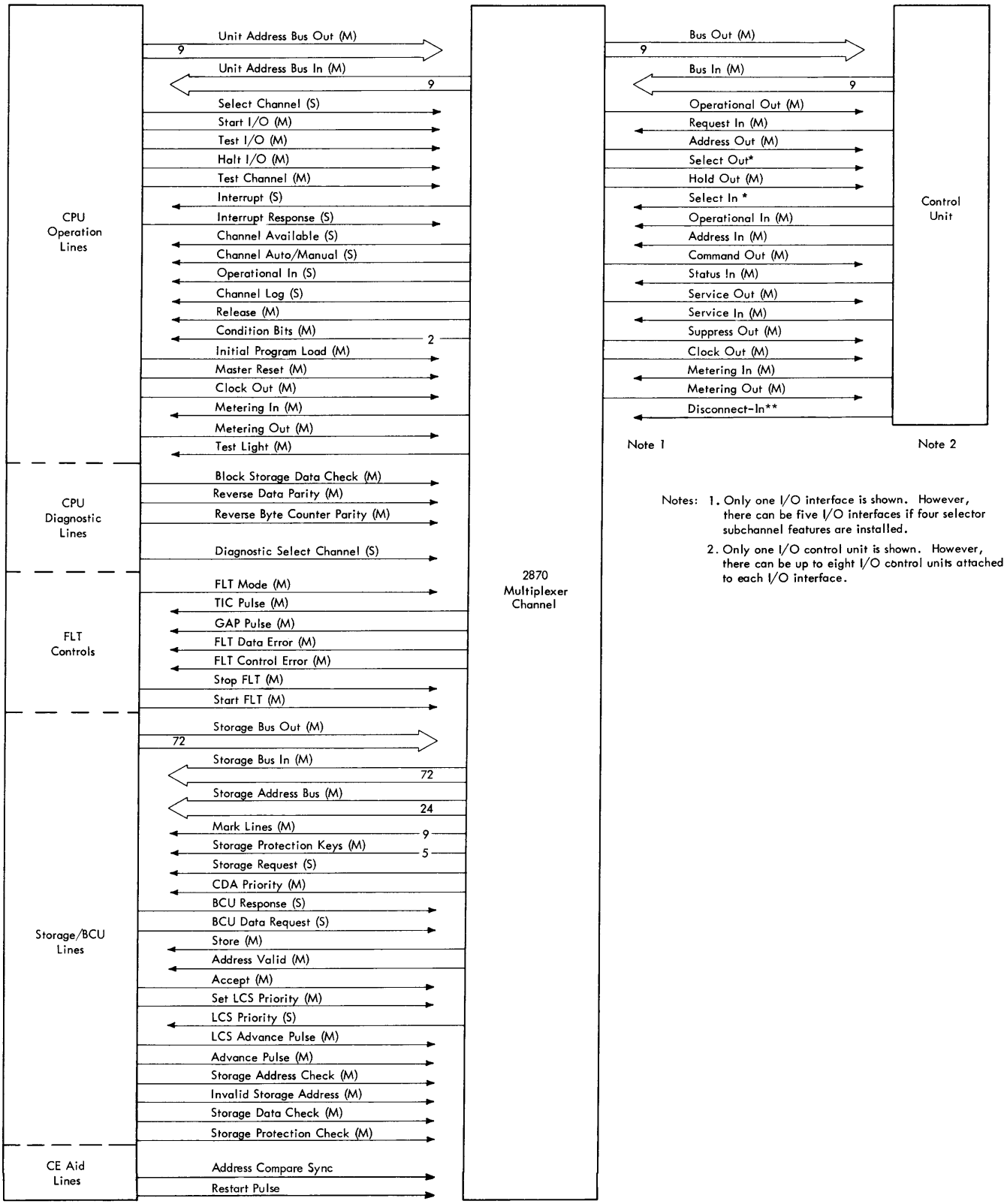
Fault Locating Test (FLT) Controls: The FLT controls (Figure 1-4) are available with the addition of the first selector subchannel feature to make possible the implementation of the scan portion of the CPU maintenance controls. The scan operation requires the breaking up of large volumes of data into short tests. This data is on tape and must be brought into storage without benefit of CPU instructions or interruptions. Therefore, the 2870 works in conjunction with the FLT controls to supply the data, keep the FLT controls aware of progress, retry when data errors are discovered, and start and stop transmission when instructed by the FLT controls. The FLT interface lines are defined in the Interface Definitions section.

Storage or Bus Control Unit (BCU) Interface

A 2870 operation is initiated when the CPU instructs the 2870 to commence a particular operation (start I/O, halt I/O, test I/O, or test channel). After the 2870 accepts the instruction, it independently obtains commands and transmits data to or from storage until the operation is completed. The storage or BCU interface lines (Figure 1-4) are defined in the Interface Definitions section.

I/O Interface

The I/O interface lines (Figure 1-4) are the interconnection between the 2870 and the control unit or units. The I/O interface provides an information



Notes:
1. Only one I/O interface is shown. However, there can be five I/O interfaces if four selector subchannel features are installed.
2. Only one I/O control unit is shown. However, there can be up to eight I/O control units attached to each I/O interface.

(M) Indicates a multiplex line
(S) Indicates a simplex line
* Select out is a single line that goes to each control unit in series and returns to the channel as a line called select in.
** EC 262203 installed

Figure 1-4. 2870 Multiplexer Channel Interface Lines

format and a signal sequence common to all control units. The interface consists of a set of lines that connect a number of control units to the 2870.

Except for the lines used to establish selection control, all communications to and from the 2870 occur over a common bus; any signal provided by the 2870 is available to all control units. At any one instant, however, only one control unit can be active on the interface.

Selection of a control unit for communication with the 2870 is controlled by the select out signal passing serially through all control units and permits, sequentially, each control unit to respond to the signal. A control unit remains logically connected on the interface until it transfers the information it needs or has, or until the 2870 signals it to disconnect. These I/O interface lines are defined in IBM System/360 I/O Interface -- Channel to Control Unit, Original Equipment Manufacturers' Information, form Z22-6843.

Selector Subchannel to Main Channel Interface

Communication between the selector subchannels and the main channel is carried out over shared signal lines; these lines are time-shared by as many as four selector subchannels. All subchannels desiring to be serviced by the main channel must vie for access to these signal paths through a priority network. A selector subchannel may activate these signal lines only when it receives a response signal in answer to its priority request. These selector subchannel to main channel interface lines are defined in the Interface Definitions section.

Main Channel to Selector Subchannel Interface

This signal interface uses both levels (L) and pulses (P) to transfer information from the main channel to the selector subchannels. A majority of the signals feed buses which are common to all of the selector subchannels. The remaining signals are routed directly to each individual selector subchannel and may be either levels (L) or pulses (P). The main channel to selector subchannel interface lines are defined in the Interface Definitions section.

Local Storage to Main Channel Interface

This interface provides signal and control paths between the main channel and local storage. Local storage interface lines do not have the same line titles in the main channel and local storage. The local storage interface lines are defined in the Interface Definitions section.

UNIT CONTROL WORDS

- Because the 2870 can perform many operations at one time, control information for each device is placed in local storage until needed.
- For each device four doublewords of information, called unit control words (UCWs), are assigned.
- In the 2870, there are no shared UCWs.
- Normally, multiplex devices use all four UCWs, while SSC devices use only two.
- Logouts for both the selector and multiplex subchannels use all four UCWs.

Local storage is used by the channel to store control information for all devices attached to the 2870. Such information as: the CAW, CCW, CSW, or data for I/O operations are stored in local storage until needed. To store all control information for a device, four doublewords (64 data bits +8 parity bits) are assigned to each device. Multiplex devices use all four doublewords, while SSC devices use only two. However, if a logout occurs, all four doublewords are used by both the multiplex and selector subchannels to store log words and a CSW.

The group of four UCWs for a device is addressed by the group's eight unit address bits. Main channel controls determine which UCW is used during an operation by adding two modifier bits to the unit address. In the 2870, if the two high-order bits of the unit address are one, the device is attached to an SSC. In some other multiplex channels, this indicates shared UCW's; however, in the 2870, there are no shared UCWs.

If a logout occurs for a multiplex or selector subchannel, all four of the assigned UCWs are used. UCWs 0, 1, and 3 are loaded with the three doublewords of log information, and a CSW is placed in UCW 2. If the channel is in automatic mode, interrupt request is raised to the CPU. When interrupt response is granted by the CPU, the first log word is transferred from local storage to main storage; a channel to main storage transfer is allowed; and another log word is transferred. This continues until all three log words and the CSW are transferred to main storage. The logout sequence is described in the logout section.

SSC UCW's

- SSC devices use UCWs 0 and 2.
- UCW 0 is the CCW modified for channel use.

- UCW 2 contains CAW information unless a CSW cycle has occurred.

- After a CSW cycle, the CSW is temporarily stored in UCW 2.

- If a logout occurs, three log words and a CSW are formed and placed in the UCW's assigned for the device.

Devices attached to the SSC I/O interfaces use only two UCW's to control their normal operations. UCW 0 holds CCW information, while UCW 2 holds either CAW or CSW information.

When the CPU issues a start I/O instruction to a device, main channel forms UCWs 0 and 2 from the CCW and CAW respectively. As the start I/O instruction is performed, UCW 0 controls main storage data transfers. During each main storage data transfer, UCW 0 is examined for ending with or without chaining. If chaining is not indicated when the operation ends (count = 0, or a device termination), a CSW is formed and placed in UCW 2. If chaining is indicated, UCW 2 is read out and the new CCW is fetched using the address supplied by UCW 2. During the CCW fetch cycle, UCW 2 is updated to point to the next CCW and a new UCW 0 is formed from the CCW. This operation continues until the chain of CCWs is exhausted; then a CSW is formed and placed in UCW 2.

If a logout occurs for an SSC device, three log words and a CSW are formed. These log words describe the type of error that caused the logout and the operation that was being performed when the logout occurred. The log words and CSW are placed in local storage (in the four UCWs assigned to the device). If the channel is in automatic mode and the log-on-machine-check switch is on, the log words and CSW are sent to main storage. The logout information can be manually read out of local storage to the control register and examined.

SSC UCW 0

Because the SSC's have data buffers and a byte counter, UCW 0 is only used to control main storage data transfers. For each doubleword of data that must be fetched or stored from the SSC, UCW 0 is read out to provide the data address, count, and flag indications necessary to control the operation. UCW 0s count and data address fields are then updated to prepare for the next operation and UCW 0 is stored back in local storage. UCW 0 is basically the CCW modified to control 2870 operations and can apply to these operations:

1. If the device is idle, UCW 0 describes the last operation performed.
2. If an operation is in progress, UCW 0 contains the current CCWs information.
3. When the count becomes less than 16 during a write CDA operation, the next CCW is prefetched and a new UCW 0 is formed.

The first UCW 0 for an operation is formed from the key field of the CAW and the first CCW. If chaining occurs, the CAW key is kept and the new CCW information replaces UCW 0's contents. UCW 0 is shown is Figure 1-5, and the fields are defined as follows:

Storage Key (Bits 0-3): This is the storage protection key taken from the CAW (fetched during a CPU start I/O instruction). This key field is loaded into the key register and sent to main storage on every data transfer.

Operation (Bits 6, 7): These bits are the encoded command field of the CCW. Main channel uses these bits during SSC data transfers to determine whether the transfer is an input or output operation. The bits mean:

Bit 6	Bit 7	
0	0	Idle
0	1	Write or Control
1	0	Read or Sense
1	1	Read Backward

Data Address (Bits 8-31): This is the main storage address for the next data transfer. For a read or write operation, this field is incremented by eight for each doubleword of data transferred, and decremented by eight for a read backward. This field is taken from the CCW.

For a read backward operation, bits 29-31 are complemented when UCW 0 is formed. For either a forward or backward operation, bits 29-31 are used to gate the main storage marks encoder on the first data transfer. After the first data transfer, bits 29-31 are reset.

Flags (Bits 32-36): The flag bits are taken from the CCW flag field and serve the same functions. Bits 32-34 (CC, CD, SLI) are also stored in the SSC flag register.

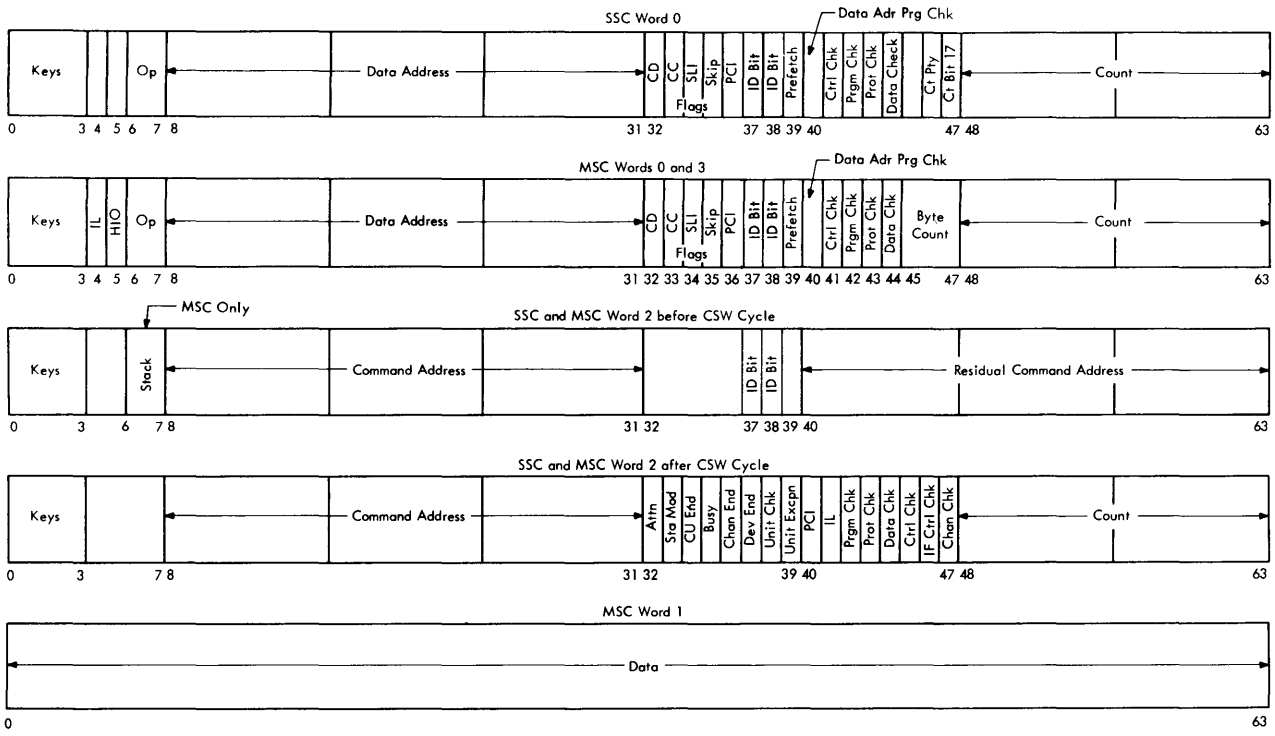


Figure 1-5. Local Storage Words

CPU Identity (Bits 37, 38): When the 2870 is used in a multiple processor system, bits 37 and 38 identify which processor in the system is operating with this device. For every data transfer, bits 37 and 38 are sent, with the data address and protection key, to the channel controller. These bits are used by the channel controller to identify which CPU the data belongs to. The bit code is:

Bit 37	Bit 38	
0	0	Processor 1
0	1	Processor 2
1	0	Processor 3
1	1	Processor 4

If the 2870 is not used in a multiprocessor system, these bits are ignored.

Machine Status (Bits 39-43): These bits define the 2870 status as follows:

Bit 39 (Prefetch) -- indicates that main channel detected a count of less than eight during a write CDA operation and prefetched the next CCW. The prefetch bit identifies this UCW 0 as the one formed from the prefetched CCW. This bit is reset when the first data transfer under the new CCW occurs.

Bit 40 (Data Address Program Check) -- this bit is only set on an output operation if the 2870 attempts to fetch data from an invalid main storage location. If the subchannel attempts to use the data, bit 42 (program check) is set and bit 40 is reset.

Bit 41 (Control Check) -- indicates that main channel detected a control error while working with this device.

Bit 42 (Program Check) -- indicates that main channel detected a program error.

Bit 43 (Protection Check) -- indicates that main channel attempted to address main storage and the storage protect keys did not match.

Bit 44 (Data Check) -- indicates that a parity error occurred in a data byte. The error could be detected by main storage or when the channel gates the data to main storage.

Count (Bits 46-63): For SSC operations, the count field is formed by adding the DAB (bits 29-31 of the CCW data address field) to the CCW count (bits 48-63). The resulting count field is defined as follows:

Bit 46 (Count Overflow Parity) -- this bit is set to maintain correct parity in byte 5 if the count overflow bit (47) is set.

Bit 47 (Count Overflow) -- this bit is set if an adder overflow (out of bit 48) occurs when the DAB is added to the count.

Bits 48-63 (Count) -- these bits are the result of adding the CCW DAB (bits 29-31) and count. For a read backward operation, the DAB is complemented before the addition. This field is decremented by eight for each doubleword of data transferred across the interface. When the SSC loads the A and B registers before beginning a write operation, this count field is not decremented. During a write operation, when the count becomes less than 16, the SSC maintains the count and this field is ignored.

SSC UCW 2

UCW 2 has two functions:

1. From the CAW fetch during start I/O until the CSW is assembled, UCW 2 contains CAW information.
2. When the operation initiated by start I/O is completed, or stopped because of an error, a CSW is formed from channel and device status and stored in UCW 2 until the 2870 can obtain main storage priority.

UCW 2 Before CSW Cycle: UCW 2 is divided into these fields (Figure 1-5):

Key Field (Bits 0-3) -- this is the storage protect key from the CAW. The key is sent to main storage for CCW fetches when a chain of CCWs is executed.

Command Address (Bits 8-31) -- this field contains the address of the next CCW to be fetched by the channel. The next CCW address is formed by incrementing the address of the present CCW by +8. This field is normally used for the command address field of a CSW.

CPU Identity (Bits 37, 38) -- these bits are the same as the ID bits described for UCW 0. For each CCW fetch, these bits are sent to the channel controller with the command address and key.

Residual Command Address (Bits 40-63) -- when a CCW has been fetched for a CDA operation (trigger 2), this field holds the address of the last CCW executed. The UCW 2 formed during either start I/O or chain command (pseudo start I/O) ignores this field. If a CCW is fetched for a CDA operation and an error occurs before the new CCW is used, this field provides the command address field for the resulting CSW.

UCW 2 is formed from the CAW by gating the storage protect key to bits 0-3 of the control register, and incrementing the command address field of the CAW by +8 and gating the result to bits 8-31 of the control register. If the operation is chained, UCW 2 is updated each time a new CCW is fetched.

To update UCW 2, the command address is gated through the adder to the residual command address field (bits 40-63); then the command address is incremented by +8 and the result is gated to the command address field (bits 8-31). Therefore, each UCW 2 after the first has both a command address field and a residual command address field.

SSC UCW 2 After CSW Cycle: UCW 2 after a CSW cycle contains the CSW stored in main storage. To form a CSW, parts of UCW 0 and UCW 2 are combined with the status sent by the control unit and the SSC. The status byte from the control unit is placed in byte 4, unaltered. Channel status is developed by main channel or the SSC as follows:

1. Program check, protection check, or program controlled interrupt are developed by the main channel.
2. Incorrect length, interface control check, or chaining check are developed by the SSC.
3. Data check and control check can be developed by either the SSC or main channel.

MSC UCW's

- MSC devices use all four UCWs to hold subchannel information.
- UCW 0 and UCW 3 hold CCW information.
- UCW 1 is the device's data buffer.
- UCW 2 holds either CAW or CSW information.
- If a logout occurs, three log words and a CSW replace the UCWs.

Because the multiplex subchannels share main channel controls and registers, their subchannel control information and data are stored in local storage until needed. To store both the control information and the data for a multiplex subchannel, four UCWs are required. UCW 0 and UCW 3 hold CCW information, UCW 1 is the subchannel's data buffer, and UCW 2 contains either CAW or CSW information.

If a logout occurs, three log words and a CSW are formed and stored in the device's UCWs. These log words describe the error that occurred and the operation that the channel was performing. This logout information is also transferred to main storage if the log-on-machine-check switch is on and the

channel is in auto mode. The log words can be manually read out and displayed in the control register. The logout sequence is described in the logout section.

MSC UCW 0

UCW 0 holds CCW information for either the last operation performed or the current operation. Each time a CCW is fetched for a device, a new UCW 0 is formed by the main channel. Because the main channel performs most of the functions of the multiplex subchannel operation, UCW 0 is read out of local storage to the control register each time the device requests service (for data or status information). UCW 0 is shown in Figure 1-5, and its fields are defined as follows:

Key Field (Bits 0-3): The key field contains the storage protect key obtained from the CAW. The key field is placed in the key register and sent to main storage with the data address for each main storage fetch or store operation.

Incorrect Length (Bit 4): This bit indicates that the block of data transferred did not match the count supplied by the CCW. This bit is set if:

1. The control unit presents ending status before the count is exhausted.
2. The control unit requests an extra data cycle after the count is exhausted.

Halt I/O (Bit 5): This bit indicates that the MSC attempted to select this device and issue a halt I/O command, but the control unit returned a control unit busy indication and prevented the halt. If the control unit requests a data cycle and this bit is on, the control unit receives a stop command (raise address out and select out and then drop select out).

Operation (Bits 6, 7): These bits are formed by encoding the command field of the CCW. Main channel uses these bits to determine whether an MSC data cycle is an input or output operation. If CPU issues a start I/O or test I/O instruction, these bits are examined to determine whether the device is busy. When an operation (or chain of operations) is completed, these bits are reset.

The bits mean:

Bit 6	Bit 7	
0	0	Idle Device
0	1	Write or Control
1	0	Read or Sense
1	1	Read Backward

Data Address (Bits 8-31): This field contains the address to be used for the next main storage data fetch or store. When data is transferred, this field is incremented by +8 for read or write, or decremented by -8 for read backward operations.

For a read backward operation, bits 29-31 are complemented when UCW 0 is formed. For either read forward or backward operation, bits 29-31 are gated to the marks encoder for the first main storage data transfer. After the first main storage data transfer, bits 29-31 are reset.

Flags (Bits 32-36): The flag bits are taken from the CCW and serve these functions:

Bit 32 (Chain Data) -- causes main channel to fetch the next CCW when the current count is exhausted. The command from the old CCW is retained and the device is not reselected.

Bit 33 (Chain Command) -- causes main channel to fetch the next CCW when the current count is exhausted. The device is reselected by using the command from the new CCW.

Bit 34 (Suppress Length Indication) -- causes main channel to ignore bit 4 of UCW 0 on an ending sequence.

Bit 35 (Skip) -- causes main channel to suppress the transfer of data to main storage on a read, read backward, or sense operation.

Bit 36 (Program Controlled Interrupt) -- causes main channel to request CPU for an interrupt. When interrupt response is granted, a CSW is formed and stored at main storage location 64 without altering the normal operation of the device.

CPU Identity (Bits 37, 38): When the 2870 is used in a multiple processor system, bits 37 and 38 identify which processor in the system is operating with this device. On every main storage data transfer, bits 37 and 38 are sent to the channel controller with the data address and protection key. These bits are used by the channel controller to identify which CPU the data applies to.

The bit code is:

Bit 37	Bit 38	
0	0	Processor 1
0	1	Processor 2
1	0	Processor 3
1	1	Processor 4

If the 2870 is not used in a multiprocessor system, these bits are ignored.

Machine Status (Bits 39-44): These bits define 2870 status as follows:

Bit 39 (Prefetch) -- indicates that main channel has prefetched a new CCW and placed it in UCW 3. This only occurs on a MSC write CDA operation.

Bit 40 (Data Address Program Check) -- indicates that main channel attempted to fetch data from a main storage address that did not exist on this system. This bit can only be set during an output (write or control) operation. If the MSC attempts to send the data to the device, bit 42 (program check) is set and bit 40 is reset.

Bit 41 (Control Check) -- indicates that main channel detected a control error while operating with this device.

Bit 42 (Program Check) -- indicates that main channel detected a program error.

Bit 43 (Protection Check) -- indicates that main channel attempted a main storage cycle but the storage keys did not match.

Bit 44 (Data Check) -- indicates that a parity error occurred in a data byte. For an input operation, this can be detected by main storage, the main channel storage bus in OR, or the I/O interface. For output operations, the error can only occur at the I/O interface.

Byte Count (Bits 45-47): The byte count field holds the three-position count that is used to control data register gating for input or output operations. This field is initially loaded from the DAB (bits 29-31) and is stepped one for each byte transferred. For a read backward operation, the byte count field is loaded with the complement of the DAB.

Count Field (Bits 48-63): This field holds the count for the current operation. For each byte of data transferred, this count is decremented by one byte for each transfer.

MSC UCW 1

For MSC devices, UCW 1 provides each device with a doubleword data buffer. On a write operation, main channel fetches a doubleword of data and places it in UCW 1. Each time the device requests a byte of data, UCW 1 is read out of local storage to the data register, a single byte of data is gated to the I/O interface, and UCW 1 is stored again. When UCW 1 is exhausted, another doubleword of data is fetched from main storage, and UCW 1 is loaded with the new data.

For a read operation, UCW 1 is read out into the data register, a byte of data is gated into the data register, and UCW 1 is stored in local storage. This occurs on each data byte transfer with each byte being set in the next position over until the doubleword is filled. When the last byte is gated into the data register, a main storage cycle stores the data in main storage, and UCW 1 is stored back into local storage (without being reset). Because UCW 1 is not reset when data is transferred to main storage, data from the last doubleword assembled remains in UCW 1 until replaced by the new data bytes. Therefore, if UCW 1 is displayed before a doubleword is completely assembled, both old and new data will appear.

MSC UCW 2

As in the SSCs UCW 2, a MSC UCW 2 holds either CAW information or a CSW (Figure 1-5). If an I/O operation consists of a chain of CCW's, UCW 2 holds the command address and key for both the current and the next CCW. These addresses are updated each time a CCW is fetched from main storage. When an operation is terminated, UCW 0 and UCW 2 are combined with control unit and channel status to form a CSW which then replaces UCW 2s CAW information.

MSC UCW 2 Before CSW: Before a CSW cycle occurs, UCW 2 has these fields:

Key Field (Bits 0-3) -- this is the storage protection key obtained from the CAW during the start I/O instruction. This key is sent to main storage each time a CCW fetch is required.

Stack (Bit 7) -- this bit is set if status information is stacked in the device.

Command Address (Bits 8-31) -- this field contains the address of the next CCW to be fetched for a chained operation. The next CCW address is formed by incrementing the address of the present CCW by +8. This field is normally used for the command address field of a CSW.

CPU Identity (Bits 37, 38) -- these bits are the same as the identity bits described for UCW 0. On each CCW fetch these bits are sent to the channel controller with the command address and storage protection key.

Residual Command Address (Bits 40-63) -- when a CCW has been fetched for a CDA operation (trigger 2), this field holds the address of the last CCW executed. The UCW 2 formed during either start I/O or chain command (pseudo start I/O) ignores this field. If a CCW is fetched for a CDA operation and an error occurs before the new CCW is used, this field provides the command address field for the resulting CSW.

MSC UCW 2 After CSW: At the termination of an I/O operation, main channel assembles a CSW and stores it in UCW 2. The CSW is formed from device status, channel status, UCW 0, and UCW 2. The status byte from the control unit is placed in

byte 4, unaltered. Channel status is taken from UCW 0 or main channel and placed in byte 5. The command address and protection key fields are taken from UCW 2. The remaining count from UCW 0 (bytes 6 and 7) is placed in bytes 6 and 7 of the CSW. The address of the device is placed in the interrupt queue register, the CSW is stored in UCW 2, and a CPU interrupt request is made. When CPU interrupt response rises, or a test I/O instruction is issued to this device, the CSW is sent to main storage location 64.

MSC UCW 3

UCW 3 holds a prefetched UCW for a write CDA operation (Figure 1-5). When the main channel detects a count between 2 and 7 and chaining is indicated, the next CCW is fetched, modified to UCW 0 format, and stored in UCW 3. UCW 3 is transferred to UCW 0 when the last data byte is transferred for the current CCW.

INSTRUCTIONS

- The 2870 recognizes four instructions from CPU: start I/O, halt I/O, test I/O, and test channel.
- Each instruction, except test channel, is accompanied by a device address.
- Once the channel determines whether the operation can be performed, CPU is released with a condition code that indicates the result of the instruction.
- Each I/O instruction termination causes one CSW and a condition code to be sent to CPU.

The 2870 recognizes only four instructions from the CPU: start I/O, test I/O, halt I/O, and test channel. Within the CPU, each instruction contains an address which identifies the channel and, except for test channel, the attached device. CPU uses the channel address to activate the select channel line to the desired channel. Therefore, the channel receives: the select channel, the instruction, and (except for test channel) the address of the device the instruction applies to. In the 2870 the device address identifies both the device and the subchannel involved.

Start I/O

A start I/O instruction to an available subchannel causes the selection of the associated device and, when possible, the initiation of a channel command. The channel commands associated with start I/O are: read, read backward, write, sense, and control. Acceptance or rejection of the initial command causes the channel to send the proper condition code and release the CPU.

To initiate a start I/O instruction at the channel, the CPU activates the start I/O line, places the eight-bit unit address on the unit address bus out (UABO), and raises the select channel line (FC101). If the subchannel is busy or unavailable, the 2870 sends condition code 10 or 11, respectively, and releases the CPU. When the subchannel is available, the 2870 gates the unit address to the unit address register and fetches the channel address word (CAW) from main storage location 72.

The CAW contains the command address and the storage protection key, which are gated to the control register. If errors are discovered in the CAW or unit address, status bytes are stored, condition code 01 is sent (FC601), and the CPU is released. If there are no errors, two operations are now started. The first involves fetching the channel command word (CCW); this is accomplished by initiating a storage request (FC551). When the BCU response is received, the channel places the command address on the storage address bus (SAB) and waits for the BCU advance pulse. This pulse sets the command information (command code, data address, flags, and count) in the proper registers. The CCW in channel trigger is turned on at this time to indicate that the command has been received; the information is checked for parity, proper field, etc. During the storage operation, the command address is incremented by eight bytes (FC105). This updated quantity is stored in unit control word 2 in local storage.

The second operation is the selection of the device specified by the unit address. This is accomplished by placing the unit address on the bus out and issuing address out, followed 250 nanoseconds later by select out. The control unit should recognize its address and respond with operational in, which in turn causes the channel to drop address out. When the control unit recognizes the fall of address out, it places the address of the device selected on the bus in and raises its address in line (FC803); at this time, a multiplex subchannel drops select out. (Selector subchannels do not drop select out because they operate with the device in burst mode.) To ensure proper selection, the channel compares the address it receives with the one it issued. An improper selection results in an interface control check, and the device is reset.

With a proper compare of the address and no

errors, the operation proceeds. The command code is placed on the bus out line (FC805), and the command out line is raised. If the control unit responds with zero status and accepts the command, the channel sends condition code 00 and releases the CPU. The channel and device are ready to proceed with the command received in the CCW.

If errors occurred, a test I/O code is placed on the bus out line instead of the command code, thus relieving the device of its status. The channel disconnects from the device and, at the same time, requests a storage cycle. When the BCU response is received, the status information is placed in the channel status word (CSW), condition code 01 is sent, and the CPU is released. The subchannel is available and ready to receive another instruction.

This same error procedure would have followed if the control unit had responded to command out with anything except zero status. The storage key, command address, and count portions of the CSW are not stored.

Resulting Condition Code:

00 The addressed subchannel and I/O device are operational and are not engaged in the execution of any previously initiated operations. There are no conditions stacked for interruption and no programming or equipment errors were discovered during the execution of the I/O instruction. This code indicates that the device has, in fact, accepted and started executing the command as issued.

01 This code indicates that the instruction either was not accepted or was completed and that the status bytes have been stored in the CSW. This code can be caused by equipment or programming errors or by a response of other than zero status to an initial command.

10 This code indicates that the addressed subchannel is already actively engaged in the execution of a previously initiated instruction. It is also the response of a subchannel whose channel and interruption has not been accepted.

11 This code indicates that a selector subchannel is not available to receive the issued instruction, or a control unit may be unavailable because it is not furnished, has been disconnected, or is in manual mode. The same applies to devices. An unavailable channel, one not furnished to the system, is detected by the CPU.

Test I/O

The test I/O instruction may be used to clear interruption conditions that exist in the addressed channel or its associated I/O devices. This instruction may cause a CSW to be placed in location 64 and the interruption conditions to be cleared. To initiate a test I/O instruction at the channel, the CPU activates the test I/O line, places the eight-bit unit address on the UABO line, and signals the channel with the select channel line. If the channel has an outstanding interruption, it compares the received unit address with the pending unit address. If the addresses are equal, the interruption conditions in the channel are stored in location 64 and the CPU is released. If the addresses are not equal and the subchannel is not busy, the channel retains the unit address received from the CPU and selects the specified device as in start I/O; but the command code is the test I/O code which requests only status from the device. When status is received, the CSW is stored and condition code 01 is sent to the CPU prior to release. If zero status is sent in response to the I/O command, condition code 00 (for available) is sent to the CPU and a release is accomplished. Thus, test I/O causes a CSW to be stored whenever the tested device has conditions for interruption either within the channel or stacked in the device. The CSW is also stored when the channel or I/O device detects an error during the execution of the test I/O instruction. The status bits in the CSW identify the error condition. The CSW that is provided by the test I/O instruction has the same format as that provided by I/O interruptions and is stored at location 64. The contents of the CSW always pertain to the device to which the instruction is addressed.

Resulting Condition Codes:

00 Both the subchannel and the device were available to accept start I/O.

01 The CSW is stored. The interruption condition indicated in the CSW is cleared in the I/O device and the channel. The presence of unit check, channel control check, and the interface control check bits in the absence of channel end or device end is caused by a condition created during the preceding operation or by an equipment error detected during the execution of test I/O. A busy bit indicates a busy device if it appears alone, or it indicates a busy control unit if the status modifier is also present.

10 The busy code indicates that no action has been taken by the channel because the subchannel is executing a previously initiated command or its associated interface is in burst mode.

11 Same as start I/O.

Halt I/O

The halt I/O instruction is initiated by the CPU by activating the halt I/O line, placing the eight-bit unit address on the UABO, and signaling the channel with the select channel line. If the halt I/O instruction is issued to a multiplex subchannel or

an SSC that has an end interrupt outstanding, the channel releases the CPU with condition code 00.

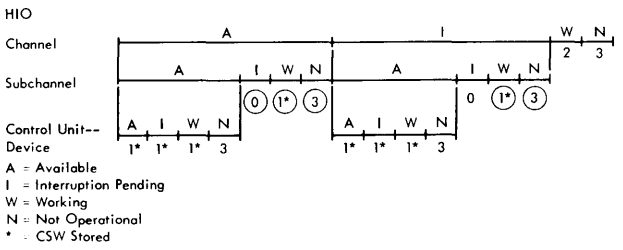
When halt I/O is issued to a working SSC, the SSC raises the address out line and drops its select out line. The control unit that is operating on the I/O interface responds by dropping all in tag lines to the channel, thus the control unit immediately disconnects from the channel. The SSC turns on its interrupt request trigger, sends condition code 10, and releases the CPU. The SSC now has an outstanding interruption that may be cleared by being enabled or by receiving a test I/O with the proper unit address.

When halt I/O is issued to a multiplex subchannel operating in burst mode, the sequence is the same as for a selector subchannel except that the interrupt request to the CPU is not made until the status of the halted device is accepted by the subchannel.

When the subchannel is available, halt I/O causes the addressed device to be selected. If the device responds with a signal on the operational in line, the interface-disconnect sequence is performed, the 16 status bits of the CSW are replaced by 0s, and condition code 01 is set. If the device responds with the control-unit-busy sequence, the status provided by the device is placed in the CSW with 0s for channel status and condition 01 is set. If select in rises in response to the selection by the channel, condition code 11 is set.

The effect of the execution of halt I/O depends on the type of device. The interface-disconnect sequence has no effect on devices that are not in the working state or are executing an operation of a fixed duration such as rewinding tape or feeding a card. If the device is executing a type of operation that is variable in duration, the device interprets the interface-disconnect as a signal to terminate the operation. The nature of termination depends on the device.

The condition code set by halt I/O for all possible states of the I/O system is shown graphically in Figure 1-6.



NOTE: Encircled condition codes pertain to conditions that occur only on the 2870 Multiplexer Channel.

Figure 1-6. Condition Code Set by Halt I/O

Test Channel

The test channel instruction is initiated when the CPU raises the test channel multiplex line and signals the proper channel on the select channel line. This instruction does not require the eight-bit unit address. Its only function is to cause the channel to send a condition code that describes the present state of the channel, at which time the CPU is released.

Resulting Condition Code:

00 The channel has an interface available. Either one SSC is not busy or the MSC is not in burst mode.

01 The channel contains an interruption that it would immediately transfer to storage if enabled by the CPU.

10 All available I/O Interfaces are operating in burst mode.

11 Channel not operational.

EXECUTION OF INPUT/OUTPUT OPERATIONS

- The 2870 can execute six commands.
- The channel address word (CAW) specifies the key and address of the first channel command word.
- The channel command word (CCW) provides the I/O command and the data address.
- The channel status word (CSW) provides information about the termination of an I/O operation.

The 2870 can execute six commands: write, read, read backward, control, sense, and transfer in channel. Each command except transfer in channel initiates a corresponding I/O operation. The term "I/O operation" refers to the activity initiated by a command in the I/O device or channel. The subchannel is involved with the execution of the operation from the initiation of the command until the CSW is stored.

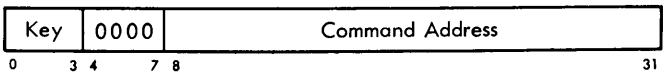
An operation may involve the transmission of data to a contiguous storage area defined by a single CCW or to a number of disjointed storage areas. In the latter case, a chain of CCWs is used and the storage areas are coupled by means of data address chaining.

Alternatively, a chain of CCWs can apply to a number of different operations. The first CCW associated with an operation specifies the operation to be performed, while the last CCW specifies

whether another operation follows. Operations are executed in the order specified in the chain of CCWs.

Channel Address Word

The channel address word (CAW) specifies the storage protection key and the address of the first CCW associated with a start I/O instruction. The CAW is fetched from storage location 72. The channel refers to the CAW only during the execution of start I/O. The CAW information is thereafter stored in the subchannel, and the program is free to change the contents of location 72. The CAW has the following format:



The fields in the CAW are allocated for the following purposes:

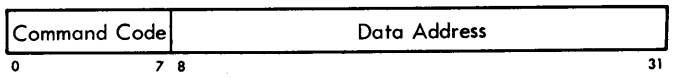
Protection Key: Bit positions 0-3 specify the storage protection key for all commands associated with start I/O.

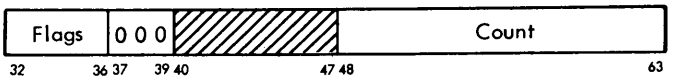
Command Address: Bit positions 8-31 specify the location of the first CCW in main storage. The three low-order bits of the command address must be 0 to specify the CCW on integral boundaries for doublewords.

Bit positions 4-7 of the CAW must contain 0's. If any of these restrictions is violated or if the command address specifies an invalid storage location, the start I/O instruction causes the status bits of the CSW to be stored with the program check bit on. The I/O operation is not initiated.

Channel Command Word

The channel command word (CCW) specifies the command to be executed, the storage area, if any, associated with the command, and the action to be taken on completion of the command. CCWs can be located anywhere in main storage. The channel fetches a CCW from main storage only once; then the pertinent information is stored in the subchannel. The first CCW is fetched during the execution of start I/O. Additional CCWs in the chain are obtained when the operation has progressed to the point where each CCW is needed. The CCW has the following format:





The fields in the CCW are allocated for the following purposes:

Command Code: Bit positions 0-7 specify the operation to be performed.

Data Address: Bit positions 8-31 specify the location of an eight-bit byte in main storage. It is the first data location referred to in the area defined by the CCW.

Chain Data (CD) Address Flag: Bit position 32 specifies chaining of data addresses. It causes the storage area defined by the next CCW to be used with the current operation.

Chain Command (CC) Flag: Bit position 33, when the CD flag is off, specifies chaining of commands. It causes the command specified by the next CCW to be initiated on normal completion of the current operation.

Suppress Length Indication (SLI) Flag: Bit position 34 controls whether an incorrect length condition is indicated to the program. When this bit is 1 and the CD flag is off in the CCW, the incorrect length indication is suppressed. When the CC and SLI flags are on, and no interrupt conditions are present, command chaining occurs regardless of the presence of an incorrect length indication. Incorrect length indications are ignored for command immediate operations.

Skip Flag: Bit position 35 suppresses the transfer of information to storage during a read, read backward, or sense operation.

Program Controlled Interruption (PCI) Flag: Bit position 36 causes an enabled channel to interrupt the program as soon as possible after fetching the CCW.

Count: Bit positions 48-63 specify the number of eight-bit storage locations in the area defined by the CCW.

Bit positions 37-39 of every CCW, other than one that specifies transfer in channel, must contain 0s. Violation of this restriction causes a program check. When the first CCW specified by the CAW does not contain the required 0s, the I/O operation is not initiated and the status portion of the CSW is stored during the start I/O instruction. Detection of this condition during data address chaining causes the I/O device to be signaled to terminate the operation. When the absence of these 0s is detected during command chaining, the new operation is not initiated and an interruption condition is generated in the channel.

Command Code

- The command code specifies the operation to be performed.
- The modifier bits determine how a command is to be executed.

The command code in the CCW specifies to the channel and I/O device the operation to be performed. The two low-order bits, or when these two bits are 00, the four low-order bits of the command code identify the operation to the channel. The channel distinguishes between four operations:

Output Forward (write and control)
Input Forward (read and sense)
Input Backward (read backward)
Branching (transfer in channel)

Whenever the channel detects an invalid code during the initiation of a command, program check is generated. When the first CCW specified by the CAW contains an invalid command code, the status portion of the CSW is stored during the execution of start I/O. If the invalid code is detected during command chaining, the new operation is not initiated and an interruption condition is generated. The command code is ignored during data address chaining.

The channel ignores the high-order bits of the command code after checking the byte for correct parity.

Commands that initiate I/O operations (write, read, read backward, control, and sense) cause all eight bits of the command code to be transmitted to the I/O device.

Definition of Storage Area

- The CCW defines the storage area.
- The channel can prefetch CCWs.

The main storage area associated with an I/O operation is defined by CCWs. A CCW defines a contiguous area by specifying the address of the first byte in the data address field of the CCW. The number of bytes contained in the storage area is specified in the count field of the CCW.

When the 2870 refers to a location not provided in the system, program check is generated. Attempts to transmit data to or from a nonexistent storage location on the detection of an invalid CCW address during data address chaining are indicated to the program with the interruption condition at the end of the operation. The I/O device is signaled to terminate the operation on detection of this condition. When an invalid address is detected during command chaining, the new operation is not initiated and an interruption condition is generated.

The count field in the CCW can specify any number up to 65,535. Whenever the count field in a CCW (other than one specifying transfer in channel) initially contains a count of 0, the program check condition is generated. When this occurs in the first CCW specified by the CAW, the operation is not initiated and the status portion of the CSW is stored during the execution of start I/O. When a count of 0 is detected during data address chaining, the I/O device is signaled to terminate the operation. Detection of a count of 0 during command chaining results in a program check that suppresses the initiation of the new operation and generates an interruption condition.

The channel may, during an output operation, fetch data and CCWs from main storage areas before the information is needed in the I/O operation. When the I/O operation uses data and CCWs from a location near the end of the available storage, such prefetching may cause the channel to refer to locations that do not exist. Similarly, the channel may detect a count of 0 in a prefetched CCW. Any programming errors detected during prefetching of data or CCWs do not cause error indications until the I/O operation attempts to use the information. If the I/O device or the channel terminates the operation before the invalid information is needed, the condition is not brought to the attention of the program.

Chaining

- Commands are coupled into a channel program by chaining.
- Data addresses or commands can be chained.

- Data chaining permits the reorganization of information as it is transferred between main storage and an I/O device.

When the 2870 has performed the transfer of the information specified by a CCW, it can continue the activity initiated by the start I/O instruction by fetching a new CCW. The fetching of a new CCW on exhaustion of the preceding one is called chaining, and the CCWs belonging to such a sequence are said to be chained.

Chaining normally takes place only between CCWs located in successive doubleword locations in storage. It proceeds in an ascending order of addresses. Two chains of CCW's located in noncontiguous storage areas can be coupled for the purpose of chaining by means of the transfer in channel command. All CCWs in a chain apply to the I/O device specified in the original start I/O instruction.

Two types of chaining are: chaining of data addresses and chaining of commands. Chaining is controlled by the chain data (CD) address and the chain command (CC) flags in the CCW. These flags specify the action to be taken by the channel on exhaustion of the current CCW. The setting of the CD and CC flags is propagated through the transfer in channel command. When the transfer in channel command is received by the channel, it is handled as a free command and causes the action specified in the last command to be stored in the storage location specified by the transfer in channel command. If the CD flag is on, the CC flag is ignored.

Data Address Chaining

Data address chaining permits different parts of the same record to be stored in or fetched from noncontiguous areas in storage. The channel interprets the CD flag as a signal to fetch a new CCW for its count, data address, and flags. The operation code field in the new CCW is ignored.

Command Chaining

The command chain (CC) flag with the CD flag off gives the programmer the option of initiating multiple I/O operations with a single CPU start I/O instruction. When the count of a particular CCW is exhausted and the CC flag is on, the channel fetches the next sequential CCW. This new CCW may specify either a transfer in channel command or a new I/O operation.

Command chaining takes place and the new operation is initiated only if no unusual conditions are detected in the present operation. If a data check, incorrect length, or exceptional condition has occurred, the sequence of CCWs is terminated and an I/O interrupt is generated. The new CCW is not fetched and the CC flag is ignored. An incorrect length condition does not suppress command chaining if the CCW had both the CC and SLI flags on. An exception to sequential chaining of CCWs occurs when the I/O device presents the status modifier bit with the device end bit. The combination of status modifier and device end with the CC flag causes the 2870 to fetch and chain to the CCW whose main storage address is 16 bytes higher than the present CCW. Therefore, the status modifier condition can cause the channel to skip one complete CCW when chaining.

Command chaining permits a single I/O instruction to specify auxiliary function such as rewinding tape at the end of data transmission. Command chaining, in conjunction with the status modifier condition, permits the channel to modify the normal sequence of operations in response to signals provided by the I/O device.

Skipping

- Skipping applies only to read, read backward, and sense operations.

- No information is placed in main storage during a skip operation.

Skipping is the suppression of main storage references during an I/O operation. It is defined only for read, read backward, and sense operations, and is controlled by the skip flag which is specified individually for each CCW. When the skip flag is on, skipping occurs.

Skipping affects only the handling of information by the channel. The operation at the I/O device proceeds normally and information is transmitted to the channel. The channel keeps updating the count but does not place the information in main storage. If the CC or CD flag is on, a new CCW is obtained when the count reaches 0. Placing information in main storage is resumed if the skip flag bit in the new CCW is off.

No checking for invalid or protected data addresses takes place during the skip operation. Normal checking for programming and equipment errors occurs. Any invalid or unusual condition that generates the corresponding condition for I/O interruption, or when discovered during the initiation of the first command, causes the status portion of the CSW to be stored during the execution of the start I/O instruction.

Skipping, when combined with data address chaining, permits the program to place selected portions of a record in main storage.

Program Controlled Interruption

- An I/O interruption can be program controlled.
- A program controlled interrupt does not affect I/O operations.

The program controlled interruption (PCI) function permits the program to cause an I/O interruption during the execution of an I/O operation. It is controlled by the PCI flag in the CCW. The flag can be in the first CCW specified by the start I/O instruction or one that is fetched during chaining. Whenever the PCI flag in the CCW is on, the 2870 attempts to interrupt the program as soon as possible after starting data transmission. Neither the PCI flag nor the associated interruption affects the execution of the current I/O operation. However, if the 2870 has an outstanding subchannel interruption in its interrupt queue register, the PCI is not attempted until that interruption is cleared.

A CSW containing the PCI bit reflects the progress of the operation at the time the CSW is stored. The CSW may be stored by an interruption while the operation is in progress; or if the interruption is not allowed, it is stored on termination of the operation with normal ending conditions.

When the PCI bit causes an interruption before the operation is completed, the end bit in the CSW is off. If the 2870 has detected data errors in the operation at this point, the channel data check bit is on although the condition in the channel is not reset and is indicated again at the end of the operation. The CCW address in the CSW identifies the location of the next CCW. The count is unpredictable. Presence of the channel end bit with the PCI bit indicates that the operation terminated. The CSW, in this case, has its regular format with the PCI bit added.

If chaining occurs before the PCI interruption has occurred, the PCI condition is carried over to the new CCW. This occurs both on data address and command chaining, and in either case, the condition is propagated through the transfer in channel command. PCI is not stacked; that is, if another CCW is fetched with the PCI flag on before the interruption for a previous PCI flag has occurred, only one interruption takes place.

The PCI flag is inspected in every CCW, except those that specify a transfer in channel command. In a CCW specifying transfer in channel, all flags are ignored. The PCI flag is ignored during all initial program load (IPL) operations. Program controlled interrupt alerts the program of the progress of an I/O operation.

Commands

- Commands are specified in the CCW and are decoded by the channel.
- Basic I/O operations are reading and writing.
- A variation of the basic read operation is the read backward command.

The 2870 can be programmed to handle the following commands: write, read, read backward, control, sense, and transfer in channel.

Write

The write command initiates the execution of a write operation at the I/O device. It causes data to be transferred from main storage to the I/O device. Data in storage is fetched in an ascending order of addresses, starting with the address specified in the CCW. A CCW used in a write operation is inspected for the CC, CD, SLI, and PCI flags. The setting of the skip flag is ignored.

Read

The read command initiates the execution of a read operation at the I/O device. It causes data to be transferred from the I/O device to main storage. Data is placed in main storage in an ascending order of addresses, starting with the address specified in the CCW. A CCW used in a read operation is inspected for all of the five flags (CD, CC, SLI, skip, and PCI).

Read Backward

The read backward command initiates a read backward operation at the I/O device. It is defined only for certain magnetic tape devices and causes a read operation to be performed with the tape moving backwards. The bytes of data within a record are sent to the channel in a sequence opposite to that of writing. They are placed in storage in a descending order of addresses, starting with the address specified in the CCW. The bits within an eight-bit byte are in the same order as those sent to the device on writing. A CCW used in a read backward operation is inspected for all of the five flags (CD, CC, SLI, skip and PCI).

Control

The control command is handled in the 2870 in the same manner as a write command. It is only at the device or control unit that a difference is detected. The operations that can be initiated by a control command depend on the particular type of I/O device. These operations, as well as their codes, are specified in the functional description of the devices.

A CCW specifying a control command cannot contain a count of 0. If the I/O device does not need additional information for the operation and signals device end during the command cycle, any control information specified by the CCW is not transferred to the I/O device and no incorrect length indication is generated. If the control function requires information other than the command code, the data address field of the CCW designates the location of the additional information. A CCW used in a control operation is inspected for the CD, CC, SLI, and PCI flags. The setting of the skip flag is ignored.

The action of the flags for a control immediate follows: The SLI flag is ignored and is always assumed to be present. The CD flag always causes termination of the operation whether or not the CC flag is present.

Sense

The sense command initiates a sense operation at the I/O device. It causes sense status information to be transferred from the I/O device to main storage. The information is placed in storage in an ascending order of addresses, starting with the address specified in the CCW. The sense command provides detailed information concerning the status of the I/O device. It may, for example, specify whether the tape in a magnetic tape drive is loaded or the stacker in a card reader is full. It also provides information concerning any unusual conditions that have occurred in a preceding operation. The status information provided by the sense operation is more detailed than that supplied by the unit status byte in the CSW. The amount and meaning of the status information are peculiar to the type of I/O device and are specified in the functional description of the device. A CCW used in a sense operation is inspected for all of the five flags (CD, CC, SLI, skip and PCI).

Transfer in Channel

The transfer in channel (TIC) command causes the channel to fetch the next CCW from the location specified by the data address field of the transfer in channel command. The data address is incremented and placed in the command address field of unit control word 2 in local storage. The transfer in channel command provides chaining between noncontiguous CCWs. The TIC command can occur in data address and command chaining.

The TIC command cannot be the first command issued; that is, it cannot be the command addressed during the start I/O instruction. Likewise, there cannot be two TIC commands in sequence. Either of these conditions detected by the 2870 causes a program check and terminates the operation. When the TIC is discovered during the start I/O instruction, the program check condition is set in the CSW and the CPU receives a condition code 01 release. When there are two TIC commands in sequence, the operation is terminated and interruption is signaled to the CPU.

To address a CCW on doubleword bounds, a CCW that specifies a TIC command must contain 0s in bit positions 29, 30, and 31. When this restriction is violated or when an invalid address is specified, program check is generated. Detection of these errors during data address chaining causes the operation at the I/O device to be terminated.

The contents of CCW bit positions 0-3 and 32-63 are ignored for TIC commands.

TERMINATION OF I/O OPERATIONS

- An interrupt is generated at termination of an I/O device.
- The channel and I/O device make status conditions available when interrupts are cleared.
- The CSW presents status conditions to the program.

When the sequence of operations initiated by the start I/O instruction is terminated, the subchannel or the I/O device generates an interrupt. The ending conditions are brought to the attention of the program by the I/O interrupt, by the test I/O instruction, or by the start I/O instruction. The 2870 allows only one multiplex subchannel to interrupt at a time by use of the interrupt queue register. If the 2870 has an outstanding interrupt in the interrupt queue register, other multiplex devices attempting to present status are stacked in the device. When the interrupt is cleared, the channel and I/O device make available to the program status conditions that describe the results of the preceding operation. These conditions, as well as an address and a count that indicate the extent of the I/O operation sequence, are presented to the program as a CSW.

Types of Termination

When the program issues a start I/O instruction, the I/O device and channel perform certain tests during the initiation of the operation. A command can be rejected during the execution of the start I/O instruction by any of the following conditions: control unit end, device end, busy, unit check, exceptional condition, program check, channel control check, interface control check, unavailable device, and protection check.

The rejection of the instruction is indicated by the channel sending condition codes 01, 10, or 11 when it releases the CPU. Condition code 10 indicates that the addressed subchannel is busy. Condition code 11 indicates that either an addressed device did not answer the interface initial selection sequence (invalid device address or malfunction), or that the address specified an uninstalled selector subchannel. Code 01 indicates that the device presented status information and a CSW was stored either because the device had status information from a previous operation, or because the command issued during start I/O was immediately executed. In these cases, no interrupts occur, and the 2870 is not tied up after the CPU is released.

The above conditions, except for busy and device end, can also occur when an I/O operation is reinitiated as a result of command chaining. When this happens, the chain of commands is terminated and an interrupt condition is stored in the 2870 until accepted by the CPU. If the interrupt queue register is unavailable, a multiplex device is stacked.

When command chaining is specified after an immediate command and no unusual conditions have been detected during its execution, the start I/O instruction does not store the channel end status bit. Chaining suppresses the immediate channel end response from the I/O device. The subsequent commands in the chain are handled normally, and the channel end condition from the last command terminates with an interrupt.

When the I/O device accepts a command, the subchannel is set up for data transmission and is said to be busy. This lasts until one of the following conditions terminates the operation at the 2870: a channel end signal is received from the I/O device, a halt I/O instruction is issued, a machine check is detected, an interface control check is detected, or the subchannel detects the end of the operation.

Channel end causes an interrupt to be stored in the interrupt queue register or at the device. For operations that do not involve data transmission, the execution time is fixed and the I/O device normally controls the ending. The duration of data transmission operations may be variable and may be controlled either by the device or channel.

During normal execution of an operation, the 2870 signals the I/O device to terminate data transmission when one of the following conditions occur: the storage area specified for the operation is exhausted, a program check is detected, a protection check is detected, or a chaining check is detected. The termination is signaled in response to a service request from the device and causes data transmission to cease. If the device is not performing a fixed length operation, it immediately terminates the operation and generates channel end. When the termination is caused by the first of these conditions, the subchannel has transmitted all information specified by the program. This occurs when the subchannel has stepped the count, in the last CCW associated with the operation, to 0. The other three conditions are caused by errors and cause data transmission to be terminated prematurely.

The I/O device can control the duration of an operation and the timing of the channel end signal by blocking data. When blocks are defined for the operation, the device always proceeds to the end of the block before providing the channel end signal, regardless of whether the device has been signaled to terminate data transmission.

When the program issues the halt I/O instruction or the 2870 detects a channel control check or interface control check, the operation at the subchannel is terminated. This termination is not dependent on the channel end signal from the I/O device. During halt I/O, the I/O device and control unit may proceed with the operation and the channel end signal subsequently indicates the termination of activity at the control unit.

I/O Interruptions

- The CPU can change state in response to channel or device conditions.
- Channel end, device end, attention, control unit end, unit check, or unit exception causes the device to initiate interrupt request.
- A program check during a chaining operation generates test I/O.
- COD-6, -9, -10.

I/O interruptions provide a means for the CPU to change its state in response to conditions that occur in I/O devices or channels. These conditions can be caused by the termination of an I/O operation or by operator intervention at the device.

The 2870 allows only one multiplex subchannel to interrupt at a time by use of the interrupt queue

register (COD-6). If the 2870 has the address of a device with an outstanding interrupt in the interrupt queue register, other multiplex subchannels attempting to present interrupt status are stacked in the device.

Requests for I/O interruptions are initiated by the 2870. The device initiates a request to the 2870 for an interrupt whenever it detects any one of the following conditions: channel end, device end, attention, control unit end, unit check, or unit exception. The channel end and device end conditions do not cause the 2870 to request an interrupt when the command chaining flag is on. Unit check and unit exception cause interruptions to be requested only when the conditions are detected during the initiation of command chaining. Once the command has been accepted by the I/O device, unit check and unit exception cannot occur in the absence of channel end, control unit end, or device end.

When the 2870 detects either the program controlled interrupt or the execution of a halt I/O instruction by a selector subchannel, it initiates a request for an I/O interrupt without having received the ending status byte from the I/O device.

When the 2870 detects a program check during the initiation of command chaining, a test I/O instruction is sent to the I/O unit. The subchannel accepts status from the I/O unit and initiates a request for an I/O interrupt. The unit status byte may or may not contain zero status; however, if the interrupt queue register is busy, the 2870 stacks the status in the device.

If a device presents secondary status (COD-9) (status presented to an idle subchannel) to the 2870 and the interrupt queue register is empty, the 2870 raises its interrupt request line to the CPU, gates the address of the device into the interrupt queue register, and stacks the status in the device. The stacked status is not retained in the 2870.

If the CPU responds with interrupt response, the channel forces a test I/O instruction (COD-10). The stacked device is selected and its present status is obtained by a test I/O instruction. The 2870 accepts this status, stores the CSW, and releases the CPU.

If the CPU responds with an instruction other than test channel, the interrupt request line is dropped and the instruction is executed. The 2870 does not remember that it had stacked the device; therefore, the device must represent its status.

Interruption Execution

- Interrupt conditions are signaled to the CPU by interrupt request.
- CSW storage is requested on acceptance of interrupt response.

An outstanding interrupt in the 2870 is signaled to the CPU by the channel activating the interrupt request line. The CPU contains both the priority and masking circuits for its multiple channels. When an interrupt request line is unmasked and the CPU determines that the interrupt has highest priority, the CPU signals the 2870 by activating its interrupt response line. When the 2870 accepts the interrupt response, it immediately initiates a storage request to store the CSW information. The 2870 then places the unit address on the UABI to the CPU and signals a release. The CPU stores the unit address and the address of the interrupting channel in its PSW and the interrupt is completed.

Channel Status Word (CSW)

- The CSW is stored at main storage location 64.
- Information about termination of an I/O operation is provided by the CSW.

The CSW provides to the program the status of an I/O device or the conditions under which an I/O operation has been terminated. The CSW is formed, or parts of it are replaced, in the process of I/O interrupts by start I/O, halt I/O, and test I/O instructions. The CSW is placed in main storage at location 64 and is available to the program at this location until the time the next I/O interrupt occurs, until it is cleared by the program, or until a start I/O, halt I/O, or test I/O instruction causes its contents to be replaced.

When the CSW is stored as a result of an I/O interrupt, the associated I/O device is identified by the unit address sent to the CPU at the time the interrupt response is released. The information placed in the CSW by the start I/O or test I/O instruction always pertains to the I/O device to which the instruction is addressed. The fields of the CSW are:

Protection Tag: Bit positions 0-3 contain the storage protection tag that was fetched when the CAW was brought into the 2870 during the last start I/O instruction.

Zeros: Bit positions 4-7 are always 0s.

Command Address: Bit positions 8-31 contain an address that is eight bytes higher than the last command address used by the 2870. Bit positions 29, 30, and 31 are 0s, making the address a double-word boundary address.

Bus In Status: Bit positions 32-39 are the status bits received from the device over the System/360 I/O interface.

Channel Status: Bit positions 40-47 contain the information generated by the 2870 to indicate the status of the preceding instruction.

Count Field: Bit positions 48-63 contain the residual count of the last CCW used by the subchannel.

Definition of Bus In Status Bits

The eight unit status bits (defined below) are received by the 2870 over the I/O bus in with the status in tag. The subchannel interprets the unit status bits received during the operation and handles them accordingly. When the bits are stored in the CSW, they are stored as they are received over the interfaces.

Attention (Bit 32)

The attention signal is generated at or by the I/O device. It is interpreted by the 2870 as an attempt by the device to interrupt the program.

An I/O device that is waiting to present the attention condition to the 2870 appears busy to a command initiated by a start I/O instruction, but it does not appear busy to commands sent to the device during chaining.

The 2870 causes the device to stack an attention condition if it has an outstanding interrupt in the interrupt queue register.

Status Modifier (Bit 33)

The status modifier bit, when received with the busy bit, is interpreted by the 2870 as a control unit busy. The status modifier, when received with device end during a command chaining operation, causes the 2870 to skip the next sequential CCW and to use the one following it to continue chaining. If command chaining is not specified when the status modifier is received with device end, the status modifier is stored in the CSW as additional information for the program. This bit may be stacked in the device.

Control Unit End (Bit 34)

The control unit end bit indicates that a control unit is available to be used by the program. This bit should come from the device only if the device has sent a control unit busy in response to a previous command. When received by the channel, an interruption is caused and the bit is stored in the CSW. This bit may be stacked in the device by the 2870.

Busy (Bit 35)

The busy bit, when accompanied by the status modifier, indicates control unit busy as discussed previously. The busy condition, alone, indicates that the I/O device cannot accept a new command because it is executing a previously initiated operation or because it contains an interrupt condition. The busy bit is off in any CSW that is formed by the test I/O instruction, unless a previously initiated I/O operation is being performed.

Channel End (Bit 36)

This condition is caused by the completion of the transmission of data or control information between the I/O device and the 2870. Channel end indicates to the program that the subchannel is available to accept another operation. Channel end may also be stacked in the device.

Device End (Bit 37)

Device end signals that an I/O device has completed its portion of an I/O operation. This bit allows the 2870 to perform command chaining when the CC flag is on. Device end may be stacked.

Unit Check (Bit 38)

This bit is sent by the device when any unusual condition is discovered. When this bit accompanies channel end or device end, it terminates the operation even if a chain flag is on. Unit check may be stacked in the device.

Unit Exception (Bit 39)

This indication is provided when the I/O device detects a condition that usually does not occur. Unit exception causes the termination of an operation. Unit exception may be stacked in the device.

Definition of Channel Status Bits

The following conditions are detected and indicated by the 2870. All of the conditions cause an interrupt condition to be set up in the 2870 and cause the subchannel to be busy until that interrupt has been recognized by the CPU.

Program Controlled Interruption (Bit 40)

This condition occurs when a subchannel fetches a CCW with the PCI flag on. The interrupt caused

by the PCI flag occurs as soon as possible after the first time the subchannel transfers data from the device to the main channel controls, but the interrupt may be delayed an unpredictable amount of time because of the masking of the channel or other activity in the system. Detection of the PCI condition in the 2870 causes the channel to request an interrupt, but it does not interfere with the progress of the I/O operation.

Incorrect Length Indication (Bit 41)

This condition occurs in the 2870 when the apparent record length on the device and the count received in the CCW do not agree, and the SLI flag is off. Presence of the incorrect length condition suppresses command chaining and causes an interrupt.

Program Check (Bit 42)

This condition is caused by programming errors that are detected in the 2870. Program check can be caused by the following:

Invalid CCW Address Specifications: The CAW or the transfer in channel command does not specify the CCW on doubleword boundaries. The three low-order bits of the CCW address are not 0.

Invalid CCW Address: The channel has attempted to fetch a CCW from an address outside the main storage of the system. This condition can be caused by an invalid address in the CAW or the transfer in channel command or by generating-on-chaining a CCW address that exceeds the available addresses in main storage.

Invalid Command Code: The command code in the CCW has four low-order 0s. The command code is not tested for validity during data address chaining.

Invalid Count: A CCW other than one specifying transfer in channel contains the value zero in bit positions 48-63.

Invalid Data Address: The channel has attempted to transmit data to or from an address that is outside the main storage of the system. An invalid data address can occur in the 2870 because the program has specified an invalid address in the CCW, or because the 2870 has stepped the address above the highest available address, or on reading backward below 0.

Invalid CAW Format: The CAW does not contain 0s in bit positions 4-7.

Invalid CCW Format: A CCW other than one specifying transfer in channel does not contain 0s in bit positions 37-39.

Invalid Sequence: The first CCW specifies transfer in channel or the 2870 has fetched two successive CCWs both of which specify transfer in channel.

Detection of any program check condition during the initiation of a command causes the operation to be suppressed. When detected after the I/O device has started, the device is signaled to terminate the operation. The program check condition is stored in bit position 42 of the CSW and may be accompanied by bus in status conditions if available to the 2870 at the time the CSW is stored.

Protection Check (Bit 43)

This bit is set when the 2870 attempts to access a portion of main storage and the protection key associated with the I/O operation does not match the key of the addressed main storage location and neither of the keys is 0. Detection of this condition causes the subchannel to signal the device to terminate the operation and the command is suppressed.

Channel Data Check (Bit 44)

This bit is set by any data parity errors detected in the 2870 or main storage. During input operations, the 2870 forces correct parity on all data placed in main storage. During output operations, the parity of data sent to the device is not changed.

Data errors cause command chaining to be suppressed but do not terminate the present operation.

Channel Control Check (Bit 45)

This bit is set by any malfunction that affects 2870 controls. This includes parity errors on a CCW fetch and data addresses and parity errors on the contents of a CCW. The conditions responsible for channel control check may cause the contents of the CSW to be invalid and conflicting.

Detection of channel control check causes the operation to terminate immediately. Under normal conditions, the 2870 causes an interrupt, which, when responded to causes three log words to be logged out. The channel control check bit is stored in the CSW in bit position 45.

Interface Control Check (Bit 46)

This condition is detected by the 2870 and usually indicates malfunctioning of an I/O device. This check results from the following:

1. The address received from an I/O device has invalid parity.

2. The status byte received from an I/O device has invalid parity.

3. An I/O device responded with an address other than the one specified by the 2870 during command initiation.

4. The addressed I/O device did not respond during command chaining.

5. A signal from an I/O device occurred at an invalid time or has invalid duration.

6. A signal from an I/O device did not occur during a predetermined time-out interval.

Detection of interface control check causes any current operation to terminate immediately.

Channel Chain Check (Bit 47)

This bit is set by a selector subchannel that is performing data address chaining during an input operation. It occurs when the I/O data rate is such that the byte boundary for the first byte cannot be predetermined. Detection of this condition causes the selector subchannel to signal the device to terminate the operation.

INITIAL PROGRAM LOADING (IPL)

- The CPU holds up the select channel line until signaled by channel release.
- Completion of IPL activates release.
- Flowchart 465.

The 2870 IPL assumes that there are switches on the CPU with which the actual channel and device are specified. These switches are set up so that the CPU raises the select channel line and holds it up until signaled by channel release. This release comes only when the 2870 has successfully completed its part of the IPL.

The IPL operation is:

1. The device unit address, from which the program is to be loaded, is set in the unit address switches on the CPU.

2. The device is properly loaded to respond to a read command from the 2870.

3. The IPL switch is depressed on the CPU and causes the following reaction from the system:

   a. The CPU and BCU are reset.

   b. The CPU latches the IPL status, decodes and selects the proper channel, and sends an IPL pulse to the channels. The CPU now waits for a channel release before proceeding.

   c. All channels perform a complete reset; that is, all devices are reset, the control units are reset, and the channels are cleared and made ready.

   d. The selected channel, after completing its reset, proceeds to read in the initial program. If the operation is completed successfully, an accept is sent to the CPU and interrupt conditions (including PCI) are suppressed. If the operation is not successful, the CPU does not receive a release signal. This requires the operator to intervene (repeat 2 and retry).

   e. The CPU, when it receives the release signal, is available to receive its PSW from address 0 and it proceeds with the operation.

The handling of the IPL read within the 2870 and the main storage locations used, are compatible with those used by other channels of System/360. The IPL sets 24 bytes of control information into main storage in the following format:

Bytes 0-7	IPL PSW
Bytes 8-15	IPL CCW 1
Bytes 16-23	IPL CCW 2

The 2870 uses the IPL pulse from CPU to perform a complete channel and device reset. The 2870 resets its own circuits and resets all control units and devices by dropping the operational out lines on all interfaces for 6 microseconds. At the completion of the reset, the 2870:

1. Gates the unit address into the unit address register.

2. Forces a count equal to 24 bytes.

3. Has a command address of 8 and a data address of 0.

4. Forces a CC flag into the flag field.

5. Forces a read operation with no modifier bits in the read command.

The addressed subchannel selects the specified device (forces burst mode for multiplex subchannels) and begins the read operation. Twenty-four bytes of data are read into main storage beginning at data address 0. Any incorrect length indications are suppressed and the 2870 chains to the command specified by CCW 1 (command address 8).

The 2870 fetches CCW 1 from bytes 8-15. CCW 1 is a read command with a chain flag, which specifies the number of bytes of data to be read in and the starting address of the field. CCW 2 is optional and is normally used for IPL from a card reader. CCW 2 has a transfer in channel command which

causes the 2870 to fetch the next CCW from the data address specified by CCW 1. This allows the card read IPL operation to read in as many cards as necessary under CCW 1 and then transfer to the new program via CCW 2.

To IPL from tape, the data is broken into two records; the first record contains the PSW and CCW 1, and the second record contains the program. CCW 2 is not necessary because the second record could fill main storage.

The 2870 continues to fetch CCWs until a CCW without a chain flag is encountered. If no errors have occurred, the 2870 suppresses the normal ending interrupt and places the channel number and device address in bytes 2 and 3 of the PSW (main storage location 0). The 2870 releases the CPU and is now ready to accept a new I/O instruction. PCI flags are ignored throughout the IPL operation. If an error occurs during the IPL, the 2870 does not issue the CPU release and the IPL must be retried.

This chapter describes the functional units of the 2870 and their use in 2870 operations.

ADDER

- The adder is used during normal channel operations to update command addresses, data addresses, and count fields.
- For SSC start I/O or chained CCW fetch operations, the adder is used to add the three low-order bits of the data address to the count.
- If an SSC operation terminates early, the adder corrects the CSW count by subtracting the SSC residual byte count from the count field of UCW 0.
- The adder increments local storage addresses for a local storage reset (clear) operation.
- The adder generates parity for its output bytes.
- Adder output is latched in the adder latches, then gated to main channel registers.

The 2870 adder has 24 positions: 21 half-adder positions and 3 full-adder positions (Figure 2-1). The three low-order positions (21, 22, 23) can be used for true add and subtract operations. Positions 0-20 are used for incrementing and decrementing. The increment/decrement positions process carries or borrows from position 21 of the full adder. The adder also accepts +1 or -1 to position 20 or 23, and 1s to positions 18, 19, 20.

An increment or decrement operation is performed by placing a data address, a command address, or an SSC count in the adder, then gating a +1 or -1 to position 20. An increment or decrement does not affect the three low-order positions

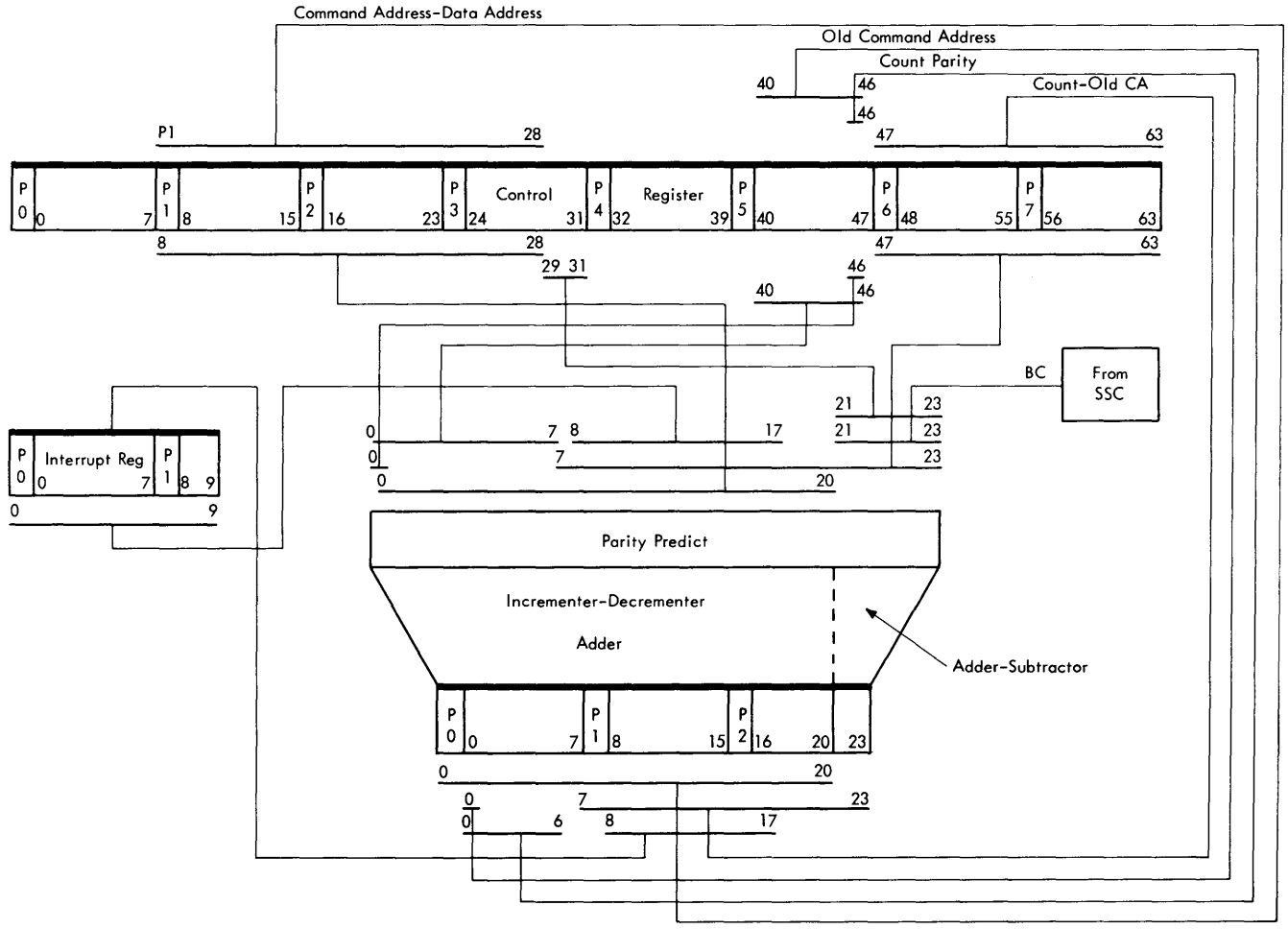


Figure 2-1. Adder Data Flow

of the adder. On read or write operations the increment function of the adder increases the data address by eight for each doubleword of data stored or fetched; on chained CCW fetches, the increment function increases the CCW address by eight. The decrement function is used by read backward or SSC count operations. For each doubleword of data sent to main storage during a read backward operation, the data address field is decremented by eight. Each time an SSC device transfers a doubleword of data to or from main storage, the count is placed in the adder and decremented by eight.

During multiplex subchannel operations, the adder decrements the count by one each time a byte of data is transferred over the MSC I/O interface. To perform this operation, the count field (from UCW 0) is placed in the adder, a byte count of one is forced, and a full subtract is performed. The result is returned to UCW 0.

When a CCW is fetched for an SSC device (start I/O or chained CCWs), the CCW count field and DAB are added to form the count field of UCW 0. This provides the SSC with an end count (location of the last byte to be transferred), and causes the count field of UCW 0 to indicate the actual number of main storage transfers to be performed. The count plus DAB operation is performed by gating the CCW count to positions 7-23, the DAB (CCW bits 29-31) to positions 21-23, and executing a full add. The result is placed in control register positions 48-63. Any overflow sets bit 47 (bit 46 is also set to correct parity in byte 5).

If an SSC operation terminates before the count is exhausted, the SSCs residual count is subtracted from the count field of UCW 0; this provides the CSW with a correct count. The operation is performed by gating the count field of UCW 0 to positions 7-23, and subtracting the SSC residual count (positions 21-23). The result is placed in control register positions 48-63.

If a local storage reset is performed, the main channel interrupt register becomes the local storage address register; the adder is used to increment the addresses. To address local storage for resetting, the adder and the interrupt register are used as follows:

1. The interrupt register is used as a local storage address register.
2. To increment the local storage address, the contents of the interrupt register are gated to adder positions 8-17.
3. To cause a carry into adder position 17, hot 1's are sent to adder positions 18, 19, and 20 and position 20 receives a carry.
4. Adder positions 8-17 (old address +1) are gated to the interrupt register.
5. The cycle continues until local storage is cleared.

Parity prediction (generation), but not parity checking, is performed by the adder. A predicted parity bit is associated with each output byte of the adder. The parity bit is generated by the adder and is based on the type of operation (full add or increment) and the input bit configuration. Actual parity checking of adder results is performed at the control register when the UCW is stored in local storage.

The adder outputs feed the adder latches, which are polarity holds. When the control line to the polarity holds is up, the outputs of the polarity holds (adder sum outputs) follow the input; when the control line is dropped (latch-adder condition), the outputs of the polarity holds are locked. Changes at the inputs to the latches no longer affect the adder sum outputs. Figure 2-2 shows the use of

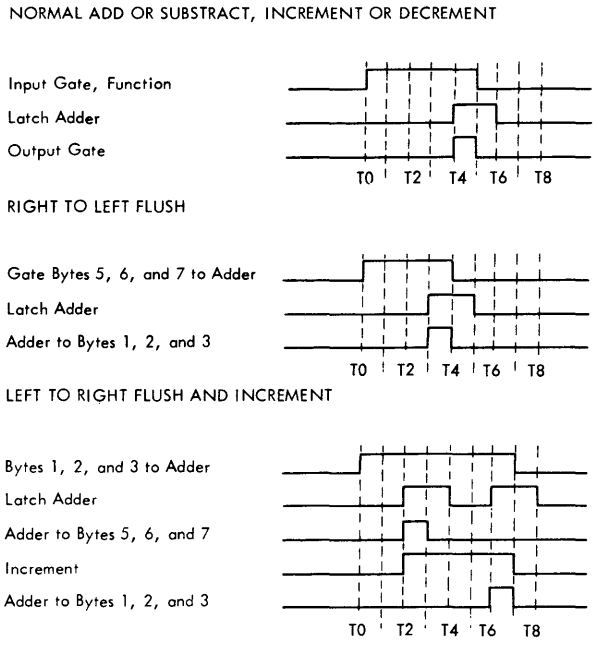


Figure 2-2. Adder Timings

the latch adder line for three operations. In each operation the adder outputs are latched while the adder results are gated into a register. The third operation (left to right flush and increment) shows the adder latches providing an output while the adder is generating a new sum. The operation proceeds as follows:

1. Bytes 1-3 of the control register are placed in the adder (gated unchanged).

2. Latch adder becomes active and the adder output is gated to bytes 5-7 of the control register.

3. While the adder is latched, increment becomes active and the adder sum changes by plus eight.

4. Because latch adder is active, the outputs do not change.

5. Gate adder to bytes 5-7 falls, increment remains active, and latch adder falls. The new sum appears at the adder output.

6. Latch adder rises again and the latched output is gated to bytes 1-3.

PRIORITY

- The priority circuit determines which unit of the 2870 has access to the main channel registers and controls.

- Priority is assigned by type of operation to be performed.

- When priority is granted, main channel busy is set and a response is sent to the unit requesting priority.

- Priority response causes the unit requesting priority to drop its request line.

- A priority check error is generated if the unit requesting priority fails to drop its request line after response becomes active, or if a response is granted to the wrong unit.

- The 2870 (Serial No. 60,002 through 69,999) has seven levels of priority, assigned as follows: SSC1, SSC2, SSC3, SSC4, MSC, MC, and CPU.

- The 2870 (Serial No. 60,001 and 70,000 and above) has eleven levels of priority.

The 2870 consists of a main channel, a local storage, a multiplex subchannel, and as many as four selector subchannels. The data registers, controls, and trigger sequences of main channel are used for local storage or main storage cycles, and for all communications between the 2870 and BCU or CPU. When CPU issues an I/O instruction or interrupt response, or a subchannel requires access to a UCW for a device, the unit must use the main channel controls. Because only one subchannel or the CPU can use main channel at any one time, all units vie for access through the priority circuit.

In the 2870 there are eleven (*seven) levels of priority. Priority is assigned by type of operation to be performed. An SSC that needs to store or fetch data from main storage has priority over the MSC or CPU. Because of the duplication of operations on the SSC's, the priority requests can be considered as five groups:

1. SSC (1-4) data -- an SSC needs main channel to fetch or store a doubleword of data during an I/O operation.

2. MSC -- the MSC needs main channel trigger 1 sequence for a data fetch or store, or triggers 7 or 9-10 for a CSW sequence.

3. SSC (1-4) secondary -- an SSC needs main channel controls to:
   a. Fetch a new CCW for a chained operation.
   b. Assemble a CSW under triggers 5-6 or 7.
   c. Fetch one or two doublewords of data at the beginning of a write operation.
   d. Interrupt response to SSC.

4. Main channel -- the CPU issues a start I/O, test I/O, or halt I/O instruction to the channel, or the MSC needs a CCW or doubleword of data for a chain command reselection sequence.

5. CPU -- CPU has raised interrupt response in answer to an interrupt request from the MPX chan only. A CSW will be transferred to main storage by trigger 11 or the log circuits.

To access main channel controls, a subchannel, the main channel, or CPU raises its priority request line. The priority circuit continually samples for the highest priority request by causing the highest request to block all lower priority units. When the priority circuit grants a response to a requesting unit, the main channel busy latch is set, a check is made that the correct response is given, and the priority circuit begins to sample for more requests. However, until the unit granted priority releases main channel by resetting the main channel busy latch, no other response is granted.

The timing chart in figure 2-3 and the diagram in figure 2-4 show the operation of the priority circuit. The timing chart assumes that main channel is not busy when the first priority request is made, and that a different unit makes a priority request prior to the release of main channel by the first unit.

Assume that SSC 3 makes a priority request for a CSW cycle. SSC 3 secondary request becomes active to the priority circuit. Because priority sample is active, the SSC 3 secondary request latch is set. Any

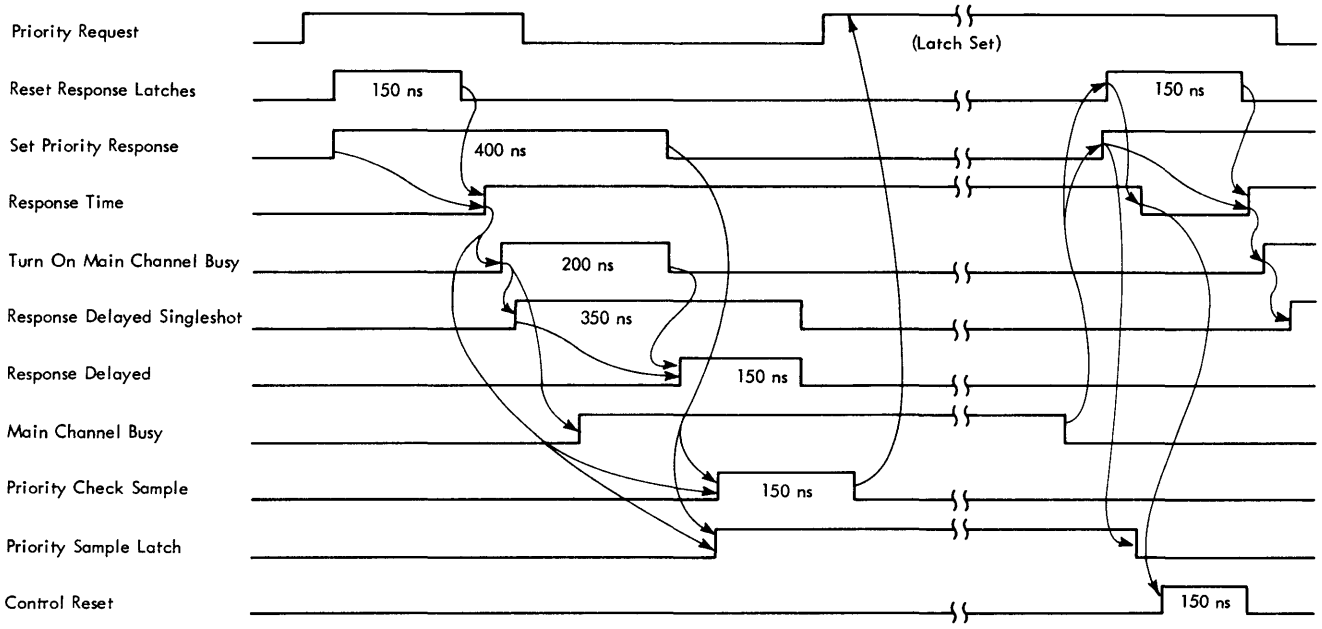


Figure 2-3. Priority Circuitry Timing Chart

priority latch set, raises the priority request line. At the same time, the SSC 3 secondary request line becomes active to the gating circuit of the SSC 3 response latch.

Priority request and not main channel busy fire the reset response and set response singleshots. The reset singleshot resets all response latches (including response time check) and blocks the gate line to the response latches. The set response singleshot resets the priority sample latch (blocking the set to any other request latches), gates the turn on of the response latches (when the reset singleshot expires), and sets the response time check latch. With the gate line active, the SSC 3 secondary request line sets the SSC 3 response latch. Priority response becomes active to SSC 3. SSC 3 recognizes that it has priority and drops its request line but does not begin operations with main channel until response delayed becomes active.

Response time check fires the busy and sample singleshots. Busy sets the main channel busy latch and fires the response delayed singleshot. The response delayed pulse is generated when the busy singleshot expires. Response and response delayed are used by SSC 3 to gate its control lines to main channel and select the trigger or control sequence to be performed. Main channel busy blocks any further priority response cycles until SSC 3 releases main channel by resetting the busy latch.

As seen in the timing chart, the sample singleshot fires approximately 400 ns after response is granted. At this time the check latch should be set and the request line from SSC 3 should be down. The check latch is set by comparing the priority request with the response. Request falls when SSC 3 receives the response signal. If the request and response are not equal or if SSC 3 fails to drop its request, a priority check is generated when the sample singleshot fires. The sample singleshot also sets the priority sample latch, and blocks the priority sample line and response gating circuits until main channel busy becomes active.

When the sample singleshot expires, priority sample rises to allow other priority requests to set their respective priority request latches. While main channel busy is on, the setting of a priority request latch cannot reset the response latches. All requests remain pending until main channel busy is reset.

As shown in the timing chart, if other requests are active when main channel busy is reset, the highest request is granted priority and a response latch is set. On this cycle, the reset of the response time check latch generates a control reset pulse and resets the check latch; the rest of the cycle operates in the same manner.

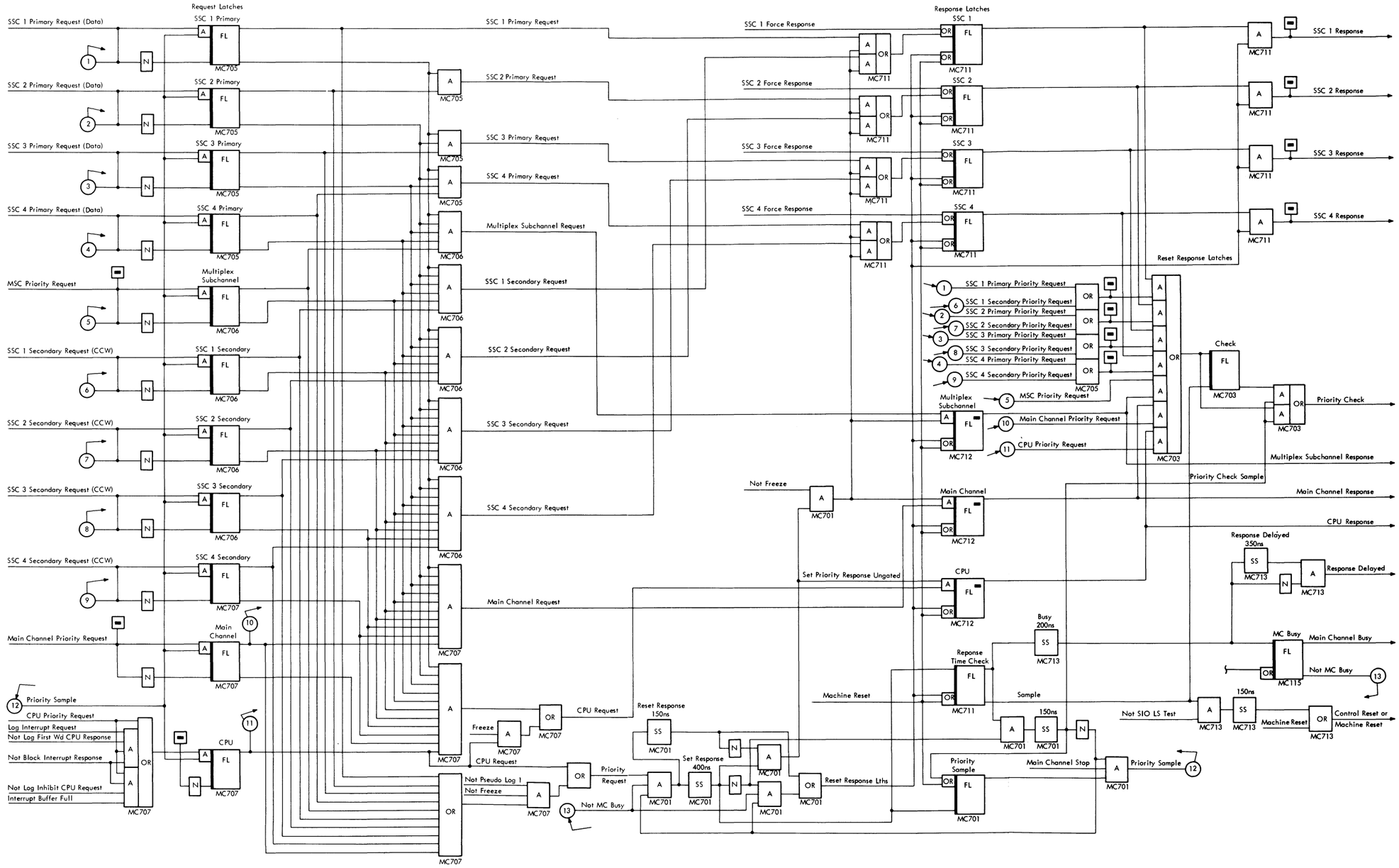


Figure 2-4. Priority

MAIN CHANNEL CLOCK

- The main channel clock produces the timing pulses that control main channel operations.
- Timing and control of the main channel clock is independent of other clocks in the system or channel.
- The clock sequence advances toward T11 time as long as the clock control latch is on.
- Once on, a clock output remains on until the clock control latch is reset.
- As a diagnostic aid, the clock can be stopped at the time pulse at which an error occurs.

The main channel clock (Figure 2-5) produces the sequential timings required to control main channel operations. CPU instruction execution, adder operations, mode trigger sequences, and logout are all controlled by the timing pulses generated by the clock. Because main channel operates independently, the main channel clock timings are not controlled by either the CPU or the subchannel clocks.

Clock Sequence

The main channel clock produces 12 sequential times. These 12 times, labeled T0 through T11, are produced at intervals of approximately 100 ns. As shown in the timing chart (Figure 2-5), each clock time remains up after it rises until the clock is turned off. Time T0 becomes active when the clock control latch is set; all other times depend on time delay circuits and flip latches. For example, time T4 becomes active when the time delay from T3 expires. These time delay circuits are adjustable delay lines, the adjustment procedure for which is given in the FE Maintenance Manual, 2870 Multiplexer Channel (60,000/70,000 Series), Form SY27-2302.

Any time during or after the sequencing of the clock latches, the clock can be turned off by resetting the clock control latch. The off side of the clock control latch fires a 150-ns singleshot which resets the clock latches and holds them reset until it expires. Should the clock control latch be immediately reset, the clock will not produce any pulses until the reset singleshot expires.

As a diagnostic aid, the main channel stop-on-error condition freezes the clock at the time an error is detected. This is accomplished by blocking the inputs to all of the time delay circuits. As seen in Figure 2-5, each time delay is controlled by the output of an AND circuit that becomes active when the previous clock pulse rises and the stop-on-error line is down. In test mode, stop-on-error condition becomes active when an error occurs with the log-on-machine-check switch in the up position. In auto mode, a CE can enable the stop-on-check condition by grounding a circuit in the channel. Freezing the clock stops any sequence in progress and allows a CE to diagnose an error in the same condition as when it occurred.

SUBCHANNEL CLOCKS

- The MSC and each SSC has its own subchannel clock.
- The subchannel clocks produce five sequential timed outputs which are used to control subchannel operations.
- The subchannel clocks operate independent of each other and of the main channel and CPU clocks.
- The SSC clocks light a clock-on indicator on the CE console.
- As a diagnostic aid, the subchannel clock cycle can be stopped at the time an error is detected in the channel.

Each subchannel has its own clock which produces subchannel timing pulses independent of CPU and main channel clocks. In both the MSC and the SSCs, setting, gating, and controlling of I/O interface operations use the timings of a subchannel clock. The clocks are controlled by raising an input line to start the clock, and dropping all input lines to stop the clock.

The subchannel clocks produce five outputs: A1, A2, A2 delayed, A3 gate, and A3 delayed (Figure 2-6). The clock sequence starts when one of the input lines is activated. The clock sequence continues as long as the input is active and the stop line is inactive. 'Stop' blocks the advance of the clock but does not reset it. The turn-on conditions for the MSC and SSC clocks differ; both are shown in Figure 2-6. Also shown is a chart of the approximate clock timings and the additional SSC clock output 'clock on.' Clock-on lights an SSC indicator on the CE console.

The clock sequence is:

1. One of the input lines is activated.
2. The A1 latch is set and the A1 pulse is generated approximately 100 ns later.
3. The A1 latch conditions the AND circuit which starts the time delay for the A2 and A2 delayed turn off pulses.
4. For SSC clocks, the output of the A1 latch also lights the SSC clock on indicator on the CE console

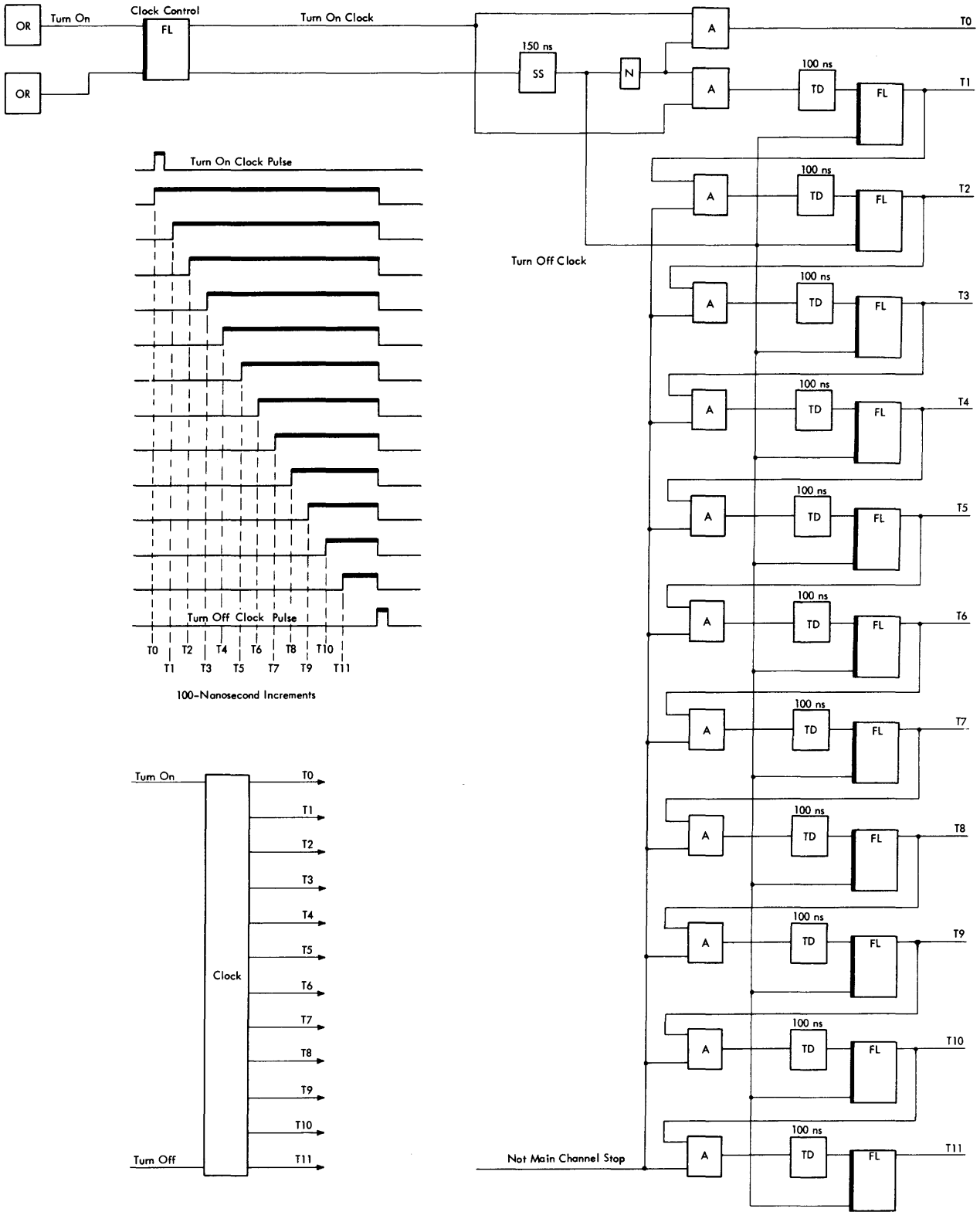
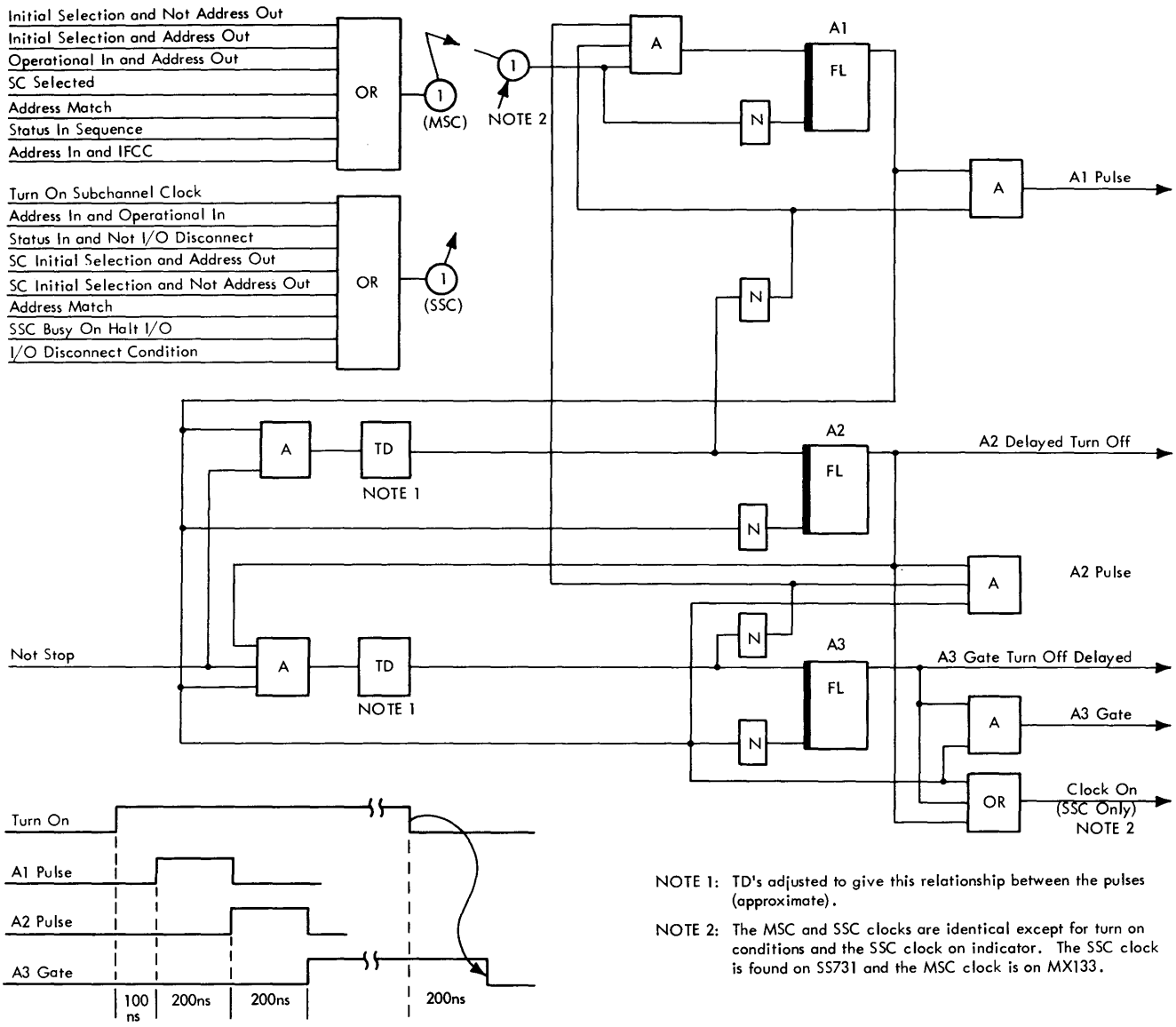


Figure 2-5. Main Channel Clock



NOTE 1: TD's adjusted to give this relationship between the pulses (approximate).

NOTE 2: The MSC and SSC clocks are identical except for turn on conditions and the SSC clock on indicator. The SSC clock is found on SS731 and the MSC clock is on MX133.

Figure 2-6. Subchannel Clock

(this light remains on while the clock is active).

5. The A2 latch is set approximately 200 ns after the A1 pulse. The A1 and A2 latches remain on (generating the A2 and A2 delayed turn off pulses), but the A1 pulse is terminated. A2 latch output conditions the AND circuit which starts the time delay to turn on the A3 latch.

6. The A3 latch is set approximately 200 ns after the A2 latch. A1 and A3 latches are ANDed to form the A3 gate. The A2 pulse terminates when the A3 latch is set.

7. As long as the input line remains active, the A2 delayed turn off, A3 delayed turn off, and A3 gate lines remain active.

8. When the input line becomes inactive, A3 gate, A3 delayed turn off, and A2 delayed turn off are terminated (200 ns later); all latches are reset.

9. If the stop line becomes active during the clock sequence, further advance of the clock is blocked. Stop has no effect on a subchannel clock if the clock has completed its cycle.

LOCAL STORAGE

- Local storage has a capacity of 1,024 words (72 bits long).
- Local storage consists of two 1,024, 36-bit arrays in parallel.
- Local storage can perform multiple read before write cycles.

- Four unit control words (local storage words) are assigned to each device.

To operate multiple devices concurrently, information about each device is stored in local storage (Figure 2-7). Four unit control words are assigned to each device (Figure 2-8). The 2870 local storage is a 1,024 doubleword array (72-bit word, 1-usec), using standard 10-ns SLT circuits (actually, two separate 36-bit arrays in parallel).

Each of the two local storage arrays has nine planes, containing four bit matrices per plane (Figure 2-9). Each bit matrix consists of 32 by 32 type T56 cores. As shown in Figure 2-9, the X and Y drive lines are common to each of the nine planes. There is a sense/inhibit winding for each matrix (Figure 2-10). The nominal read/write cycle is 1 usec, and independent read/write operations require 500 ns.

Sense/Inhibit Winding

One line is used for both sensing and inhibiting. Each bit has one associated sense and inhibit line. The sense/inhibit winding is a loop threaded through each core in the matrix (Figure 2-10). The sense line detects whether the addressed core is 1 or 0. Sensing is performed only during read operations; inhibiting is performed during write operations.

Read

During a read operation, a strobe pulse is generated to gate the sense amplifier. The strobe pulse is approximately 150 ns wide, delayed 120 ns after the use of the read Y gate. The X and Y drive lines select one core. If this core has a 1, the coincidence of plus I/2 in the two drive lines causes the core to flip (Figure 2-11). The flux state of the core changes to 0. When the core changes state, a voltage is induced in the sense winding and a pulse is produced at the sense amplifier. If the core is already in state 0, no change of state occurs and no current is induced in the sense/inhibit line. During the read operation, plus I/2 current is always present in both drive lines and the selected core stays at 0 or is reset to 0. This is called destructive readout.

Write

During a write operation, the write X gate controls the inhibit drivers. This ensures an overlapping of the X and Y current by the inhibit drivers; thus, the core is prevented from jumping from one state to another. If the inhibit line rises at a later time, a 1 may be stored accidentally.

During a write operation, plus I/2 current is sent on the X and Y lines to select a core. Because the core is in state 0, it flips to state 1. It may be necessary, however, to write a 0 in the core. In this case, minus I/2 current is sent on the sense-inhibit line that is opposite the plus I/2 current on the X line. The two opposite currents cancel, leaving the plus I/2 Y current. The plus I/2 Y current is not sufficient to flip the core and the state is not changed to 0. Actually, a 0 is not written; the inhibit current opposite the Y current prevents the writing of a 1 (Figure 2-11).

Strobe Generation

The read Y gate causes a strobe pulse to be generated. The strobe pulse is sent to the sense amplifier gating out the data. Thus, the strobe pulse is used only in a read operation.

The delay, which is controlled by an adjustable singleshot, establishes when the strobe will be initiated (Figure 2-12). The width of the strobe pulse is controlled by a fixed singleshot circuit (Figure 2-12).

Location Addressing

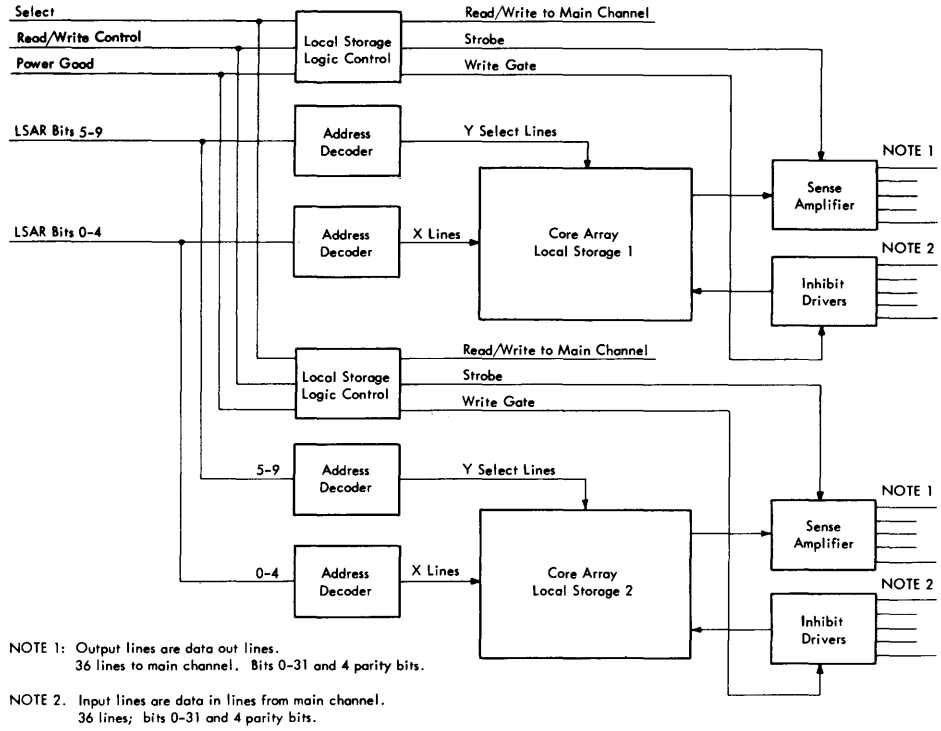
Local storage address (LSAR) bits from the main channel determine the address location. Each address is formed by the eight-bit address of the device plus two additional low-order bits. These two low-order bits determine the UCW sought. The five high-order bits are used for addressing an X line; the five low-order bits are used for addressing a Y line:

LSAR Bit	0 1 2 3 4	9 6 7 8 5
	X Line	Y Line

By using the five high-order and five low-order bits, 32 by 32 or 1,024 addresses are defined. The 32 partial addresses are formed from a 4 by 8 matrix.

The selection logic consists of read and write drivers, and read and write gates. During a read/write operation, the appropriate drivers and gates are conditioned to select the addressed core (Figure 2-13). The drivers provide the current, and the gates complete the circuit through a particular line of local storage. In addressing, only one gate and one driver are conditioned for each X and Y address line chosen.

Figure 2-13 shows the logic used to select both the X and Y lines for either a read or a write operation. Note that the bits used to select the X lines are shown in parentheses.



NOTE 1: Output lines are data out lines. 36 lines to main channel. Bits 0-31 and 4 parity bits.

NOTE 2. Input lines are data in lines from main channel. 36 lines; bits 0-31 and 4 parity bits.

Figure 2-7. Block Diagram of Local Storage

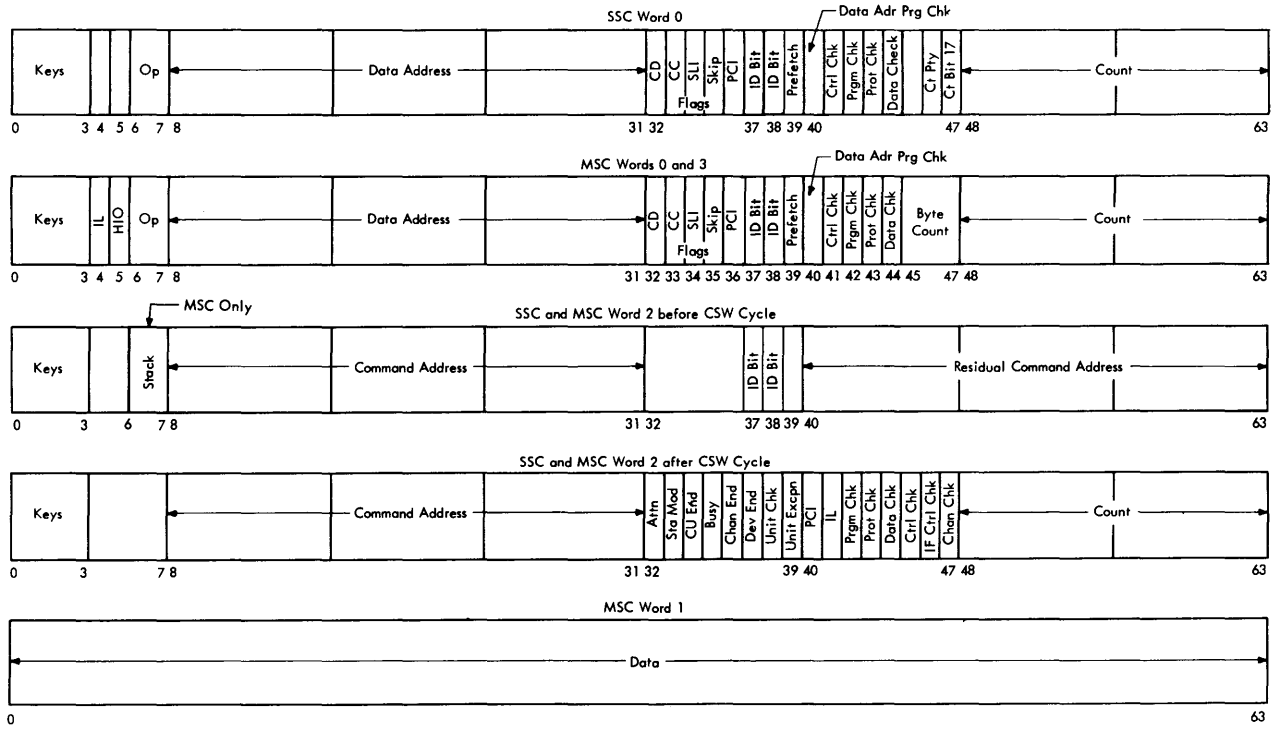
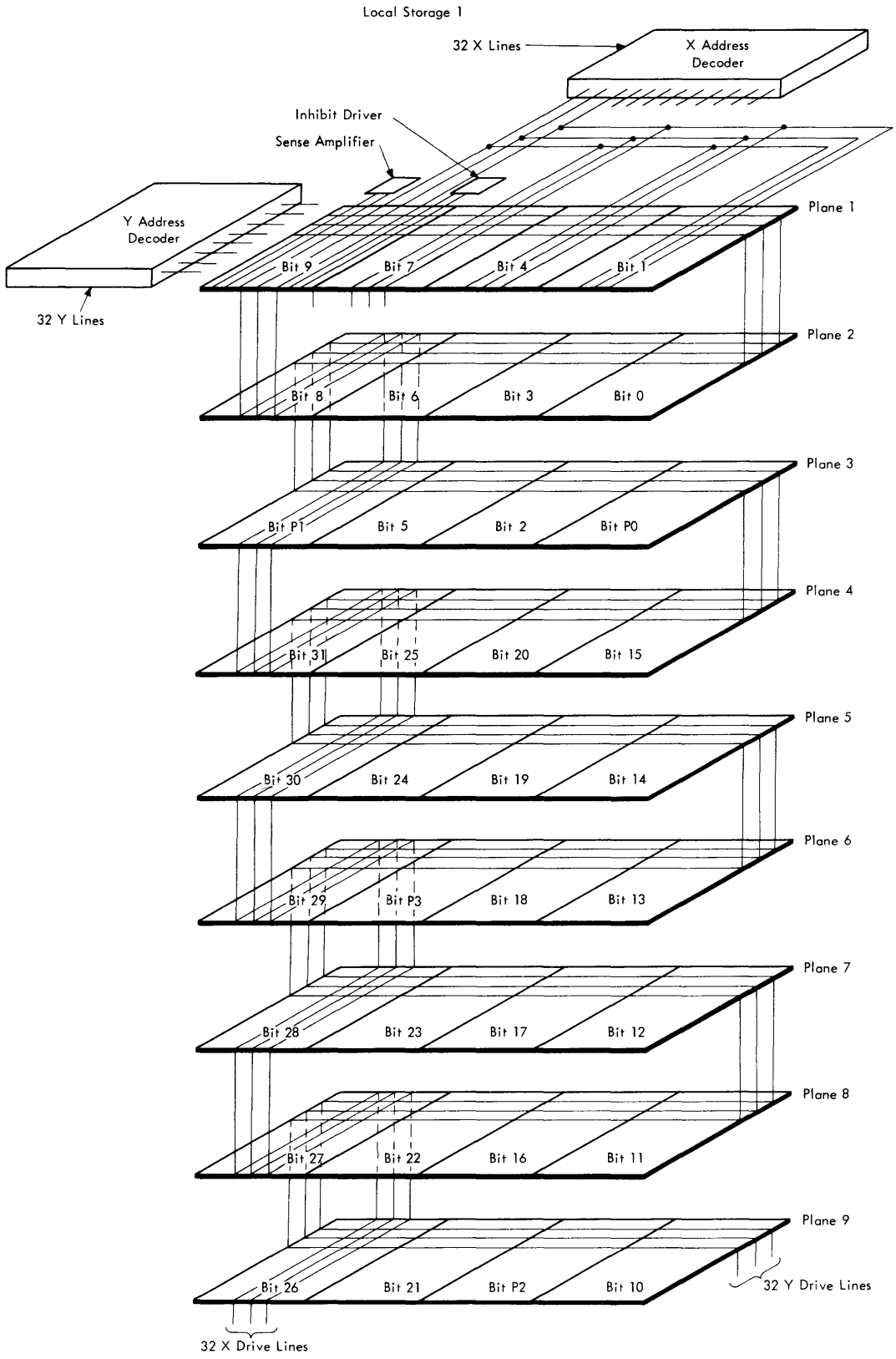


Figure 2-8. Local Storage Words



NOTE: There is an identical core array for local storage 2.

Figure 2-9. Local Storage Array

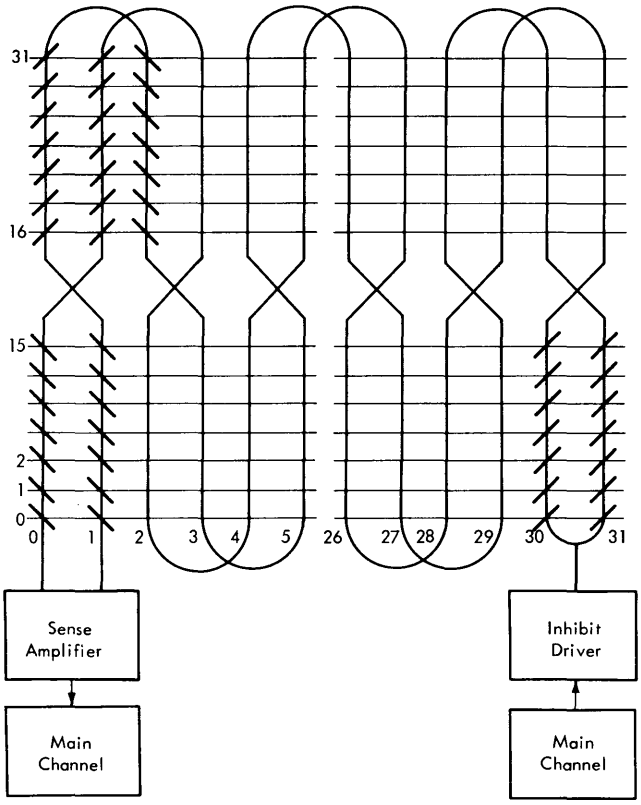


Figure 2-10. Sense/Inhibit Line

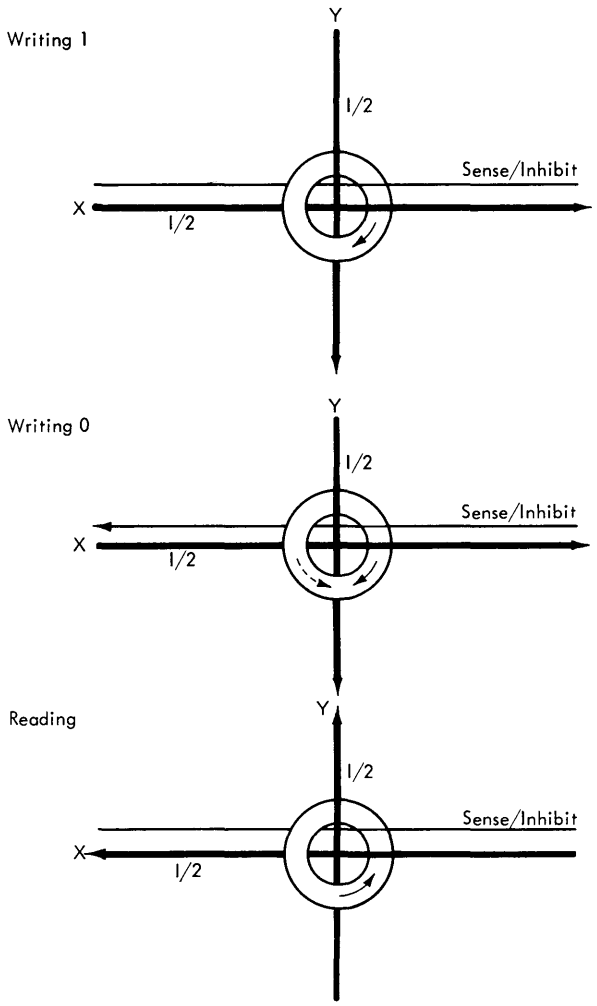


Figure 2-11. Core Reading and Writing

Consider the following example of a write operation for UCW 1 of device "AA":

Bits	0 1 2 3 4 5 6 7	Mod 89
AA	1 0 1 0 1 0 1 0	UCW 1 - 01
	X Selection	Y Selection
	0 1 2 3 4	5 6 7 8 9
	1 0 1 0 1	0 1 0 0 1
	0 1 2 3 4	9 6 7 8 5
Address as used by local storage	1 0 1 0 1	1 1 0 0 0
Value	21	24

The X line (21) is selected by write driver 2 (conditioned by bit 4, not bit 3, write, X write current source) and write gate 6 (write, bit 2, not bit 1, bit 0). The Y line (24) is selected by write driver 1 (Y write current source, write, not bit 5, not bit 8) and write gate 7 (write, not bit 7, bit 6, bit 9). Notice that local storage addressing uses address bits 9 and 5 reversed, and that the value of the address bits is the number of the line selected.

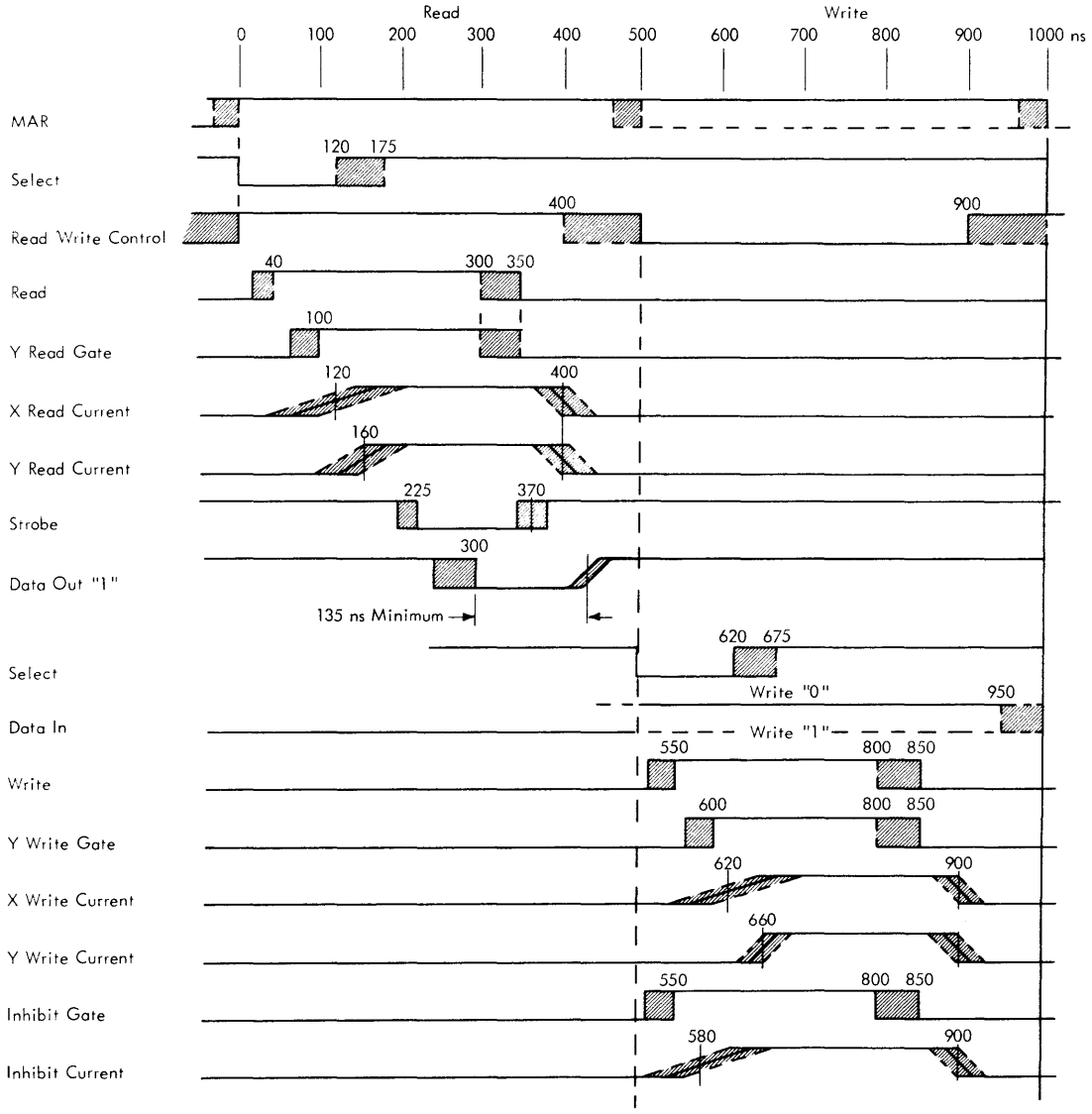


Figure 2-12. Local Storage Timing Chart

INPUT OR

- Input OR is 72 bits wide.
- Doublewords are transferred from input OR to the data register.
- The input OR gates byte 0 to the command register and multiplex CC command register.

The main channel input OR has a capacity of 72 bits (doublewords). Inputs from main storage bus out and the CE simulate storage bus out switches are gated through the OR to the main channel data register.

Byte 0 (the command byte) of a multiplex CCW is gated to the command register or multiplex CC command register.

DATA REGISTER

- The data register handles doubleword transfers between main storage and the 2870.
- The data register receives the CAW and CCW from main storage.
- The data register is used by the multiplex subchannel for the assembly or disassembly of doublewords of data.
- The data register transfers doublewords of data between the subchannels and main storage.

The main channel data register is a 72-bit (64 data plus 8 parity bits) register (Figure 2-14).

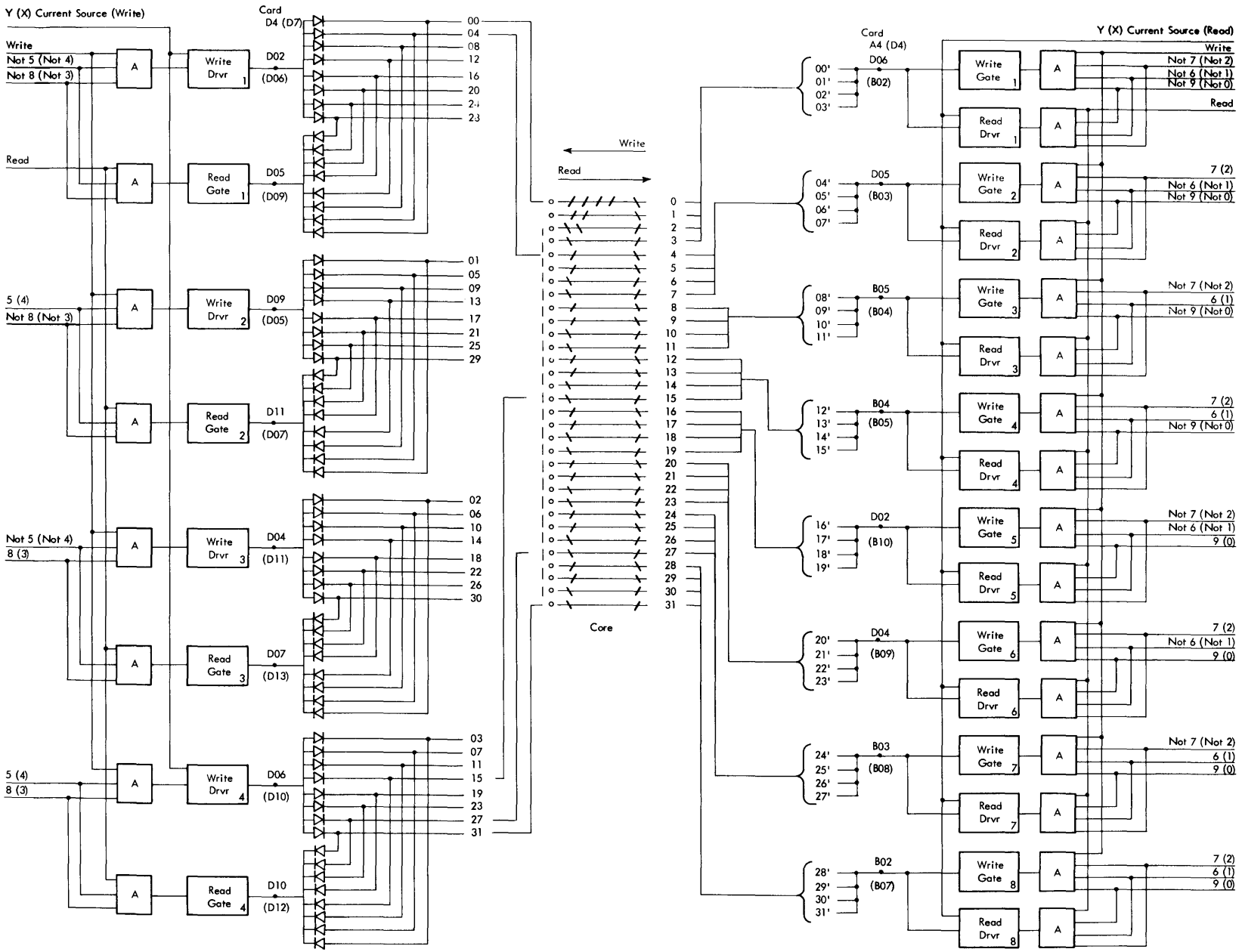


Figure 2-13. Local Storage Addressing

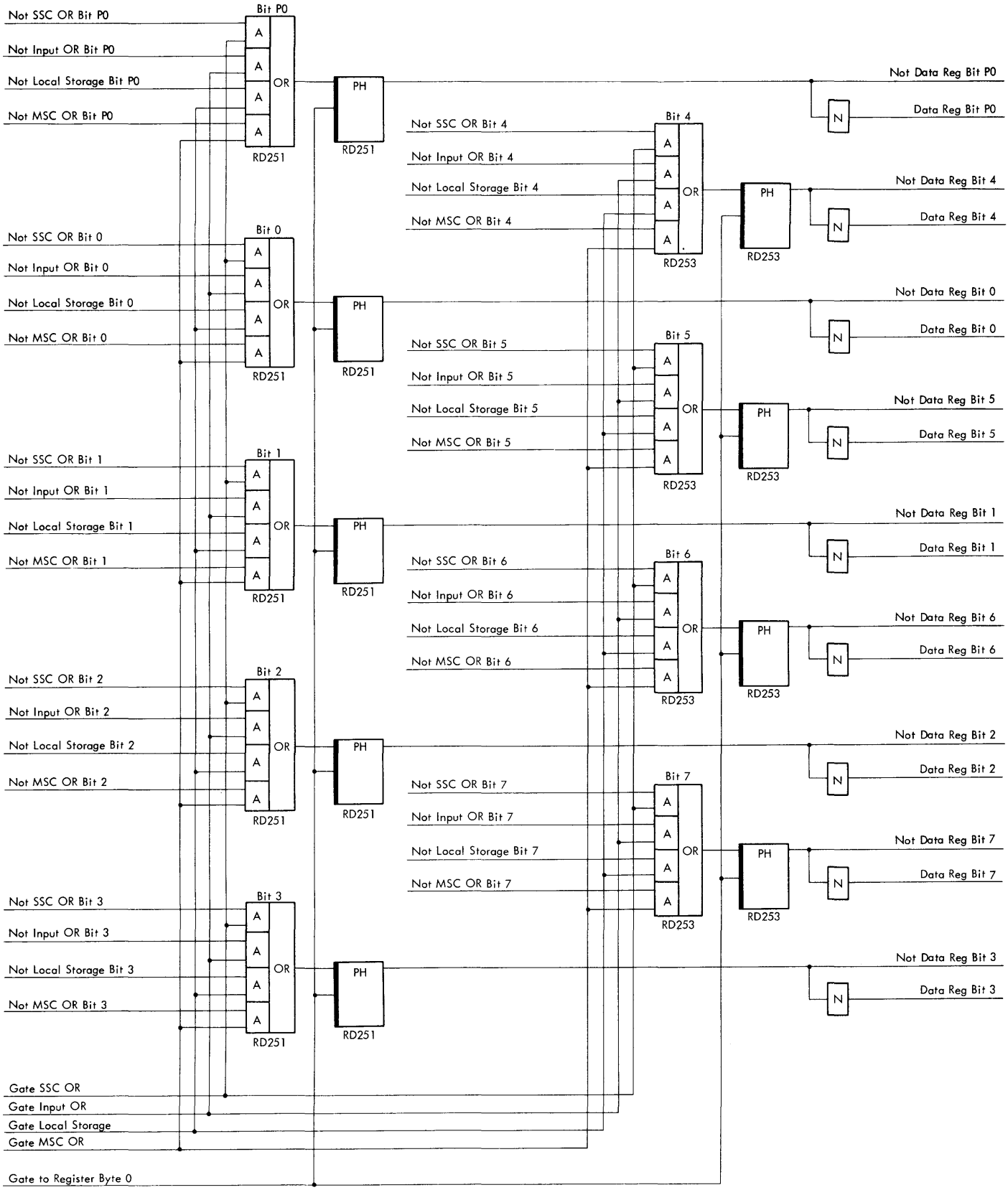


Figure 2-14. Data Register Byte 0

Information is gated into the data register from the input OR, selector subchannels, multiplex subchannel, and local storage bus out. CAWs, CCWs, and data are transferred in doublewords to the data register.

The selector subchannel sends doublewords of data (read operation) or bytes of status to the data register. From the data register, the selector subchannel receives doublewords of data (write operation) or the command bytes (start I/O or chain command).

The multiplex subchannel sends or receives data, status, or commands by bytes. During an MSC read operation, data is received from the MSC by bytes and is assembled in doublewords. During a write operation, doublewords of data are placed in the data register and gated to the MSC data OR by bytes.

CONTROL REGISTER

- The control register holds information to control the 2870 (CAW, CCW, and UCW).
- Unit control words are assembled in the control register.
- The control register is used in conjunction with the adder to perform data address update, CCW address update, count update, and residual count operations.

The control register is a 72-bit (64 data + 8 parity bits) register that controls the operations of the 2870 (Figure 2-15). Multiple fields of control information are gated selectively into and from the control register. Control information is gated into the control register by bits, bytes or doublewords.

The control register can hold a CAW, CCW, or local storage control information (UCW's). At the end of an operation initiated by start I/O or test I/O, an I/O interruption occurs; a CSW is formed in the control register and is stored in local storage until CPU interruption. The CSW is stored in main storage location 64.

The control register, used in conjunction with the adder, updates the command address, data address, and count fields for the unit control words.

COMMAND REGISTER

- The command register stores only multiplex subchannel commands.
- Byte 0 from the input OR is the only input to the command register.
- Output of command register is gated to the MSC bus out OR.

The command register is a nine-bit (eight bits plus one parity bit) register in the main channel that stores multiplex subchannel commands. When a CCW is received in the input OR from main storage, the information contained in byte 0 (the command code) is gated to the command register. At the command register, this information is gated into the register by the gate command register line. The command code contained in byte 0 specifies the operation to be performed.

MSC CC COMMAND REGISTER

- MSC CC command register holds the new command of a chained CCW.
- Register is loaded from byte 0 of a chained CCW.

The multiplex CC command register is a nine-bit (eight bits plus one parity bit) register; it stores the multiplex command to be chained. If a new (chained) CCW is requested, the new command is stored in the multiplex CC command register.

ENCODER

The encoder takes byte 0 of the data register and encodes the two-bit operation code. The two-bit operation code is stored in bits 6 and 7 of the control register. The bits mean:

6	7	
0	0	Idle
0	1	Write/Control
1	0	Read/Sense
1	1	Read Backward

SSC DATA OR

- SSC data OR gates data and status to the data register.
- Used to select which SSCs data or status information is gated to the data register.

The SSC data OR has a capacity of 72 bits (64 bits plus 8 parity bits); it gates information from the selector subchannels to the main channel data register. Data in a read operation is transferred to and from the SSC data OR in doublewords. When applicable, the SSC data OR gates control unit and SSC status-in bytes 4 and 5 to the main channel data register.

STORAGE ADDRESS BUS (SAB) REGISTER

- The SAB register is a 24-bit register.
- Data and command addresses are loaded from the control register.

The SAB register is a 21-bit plus 3 parity-bit register (Figure 2-16). The register stores addresses for main storage fetching and storing operations. Data and command addresses are loaded from bits 8-28 of the control register. The CAW, CSW, or log addresses are set in the storage address register by the channel controls.

INTERRUPT REGISTER

- The interrupt register holds the unit address of any multiplex subchannel device that has an interruption pending.
- This register holds only the address of one device (all other interruptions are stacked in the control units).
- Register is used as a local storage address register during local storage reset and test operations.
- It holds the device address for an SSC with pending PCI interrupt.

The interrupt register contains ten bits plus a parity bit. After the multiplex subchannel has accepted ending status, assembled a CSW, and stored the CSW in local storage, the device address is placed in the interrupt register to await CPU interrupt response. When the CPU response arrives, the CSW is read from local storage and sent to main storage.

In the case of a selector subchannel program-controlled interruption, the interrupt register holds the unit address. In all other cases, the selector subchannel unit address is not loaded in the interrupt register; instead, an interrupt pending line is raised.

To address local storage for resetting, the adder and the interrupt register are used as follows:

1. The interrupt register is used as a local storage address register.
2. To increment the local storage address, the contents of the interrupt register are gated to adder positions 8-17.
3. To cause a carry into adder position 17, hot 1s are sent to adder positions 18, 19, and 20 and the line 'gate byte count to the adder' causes a carry to position 20.
4. Adder positions 8-17 (old address plus one) are gated to the interrupt register.
5. The cycle continues until local storage is cleared.

DAB REGISTER

- The DAB register holds the DAB portion of the data address (bits 29-31 of the CCW).
- This register gates the DAB bits to the SSC byte count backup register to initiate an SSC operation.

The DAB register stores bits 29-31 (DAB) of the data address of the CCW. DAB designates the byte at which to start storing or fetching operations. The DAB is also used to set the byte count; it establishes the initial byte of the SSC byte counter.

UNIT ADDRESS OR

- The main channel unit address OR has a capacity of 11 bits.
- The main channel unit address OR supplies local storage addresses.

The unit address OR has a capacity of nine bits (eight bits plus one parity bit) for unit addressing, and two local storage address modification bits. These local storage address modification bits are used in addition to the nine unit address bits to generate a local storage address.

Inputs to the MC unit address OR are from the SSC and MSC OR, the interrupt register, the logout register, and the initial unit address register.

The output of the MC unit address OR can be gated to local storage, local storage OR, storage bus in OR, interrupt register, logout register, initial unit address register, and unit address bus in.

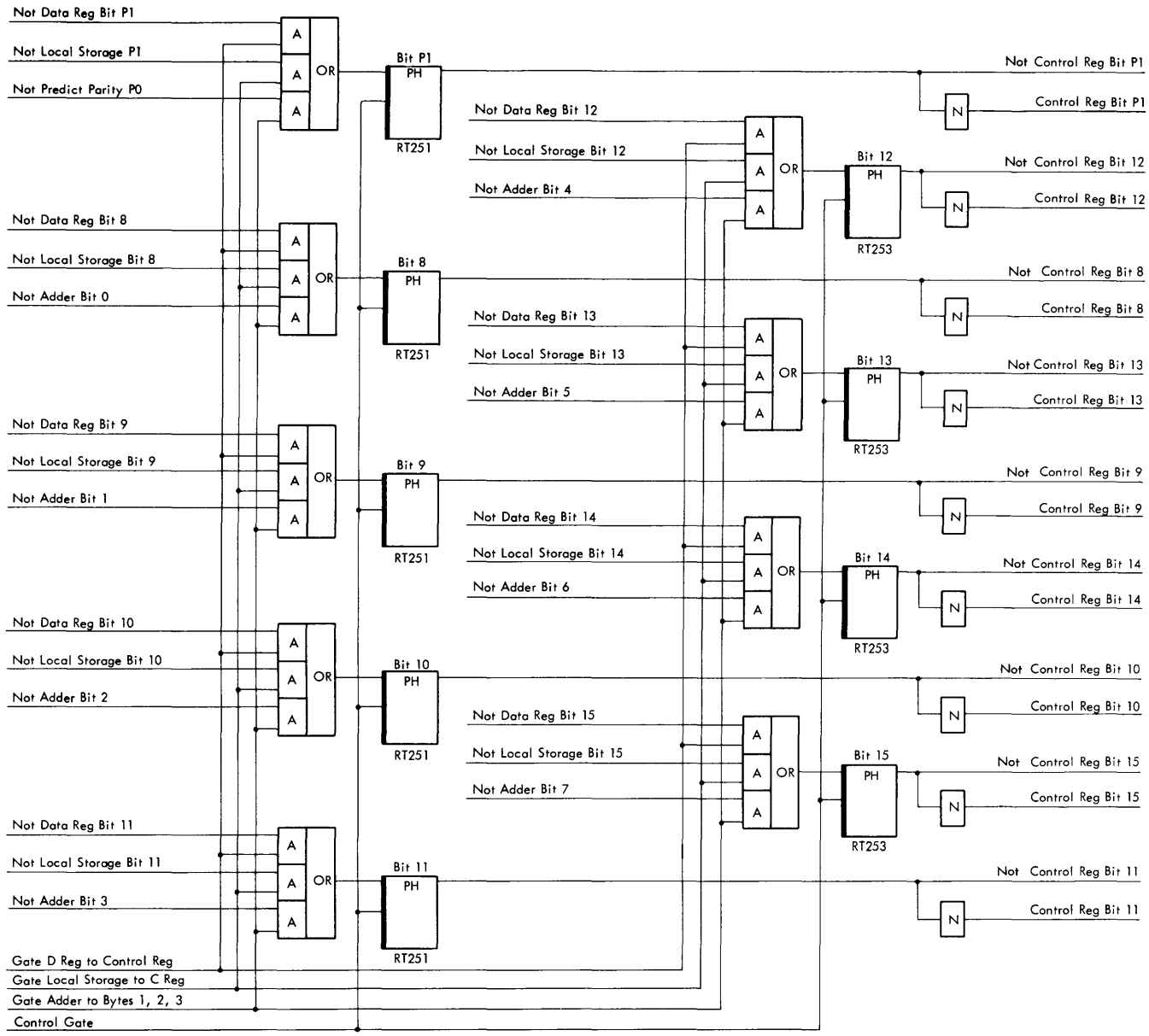
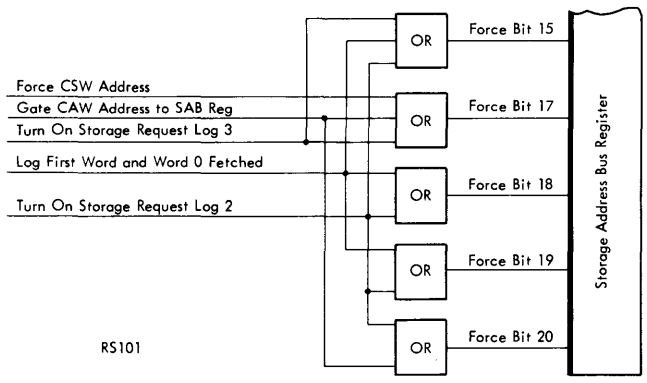


Figure 2-15. Control Register Byte 1



Bit	15	16	17	18	19	20	21	22	23
Value	256	128	64	32	16	8	4	2	1

Not Used

To:

Store CSW	Bit 17	Address 64
Fetch CAW	Bits 17, 20	Address 72
Store Log Word 1	Bits 15, 18, 19	Address 304
Store Log Word 2	Bits 15, 18, 19, 20	Address 312
Store Log Word 3	Bits 15, 17	Address 320

Figure 2-16. Force Storage Address Bits

INITIAL UNIT ADDRESS REGISTER

- Holds the initial unit address for I/O operations.
- The contents of this register can be gated to the multiplex or selector subchannel unit address registers or to the main channel unit address OR.

The initial unit address register is a one-byte register that stores the unit addresses from the CPU for initial selection operations. The contents of the register can be gated to the SSC or MSC unit address registers or to the main channel unit address OR.

COUNT OR

- Count OR gates end count bits 1, 2, and 4.
- Count OR gates last word and double last word latches.

Count OR gates bits 1, 2, and 4 from the SSC end count register; it gates the SSC last word and double last word latches to bits 59-63 of the control register (Figure 2-17). End count bits 1, 2, and 4 are gated to control register bit positions 63, 62, and 61. Last word and double last word latches are gated to control register bit positions 60 and 59.

MARK ENCODER

- Mark encoder encodes DAB and byte count bits to designate mark lines.
- Used each time information is sent to main storage.

Mark encoder takes the contents of the main channel DAB register and either the MSC byte count or the selector subchannel residual byte count and encodes the information to designate the proper mark lines. These mark lines are raised to the BCU to designate the bytes to be stored.

MSC SIMULATE I/O REGISTER

- The simulate register is a nine-bit register.
- This register is located between bus out and bus in of the multiplex subchannel.
- The register receives the bytes transmitted during a write or control operation.
- It retains the last byte written during a write operation.

The multiplex simulate I/O register is a nine-bit register located between bus out and bus in. Input to this register is from multiplex bus out OR; the output from this register is gated to the MSC bus in OR. The simulate register receives the bytes transmitted over bus out during a simulated write or control operation. The last byte written is retained and placed in the bus in OR during a simulated read operation.

MSC BUS IN OR (BIOR)

- MSC BIOR gates the MSC bus in and the MSC simulate I/O register.
- MSC BIOR has a capacity of one byte.

MSC bus in OR gates a byte of information from either the control unit bus in or the MSC simulate I/O register, to the unit address OR, address compare, and the main channel data register. Bits on bus in are gated by 'not simulate IF,' and bits from the simulate register are gated by 'diagnostic simulate IF.' The gated bus in and simulated bits are OR'ed (Figure 2-18).

MSC DATA OR

- MSC data OR receives a full doubleword from the main channel data register.
- MSC data OR has a capacity of one byte.
- The register gates bytes to the MSC data register.

MSC data OR has an output of one byte. Sixty-four bits of information (one doubleword) are received from the main channel data register. Corresponding bits in each byte are gated by bytes and are ORed to provide one byte for transfer to the MSC data register. See Figure 2-19.

MSC DATA REGISTER

- The MSC data register has a nine-bit capacity.
- The MSC data register stores one byte of data.

The MSC data register is a nine-bit (eight bits plus one parity bit) register that stores one byte of data from the main channel data register. The contents of the data register are gated to the MSC bus out OR for transfer to the I/O bus out or the simulate I/O register.

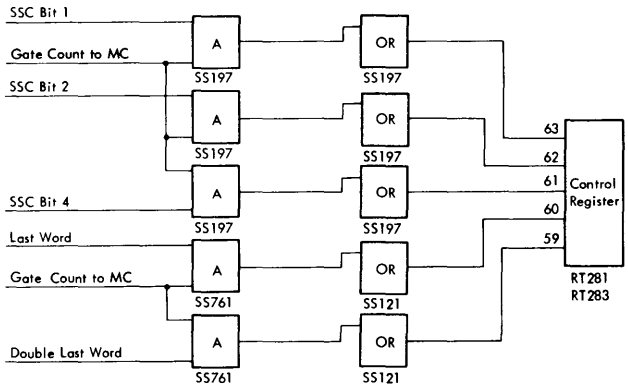


Figure 2-17. Count OR

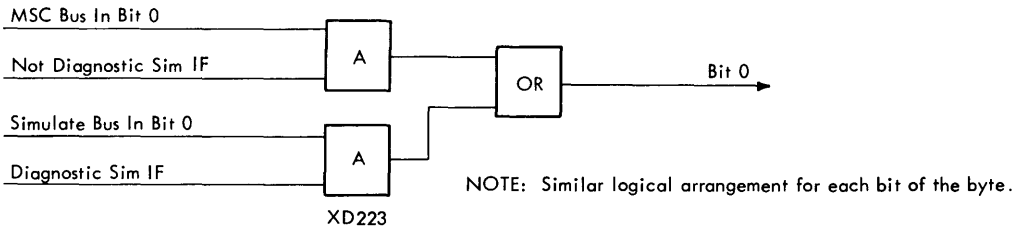
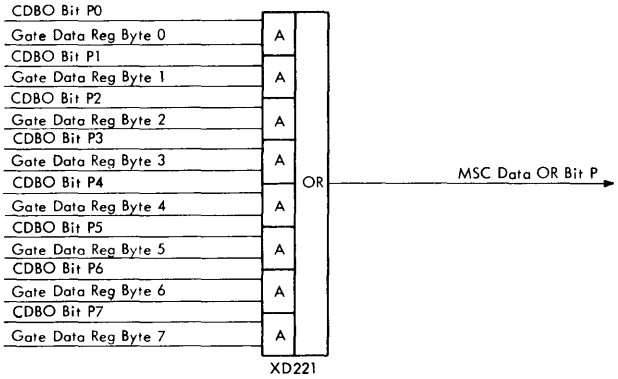


Figure 2-18. MSC Bus In OR



NOTE: There is similar logical gating for corresponding bits of each byte.

Figure 2-19. MSC Data OR

MSC BUS OUT OR

- MSC bus out OR gates information to the I/O bus out.
- MSC bus out OR provides the input to the simulate I/O register.

MSC bus out OR receives inputs of one byte each from the main channel command register, the MSC data register, the MSC unit address register, and the main channel multiplex CC command register. Information from these inputs is ORed and gated to MSC I/O bus out. The bus out OR also provides an input to the simulate I/O register. Each byte is parity checked in the bus out OR.

MSC ADDRESS COMPARE

- This circuit compares addresses from the main channel and control unit.
- An unequal comparison sets the incorrect selection latch and interface control check.
- If the addresses compare equally, address match is generated.

The main channel initial unit address register sends an address to the control unit via the MSC unit address OR, unit address register, and bus out OR. The control unit address is returned to the MSC on bus in and is gated through the MSC bus in OR to address compare. The address received from the control unit is compared with the addresses sent to the control unit. If the addresses are an equal compare, an address match condition is generated for use in initial selection. However, if the addresses do not compare equally, an address mismatch condition is generated that sets the MSC incorrect selection latch. The setting of the incorrect selection latch turns on MSC interface control check. See Figure 2-20.

SUBCHANNEL UNIT ADDRESS OR

- Unit address OR has a nine-bit capacity.
- Output of unit address OR is gated to the unit address register.

The subchannel unit address OR gates multiplex and selector subchannel unit addresses to the main channel unit address OR. The multiplex subchannel addresses are full eight-bit bytes. The selector subchannel addresses consist of unit address bits 4-7 and selector subchannel 1-4 response lines. See Figure 2-21.

SELECTOR SUBCHANNEL A AND B DATA REGISTERS

All data, status, or commands transmitted to or from the selector subchannels use the A and B data registers. Data flows in the selector subchannels as follows:

1. Data or commands are transmitted from the main channel to the SSC interface, then to the SSC A register (doublewords of data or byte commands).
2. Data or status bytes are transmitted from the SSC I/O interface to the SSC A register (one byte at a time).
3. The contents of the A register are transferred to the B register (doubleword transfer).
4. Data or commands are gated, one byte at a time, from the B register to the SSC I/O interface.
5. Data or status is gated from the B register to the main channel (doublewords of data and two bytes of status).

Figure 2-22 is a logic drawing of byte 0 of the SSC A and B data registers. The CCW gate gates the command to byte 0. Input operation and data cycle are required to gate the bus in bits from the SSC I/O interface. Output operation and SSC selected are required to gate the channel data bus out (CDBO) bits to the A register. The A and B register positions are polarity hold (PH) devices. These devices are controlled by a gate line. When the gate is activated, the PHs follow their data inputs (released); when the gate is deactivated, the output is locked in its present status and is no longer affected by its data input.

Figure 2-23 is a logic drawing of byte 4 of the SSC A and B register. Byte 4 has special gating to permit control unit status to be gated during an I/O disconnect cycle (CSW).

Figure 2-24 is a logic drawing of byte 5 of the SSC A register. Byte 5 has special inputs and gating which permit the selector subchannel status to be gated into byte 5 for an I/O disconnect (CSW). Bytes 4 and 5 are sent to the main channel where the CSW is assembled.

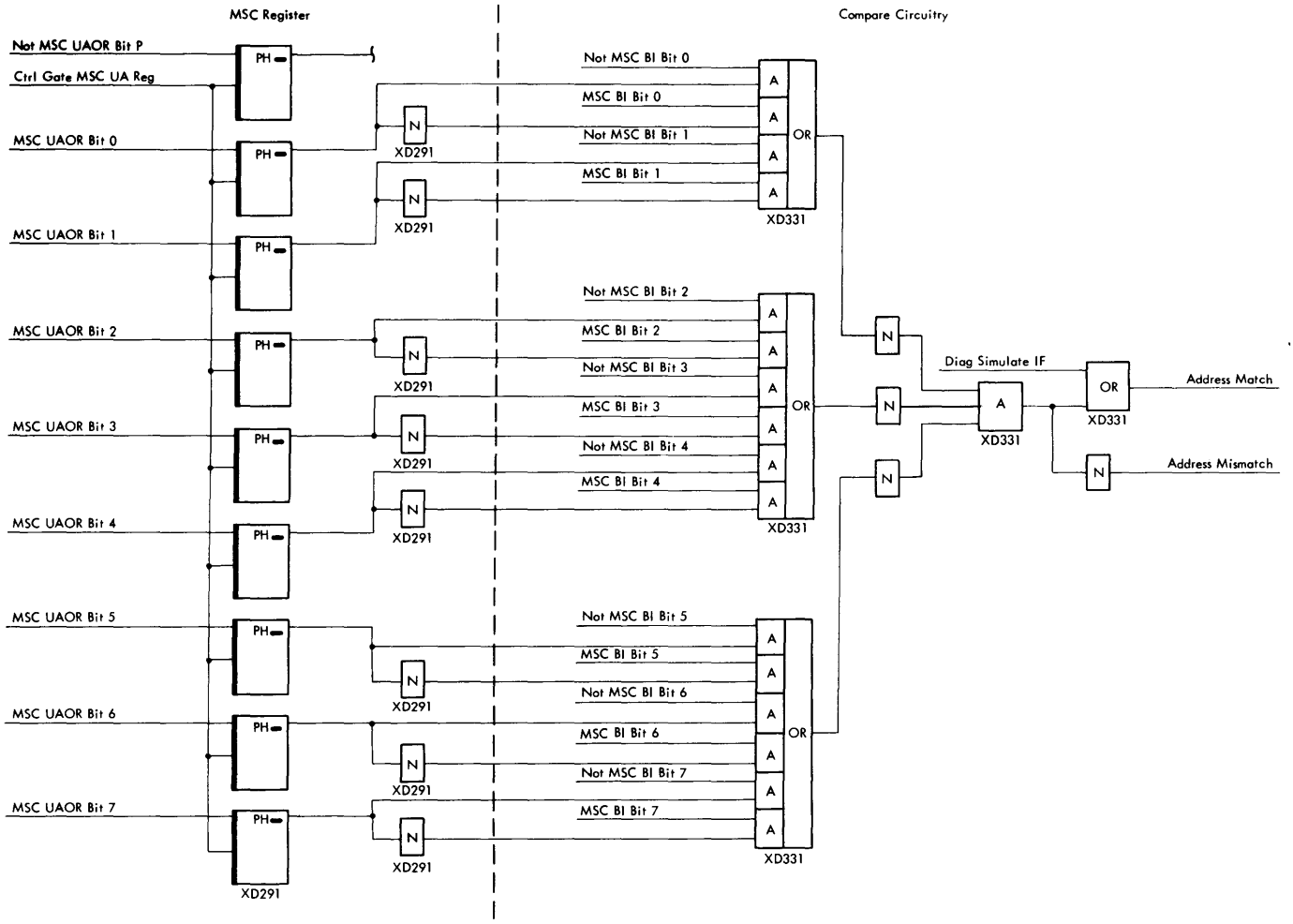


Figure 2-20. MSC Unit Address Register and Compare Circuits

SELECTOR SUBCHANNEL FLAG REGISTERS

Figure 2-25 is a logic drawing of the SSC A and B flag registers. CCW gate sets CCW bits 32-34 into the flag A register (CDA, CC, and SLI). The flag A register is gated to the flag B register when the byte count backup register is gated to the byte count latches on read chain data and channel bus out conditions or when the backup register is gated to main channel at the end of an operation.

SELECTOR SUBCHANNEL END COUNTER

- The SSC end counter holds the indication of the last byte to be transferred on a selector subchannel data transfer.
- The SSC end counter consists of the end count backup register and the end count register.
- Each selector subchannel has one end count register.
- An end count OR sends the end count to the main channel.

Figure 2-26 is a logic drawing of the SSC end counter. The CCW gate to the SSC sets CCW bits 61-63 in the end count backup register. The contents of the end count backup register are gated to the end count register. When the last word trigger is on, the contents of the end count register are compared

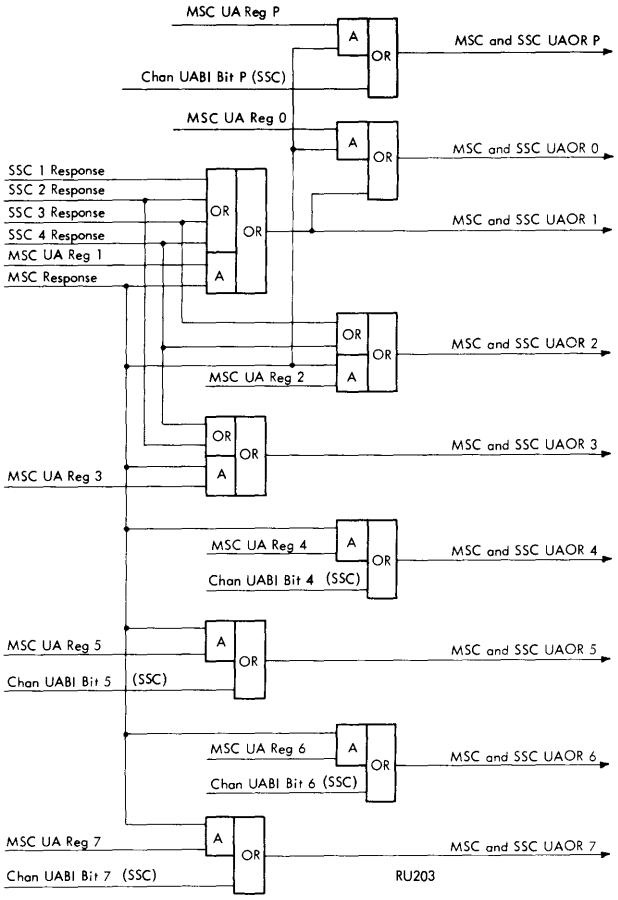


Figure 2-21. Subchannels Unit Address OR

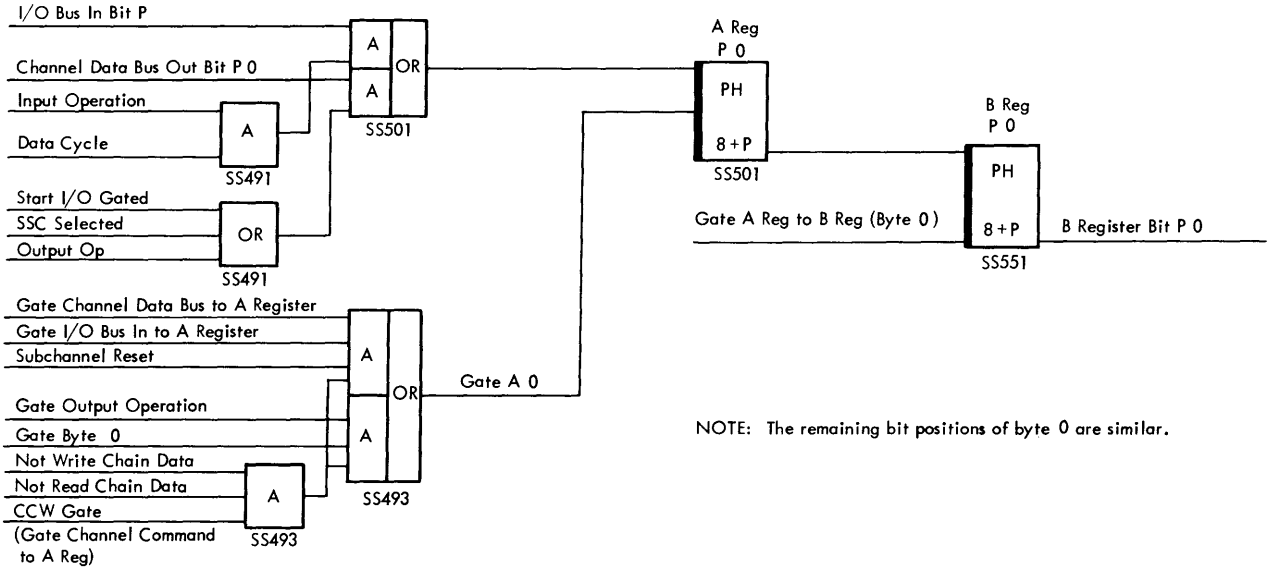


Figure 2-22. Selector Subchannel A and B Data Register Byte 0

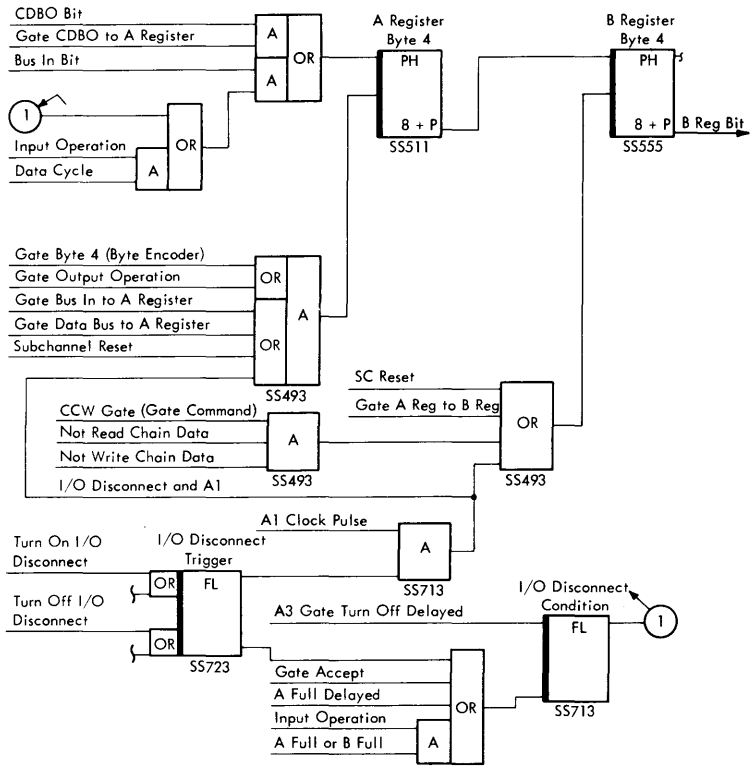


Figure 2-23. Selector Subchannel A and B Register Byte 4

with the byte count latches to determine the last byte of data to be transferred (byte count equals end count). If the operation ends prior to the byte count equals end count condition, the end count is transmitted to the main channel via the end count OR.

SELECTOR SUBCHANNEL BYTE COUNTER

- Contains three positions: 4, 2, and 1.
- Controls the gating of bytes into the A register or from the B register.
- During a read operation, it signals when the A register is full; during a write operation, it signals when the B register is empty.
- Increments on each data transfer.
- Consists of the byte count backup register, byte count latches, and byte count register.
- Each selector subchannel has a byte counter.

The selector subchannel uses the byte counter to control the transfer of data bytes. The byte counter controls which byte of a doubleword is to be transferred during a read or write operation. When the byte counter is at 0, the end of a doubleword is signaled. The byte counter starts at an initial value, advances one count for each byte transferred, and repeats its eight-count cycle as long as data is being transferred.

When the selector subchannel receives the CCW gate, the byte counter is initialized by transferring the three low-order bits of the data address from the main channel DAB register to the byte count backup register. These bits designate the location of a byte in a doubleword. All transfers between storage and the main channel D register and between the selector subchannel A or B register and the D register are doublewords. During initialization (CCW gate), the end count is loaded into the end count register to identify the end byte. The byte count and end count are compared to generate an end signal during the transfer of the last doubleword.

To signal the filling of the A register (read) or the emptying of the B register (write), the byte counter signals completion of a doubleword when it advances from 7 to 0. The A register full signal or B register empty signal causes a doubleword data transfer between the main channel D register and the selector subchannel A or B register. UCW 0 (for the device in operation) is read from local storage, the doubleword count and data address are updated, and UCW 0 is stored in local storage.

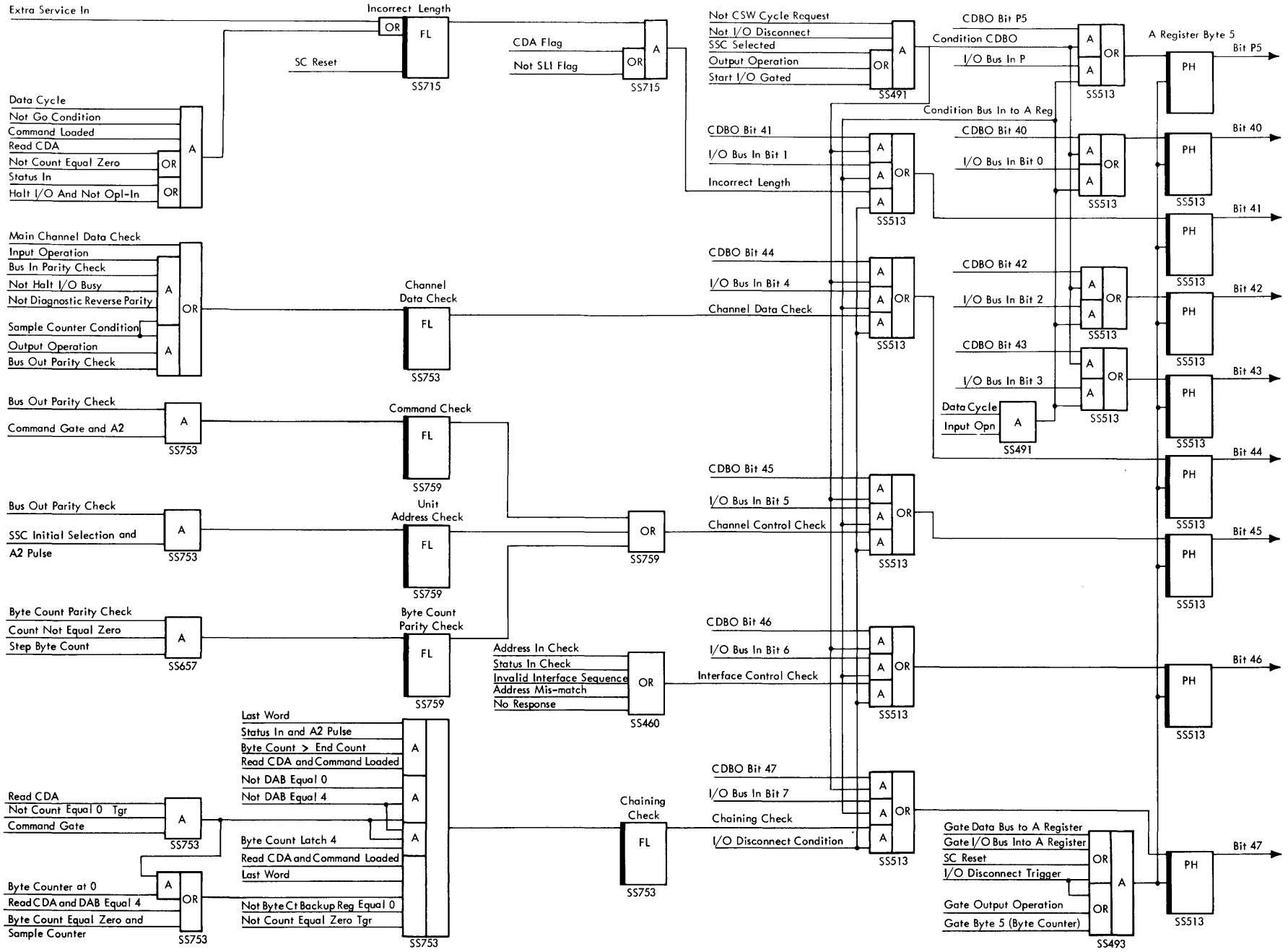


Figure 2-24. Selector Subchannel Status to A Register

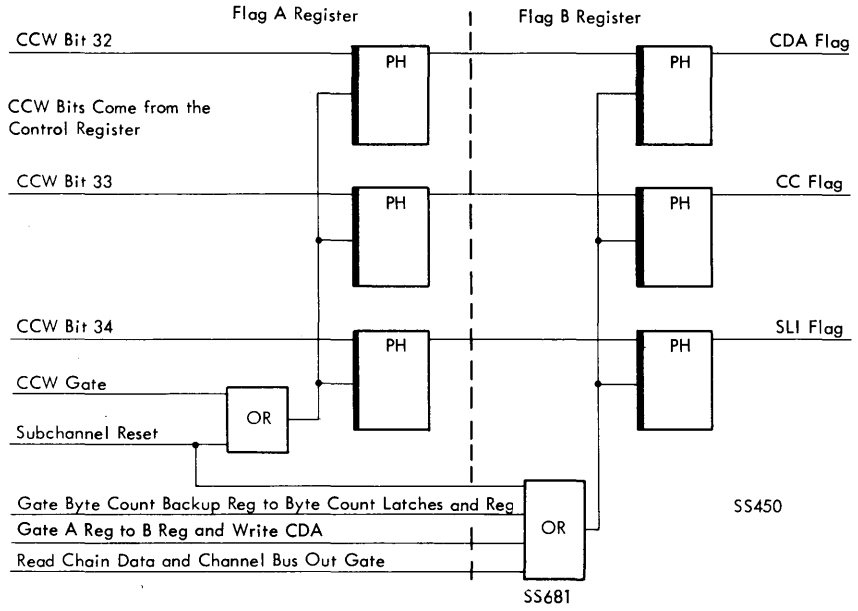


Figure 2-25. Selector Subchannel Flag Registers

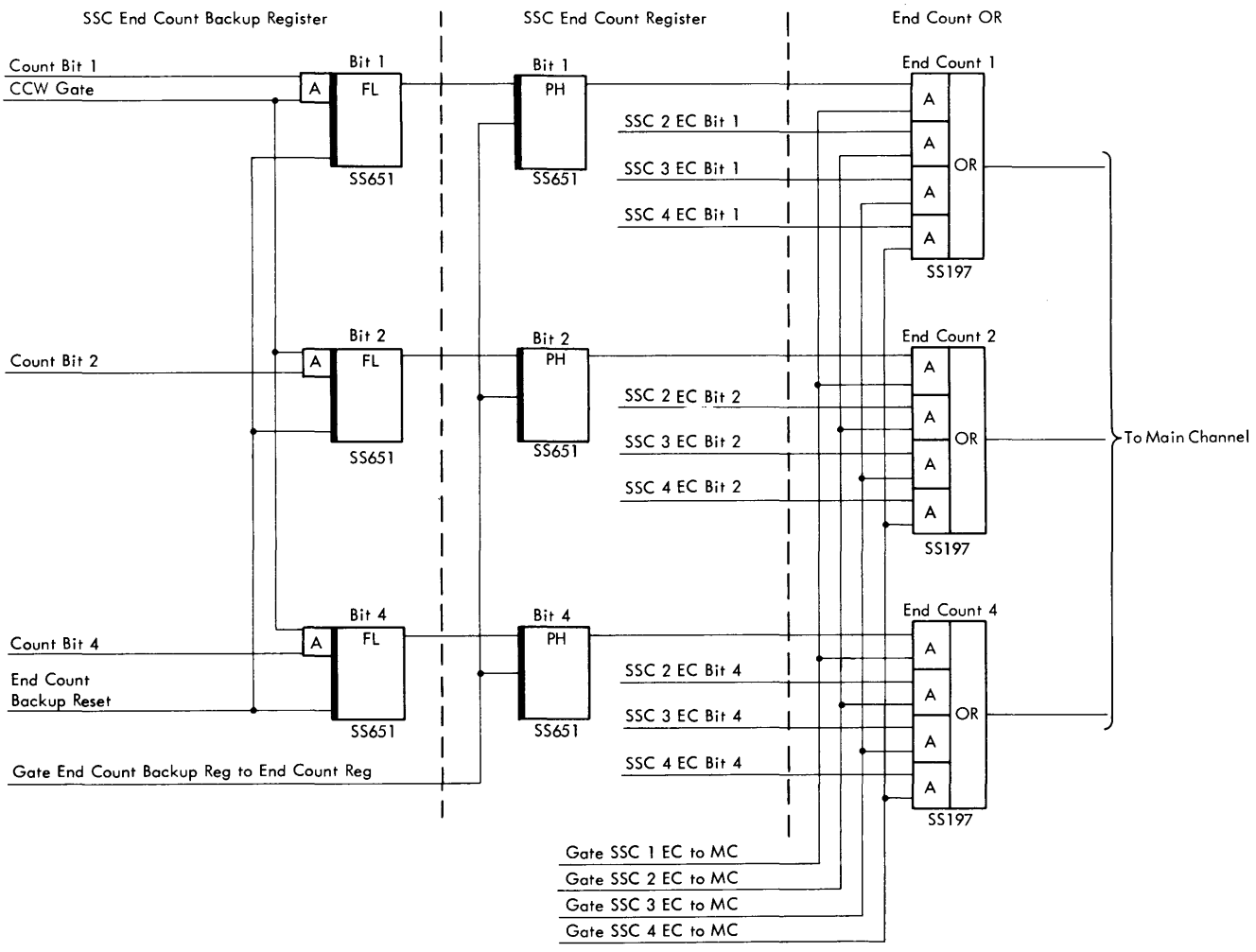


Figure 2-26. Selector Subchannel End Count

Byte Counter Operation

The detailed logic of the selector subchannel byte counter is shown in Figure 2-27 (sheet 2). The overall operation of the byte counter can be seen in Figure 2-27 (sheet 1). The three bits (29-31) of the DAB register are gated to the byte count backup register by the CCW gate to the selector subchannel. The parity bit, which is generated as the bits are transferred, provides an odd parity input to the backup register. The byte count is transferred to the byte count latches by 'gate byte count backup register to the byte count latches.' To gate bytes of data to or from the A or B register, the byte count latches are gated to the byte count register. Actual generation of the byte count gates is determined by the byte count encoder. To increment the byte counter, service in and service out generate the step byte count pulse. The step byte count pulse gates the byte count register to the byte count latches and increments the byte count register value by 1. When service in falls, the service out latch is reset and the byte count latches are gated to the byte count register; therefore, the byte count latches and the byte count register are equal except during step time.

INTERFACE DEFINITIONS

The electrical interconnections between any two areas, gates, or units are defined as an interface. The 2870 has the following interfaces: CPU, BCU, SSC, local storage, and I/O.

CPU Interface

The CPU interface with its associated controls is classified in four groups: operation lines, diagnostic lines, FLT controls, and CE aid lines (Figure 2-28).

Operation Lines

Operation lines provide the only control needed during normal program operation; in all modes they furnish information to the 2870.

Unit Address Bus Out (UABO): Nine multiplex lines (eight data and one parity) that transmit addresses from the CPU to the receivers in each channel. These lines are valid when the channel receives the select channel line, and they remain valid until the select channel line is dropped.

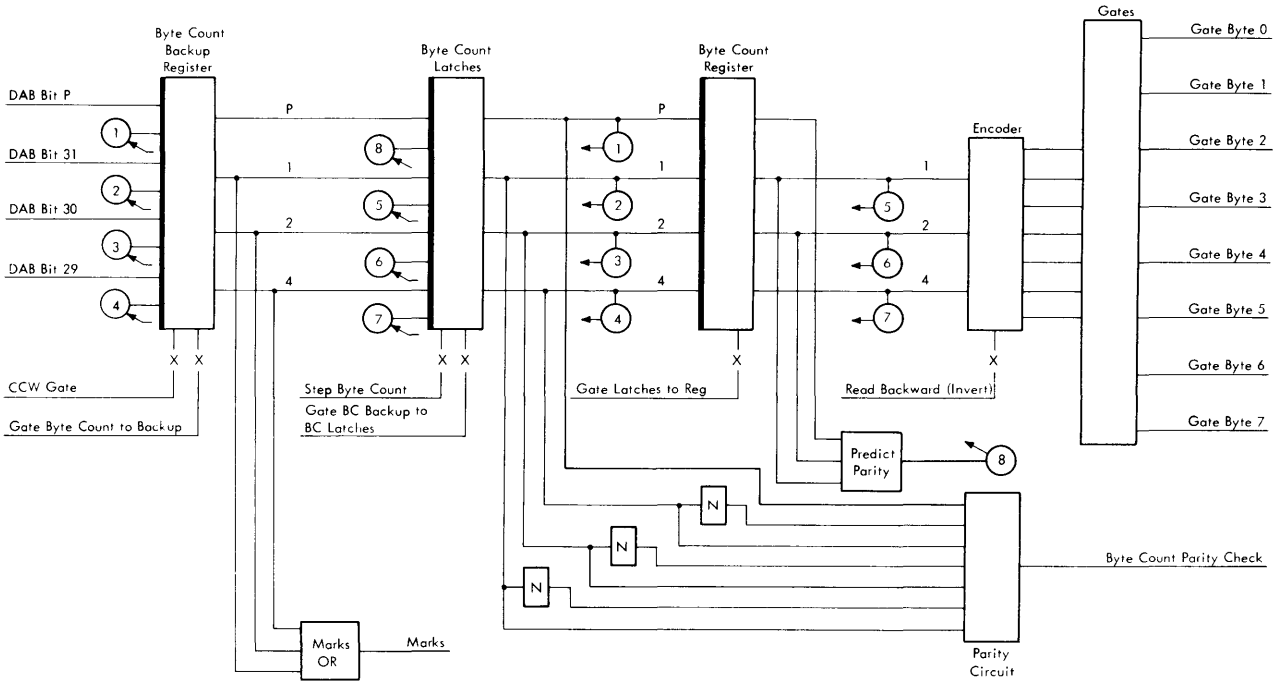


Figure 2-27. Selector Subchannel Byte Counter (Sheet 1 of 2)

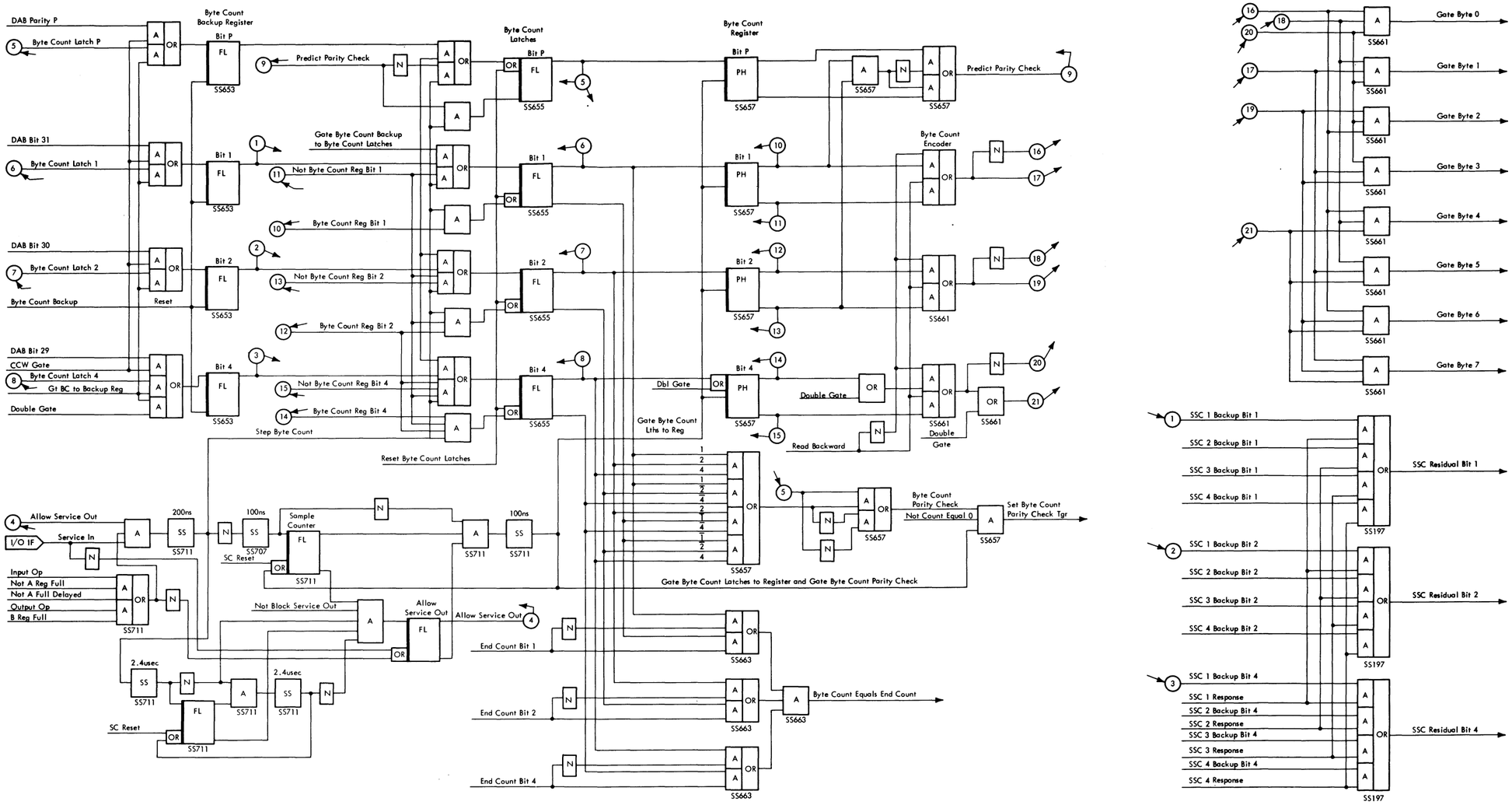
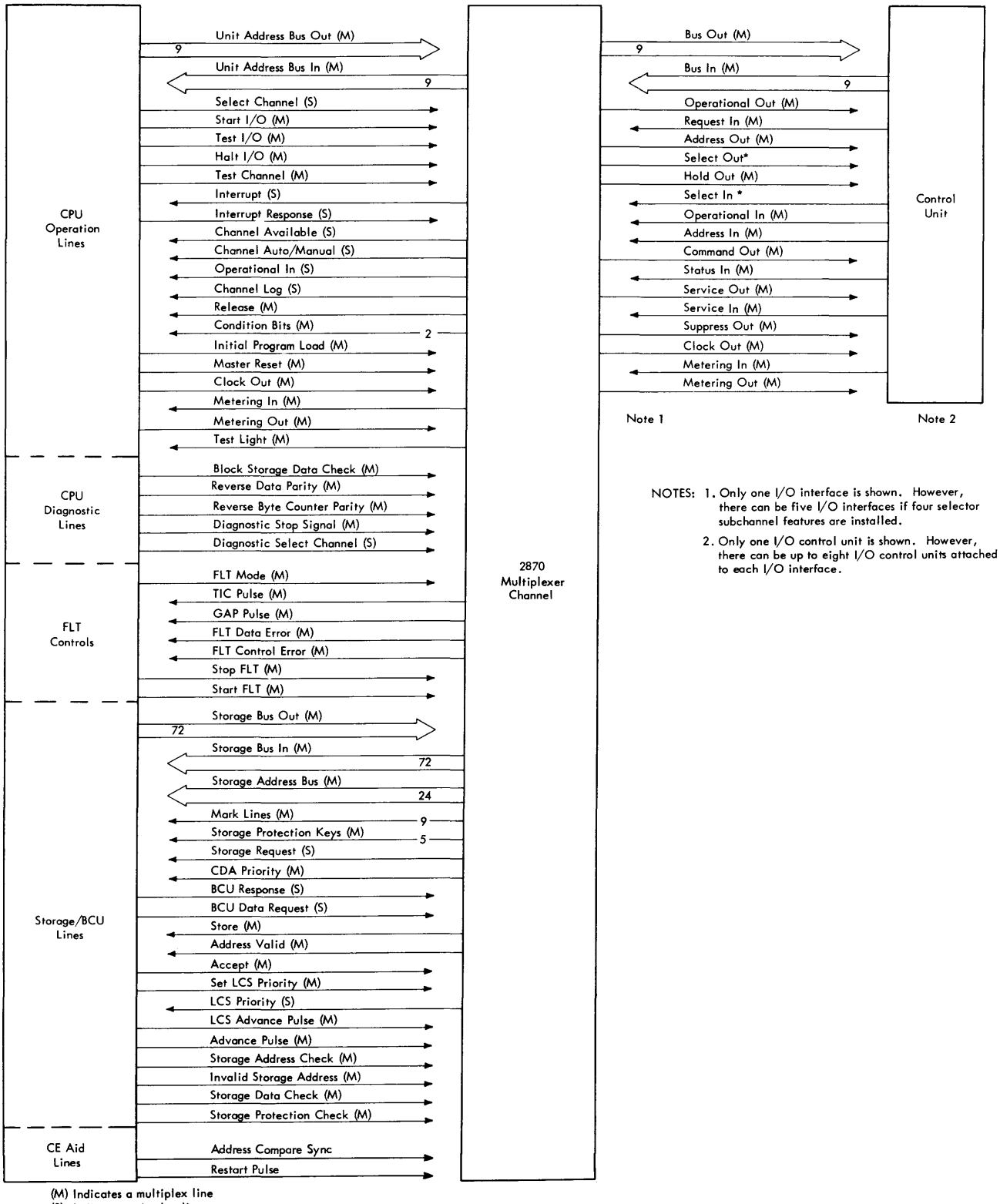


Figure 2-27. Selector Subchannel Byte Counter (Sheet 2 of 2)



NOTES: 1. Only one I/O interface is shown. However, there can be five I/O interfaces if four selector subchannel features are installed.

2. Only one I/O control unit is shown. However, there can be up to eight I/O control units attached to each I/O interface.

Figure 2-28. 2870 Multiplexer Channel Interface Lines

Unit Address Bus In (UABI): Nine multiplex lines (eight data and one parity) that transmit addresses from each channel to the CPU. These lines are valid when the CPU receives the release signal, terminating an interrupt signal from the CPU.

Select Channel: A single line from CPU to each channel. It is activated when the CPU initiates an IPL or an I/O instruction at a specific channel. This line remains active until the channel sends release.

Start I/O: One multiplex line from CPU to all channels that is activated as soon as select channel; it remains active until select channel is released.

Test I/O: Same as start I/O.

Halt I/O: Same as start I/O.

Test Channel: Same as start I/O.

Interrupt: Single channel-to-CPU line activated when an interruption condition is recognized by the channel. It remains active until the CPU recognizes it by sending an interruption response or until that subchannel is selected for a test I/O operation. If the interrupt was caused by a device presenting secondary status (status presented to an idle subchannel) and an instruction other than test channel is presented to that subchannel, then the interrupt condition is reset by the instruction response.

Interrupt Response: Single CPU-to-channel line activated on a priority basis to permit a channel to store its CSW, starting at Adr 64. It remains active until release is sent from the channel.

Channel Available: Single channel-to-CPU line activated when the channel is available to the CPU; consequently, the absence of this line indicates to the CPU that the channel does not exist, its power is down, or it is in test mode.

Channel Auto/Manual: Single channel-to-CPU line that turns on an indicator on the CPU CE panel when the channel is in automatic mode.

Operational In: Single channel-to-CPU line that turns on an indicator on the CPU CE panel when an I/O device has raised the operational in line on a channel I/O interface.

Channel Log: Single channel-to-CPU line that turns on an indicator on the CPU CE panel when the channel-log-on-machine-check switch is in the down position and the channel is in automatic mode.

Release: Multiplex line from each channel to the CPU. It terminates the communication between the CPU and the channel as follows:

1. Release ends instructions by signaling the CPU that the condition codes are valid and that the instruction may be terminated.
2. Interruption response release indicates that the channel has completed storing the CSW in the location starting at byte 64 and has reset its interrupt status.
3. Release responds to IPL when the IPL is completed and permits the CPU to fetch the PSW from storage address 0.

Condition Bits: Two multiplex lines that transmit condition codes from each channel to the CPU. These bits are valid when the CPU receives the release signal.

Initial Program Loading (IPL): Multiplex line from CPU to all channels. This line causes each channel to perform a master reset and the selected channel to perform the initial program load from the specified unit. The IPL signal overlaps the select channel signal. IPL is the only condition during which the multiplex subchannel forces the control unit to operate in burst mode. The selector subchannel feature always forces burst mode operation.

Master Reset: Multiplex line, from CPU to all channels, carrying a 2.2 ± 1.8 usec pulse that causes a complete channel, control unit, and device reset. All control units and devices are reset except those devices which are performing an operation without the control unit (e.g., a tape unit rewinding).

On CPU Stopped (Clock Out): Multiplex line from CPU to all channels that carries a signal indicating that the CPU is not in a halt or wait state. The channel may not change its enable or disable meter conditions at this time.

Metering In: Multiplex line from the channel to CPU that signals the CPU cluster clock that it should run as long as the signal is present.

CPU Clock Running: Multiplex line from CPU to all channels that is conditioned whenever the customer meter is running.

Test Light: Multiplex line from channel to CPU that is active whenever a channel is not set to perform a log-on-machine check.

Diagnostic Lines

The diagnostic lines are used by the CPU to determine the validity of the channel checking functions.

Block Storage Data Check: Multiplex line from CPU that:

1. Causes channel to block the setting of the control check or data check due to incorrect parity on a CCW or data fetched from main storage.
2. Blocks parity checking of the storage bus in lines.

This permits invalid CCWs or data to be brought into the channel to test sections of the channel test circuitry.

Reverse Data Parity: Multiplex line that operates with the diagnostic simulate interface function. It causes a reversal of the parity bit coming out of the simulate data register, thus allowing an invalid byte to be stored. This function also blocks a bus in parity check.

Reverse Byte Counter Parity: Multiplex line that allows a diagnostic program to test the 2870 local storage. The program has the ability to transfer data between main storage and the 2870 local storage.

Diagnostic Select Channel: Simplex line to the specific channel that is requested to respond to the preceding diagnostic lines. This line causes the 2870 to operate with the simulate I/O controls on all available interfaces.

Fault Locating Test (FLT) Controls

On the 2870, FLT's can be entered only through the selector subchannels. The FLT operation requires a large volume of data that is broken up into short tests. This data is on tape, and must be brought into storage without benefit of CPU instructions or interrupts. The channel must therefore work in conjunction with the FLT controls to supply the data, to notify the FLT controls of progress, to retry when data errors are discovered, and to start and stop transmission when so instructed by the FLT controls.

The following lines are used to control the 2870 when the CPU is performing fault locating tests:

FLT Mode: Multiplex line to all channels that indicates when the FLT controls are operative.

Transfer In Channel (TIC) Pulse: Multiplex line from the channel to FLT controls that carries a 350±30 ns pulse when a TIC command is encountered after the IPL latch is reset. This pulse indicates that a buffer has been filled.

Gap Pulse: Multiplex line from the channel to FLT controls that carries a minimum 1 usec pulse whenever an end of record is passed. This pulse does not occur if an error is detected in the record.

FLT Data Check: Multiplex line from the channel to FLT controls that rises when a control check, command reject, or exceptional condition is detected; it signals that the channel is unable to proceed.

Stop FLT: Multiplex line from FLT controls to the channels. This line carries a 250 ± 50 ns pulse that commands the operating channel to stop transmission of data to storage and wait. The tape proceeds to the end-of-record and is deselected, then reselected. Interface operations stop with the SSC waiting for the command loaded latch to be set. Command loaded is set after start FLT is issued.

Start FLT: Multiplex line from FLT controls to the channels. This line carries a 250 ± 50 ns pulse that commands the selected channel to restart transmission of data to storage. The channel fetches the command at location 128 and continues; this causes the restart always to begin at the front of the block that was transmitting at the time stop FLT was received. If the stop is received during an error backspace, the backspace is concluded and an ensuing start FLT goes to the read command that loads buffer 1.

CE Aids

The following lines are included in the 2870 CPU interface to aid the customer engineer in trouble-shooting channel problems.

Address Compare Sync Pulse: Line carrying a minimum 200 ns pulse to the channel whenever the address sent from channel to BCU during a storage request matches the address set in the switches on the CPU console.

Time Clock Step Pulse: Line carrying a minimum 200 ns pulse to the channel every 16.7 ms (60 hertz) or at line frequency.

Storage or Bus Control Unit Interface

The storage interface carries the data and control information necessary to the channel when the channel operates independent of the CPU.

Storage Bus Out: Seventy-two multiplex lines (64 data and 8 parity) from storage to all channels. After the BCU response and accept lines fall and approximately 200 ns after advance rises, the storage bus out lines become active.

Storage Bus In (SBI): Seventy-two multiplex lines (64 data and 8 parity) that transmit data from the channel to storage. They are activated when the channel recognizes BCU data request, and they remain active until BCU data request falls.

Storage Address Bus (SAB): Twenty-four multiplex lines (21 data and 3 parity) transmit addresses from the channel to storage and/or BCU. They are activated when the channel recognizes BCU response, and they remain active until BCU response falls.

Mark Lines: Nine multiplex lines (eight data and one parity) from the channel to storage that respond the same as the SAB lines. These lines, when active, indicate which of the eight data bytes are to be stored when the channel is performing a store operation.

Protection Key: Five multiplex lines (four data and one parity) from the channel to storage that remain active with the SAB lines. These lines carry the storage protection information.

Storage Request: Single line from each channel to the BCU that requests priority for a storage cycle. It falls when the channel recognizes the BCU data request.

Chain Data Priority: Multiplex line from the channel to the BCU that eliminates CPU interferences on systems that do assign absolute priority to channels.

Bus Control Unit (BCU) Response: Single line from BCU to channel. It rises when the BCU grants priority to a particular channel and is requesting an address on SAB. This line remains active under BCU control as long as SAB requires an address.

Address Valid: Multiplex line from channels to BCU that indicates to the BCU that the address on the storage address bus is valid. This signal falls after the expiration of BCU response.

Store: Multiplex line from channels to BCU. It rises with the address on the storage address bus and indicates that the channel is performing a store operation.

Accept: Multiplex line from BCU to channels that notifies the channel that originated the storage request that the storage cycle has been started, and that the next advance pulse pertains to that request.

Set Large Capacity Storage (LCS) Priority: Multiplex line from BCU to channels that indicates that the BCU has decoded an address existent in large capacity storage. This causes the requesting channel to set the LCS priority latch. The line is ignored by systems that do not use large capacity storage.

Large Capacity Storage (LCS) Priority: Simplex line from each channel to the BCU to notify the BCU that the channel has an outstanding request to a location existing in large capacity storage. This line is ignored by systems not connected to large capacity storage.

Large Capacity Storage (LCS) Advance Pulse: Multiplex line from storage that carries a 240±60 ns pulse that precedes the data to the proper channel by approximately 200 ns. This line is necessary only when large capacity storage is attached.

Advance Pulse: Multiplex line from storage to the channel that carries a 240±60 ns pulse that precedes the data to the proper channel by approximately 200 ns.

Storage Address Check: Multiplex line that indicates that BCU or storage has detected a parity error on the address marks, or key received. The error pulse sent to the channel overlaps the raw advance pulse sent from storage.

Invalid Storage Address: Multiplex line that indicates that BCU has detected a nonexistent address on the storage address bus lines from the channel. The error pulse sent to the channel overlaps the raw advance pulse sent from storage.

Storage Data Check: Multiplex line from storage to the channels that indicates a data parity error has been detected in the information sent to storage

during a store operation, or in information coming from storage during a fetch operation. This pulse rises approximately 370 ns after the advance pulse.

Storage Protection Check: Multiplex line from storage to the channel indicating that the channel attempted to store information in a protected area. The error pulse sent to the channel overlaps the raw advance pulse.

Selector Subchannel to Main Channel Interface

Communication between the selector subchannels and the main channel occurs over shared signal lines (Figure 2-29). These lines are time-shared by as many as four selector subchannels.

Channel Data Bus In (CDBI): 72-bit bus that is the data path from the four selector subchannels to the main channel. Data is transferred from selector subchannel B register to CPU main storage via the CDBI and the main channel data register. The channel data bus sends status information (bit positions 32-47) to local storage during a CSW cycle, and sends a status modifier bit to the main channel during a chain command cycle. The parity of bits 32-39 is not defined during status presentations.

Channel Unit Address Bus In: Bus carrying the four low-order bits (4-7 plus parity) of the unit address. These four bits and the response gate form the entire unit address byte, which is used by the main channel to address the proper local storage location. During a test I/O, the unit address is gated to the main channel for address comparison if an interruption condition is pending in the selector subchannel.

Residual Byte Count: Bus used during input operations as an entry to the mark encoder to activate the correct mark lines to main storage. During a CSW cycle, the residual byte count bits are used to form the residual count if an incorrect length condition exists.

Residual Count 16: Line used during a CSW cycle to form a residual count, if one exists. When the selector subchannel is informed that the count has been reduced to 16 bytes or less, the count is no longer retained in local storage. Therefore, the selector subchannel must recover this count if a CSW cycle is performed.

Residual Count 8: Line used to form residual counts greater than 8 bytes and less than 16 bytes.

End Count: Bus onto which are gated the contents of the end count register whenever a selector subchannel is serviced. Prefetching of a new command on a write chain data (CDA) operation results in the loss of the residual count in local storage for the current operating command. If the current operation is terminated before the count reaches 0, the contents of the end count register and the residual byte count are subtracted in the main channel to form the entire residual count.

Inhibit Decrement Control: Line active to main channel during initial main storage data fetches for a write operation. It blocks decrementing of the count (in UCW 0) when the two initial double words of data are buffered in the SSC. The result is a main channel count which represents the actual number of bytes transferred across the I/O interface.

Inhibit Program Check: Line that signals main channel to suppress any invalid address or protection check condition associated with the fetching of new data or commands for the selector subchannel.

Accept: Line that signals main channel that an I/O selection for either a start I/O or test I/O instruction has been executed successfully. Accept indicates receipt of satisfactory status from the I/O unit and that the CPU can be released with condition code 00. Accept also indicates to the main channel that an interruption is pending in the selector subchannel at the time a halt I/O instruction is issued to the selector subchannel. A priority response is not required to gate accept.

No Selection: Line that signals main channel that no unit responded to an attempt to address an I/O device during a SIO, TIO, or HIO selection process. The main channel releases the CPU with condition code 11. A priority response is not required to gate no selection.

Chain Data Control: Line used during a CSW cycle to signal main channel to use the residual command address field of UCW 2 rather than the new command address.

New CCW: Line that signals main channel during a data cycle that the selector subchannel is in a chain data condition and needs the new flags, initial byte count, and end count (from the new CCW).

CSW Cycle: Line that signals main channel that the current cycle requires the storing of a CSW (in local storage) and that bits 32-47 of the CDBI represent status information.

Chain Command Cycle: Line that signals main channel that the current cycle is a request for a new command.

Interrupt Cycle: Line that signals main channel that the current cycle requires the main channel to read out the CSW (associated with the subchannel) from local storage to main storage. The unit address is gated to the CPU, and the CPU is released.

Interrupt Request: Line active to main channel when an interruption is pending in a selector subchannel. The main channel uses subchannel interrupt request to signal the CPU that an interruption is pending in the channel. Interrupt request is dropped when the CPU clears the interruption.

Busy: Line active from the time a selection process for an operation is initiated until the interruption condition for the operation is cleared. The main channel tests for a busy selector subchannel by sampling the busy line.

SSC Primary Priority Request (Data): Line raised by an SSC when it must transfer a doubleword of data to or from main storage during an I/O operation. This line is not used when the SSC initializes the A and B register for a write operation.

SSC Secondary Priority Request (CCW): Line raised by an SSC when it requires main channel to:

1. Fetch a new CCW for a chain command operation (SSC pseudo start I/O).
2. Assemble a CSW (trigger 5-6, 7).
3. Fetch one or two doublewords of data to initialize the A and B registers prior to responding to the initial status-in signal (with service out) for a start I/O or chain command operation.

Metering Condition: Line that signals main channel that a selector subchannel or I/O unit is busy and that the metering circuits must remain active.

Log Condition: Signal that indicates that a control check condition exists in the selector subchannel and the current CSW cycle must be preceded by a log into local storage routine.

SSC Request and Selected: Line that signals main channel that a CSW must be assembled under trigger 7. This line is active if a non-zero status byte is returned during an initial selection sequence (SSC selected and CSW cycle gate).

SSC Installed: Signals the main channel address decoder that this SSC is installed.

SSC Stopped: Signals main channel that the SSC stopped because a check condition occurred with the enable stop line active. When this condition occurs, the 2870 stops all operations without resetting any indicators (however, memory cycles already in process are allowed to finish).

Operational In: Signals main channel that SSCs operational in line is active. This line is ORed with the other operational in lines (SSC and MSC) and the result is sent to CPU.

Data Cycle: Signals main channel that the SSCs priority request is active for a data transfer sequence. The main channel trigger 1 sequence performs the data transfer.

Control Unit Interrupt Accept: Signals main channel that CPU response is active and that this SSC has a control unit interrupt pending. The main channel trigger 7 sequence assembles a CSW and stores it in main storage.

Address in Check: Signals main channel that a bus-in parity check occurred when the control unit presented its address on bus in. Main channel turns on the pseudo log 1 latch and the pseudo log sequence is performed.

Main Channel to Selector Subchannel Interface

This signal interface utilizes both levels (L) and pulses (P) to transfer information from the main channel to the selector subchannels (Figure 2-30).

Channel Data Bus Out (CDBO) (L): 72-bit bus that transmits data to the four selector subchannels. Data for output operations is transferred on this bus. Byte 0 of this bus sends the command byte for either an SIO or chain command to the selector subchannels.

Channel Unit Address Bus Out (L): Bus that sends the four low-order bits (4-7) and the parity bit of the unit address to the selector subchannels during operations initiated by the CPU. These bits are set in the unit address register in the selector subchannel and are used by the SSC to address the I/O interface.

Data Address Byte (DAB) Bus (L): This three-bit bus is used by the main channel to initialize the byte counter of the selector subchannel. In the SSC, these bits are gated to the byte count backup register and then to the byte counter. The DAB establishes the starting byte position for I/O operations.

Count Bus (L): Three-bit bus used by selector subchannel to receive the end byte count for I/O operations. The end byte count is a result of the addition of the initial three low-order bits of the count field and the DAB. The resulting end count is gated into the end count backup register and then to the end count register. The end count is used by the selector subchannel to determine when the current count is exhausted (byte count equal to end count on last word).

Flag Bus (L): Three-bit bus that sends the chain data (CD), chain command (CC), and suppress length indication (SLI) flag bits to the selector subchannels. The flag bits are gated to the flag backup register and then to the flag register.

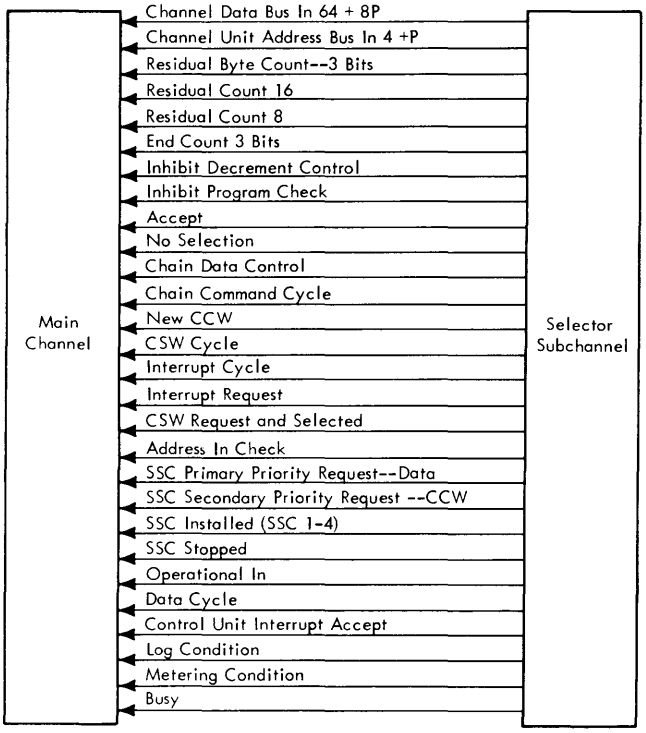


Figure 2-29. Selector Subchannel to Main Channel Interface

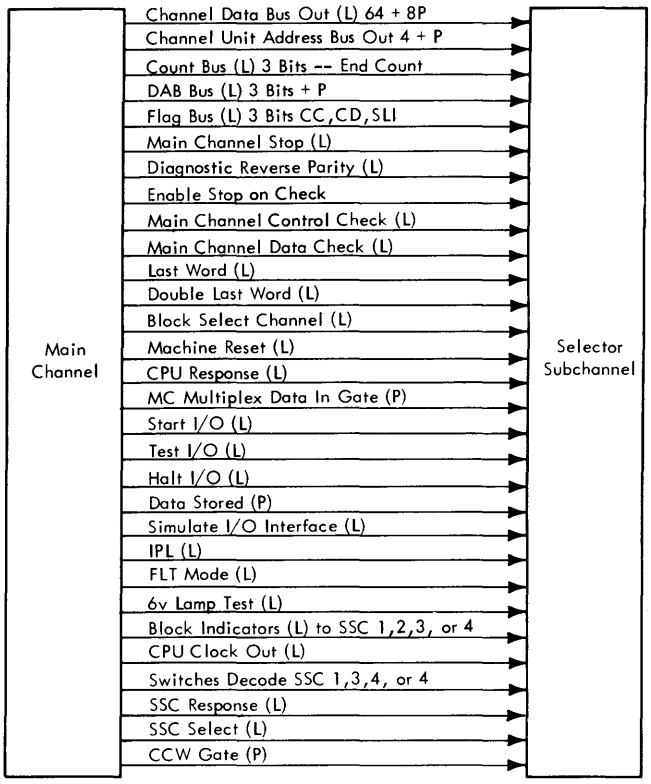


Figure 2-30. Main Channel to Selector Subchannel Interface

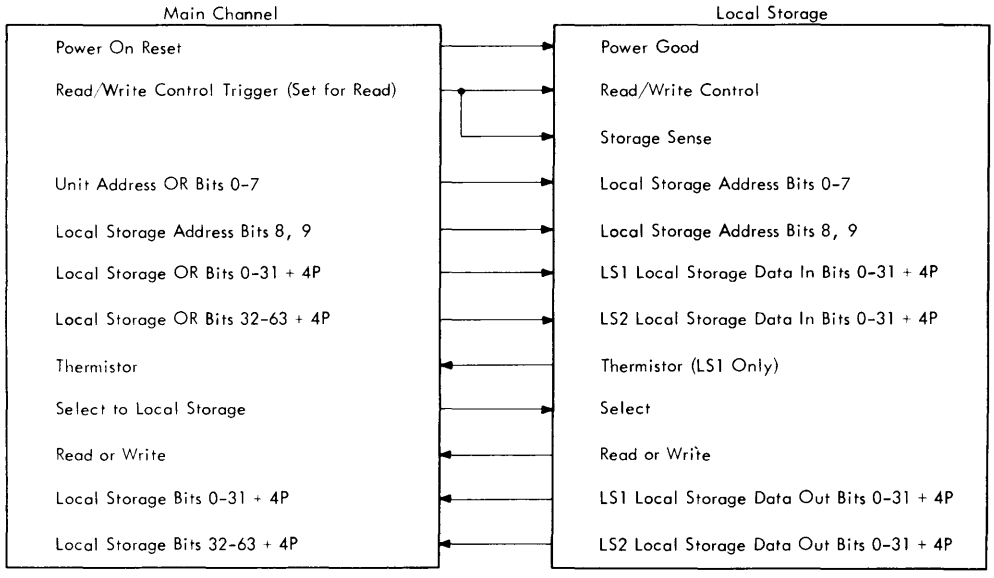


Figure 2-31. Local Storage to Main Channel Interface

Last Word (L): Sent to selector subchannels during data or CCW cycles whenever the major count is reduced to eight bytes or less. This condition is retained in the pre-last word latch of the selector subchannel and is gated to the last word (LW) latch. The basic function of the last word latch is to determine when the count for the current operation is reduced to 0.

Double Last Word (DBLW) (L): Sent to selector subchannels during data or CCW cycles whenever the major count is reduced to 16 bytes or less but is greater than 8 bytes. This condition is retained in the double last word (DBLW) latch of the selector subchannel and is gated to the last word latch.

Main Channel Control Check (L): Sent to selector subchannels during data or CCW cycles if a program or control check condition is detected in the main channel.

Main Channel Data Check (L): Signal sent to selector subchannel being serviced if a data check condition is detected in the main channel. This condition is retained in the selector subchannel and returned to the main channel during the CSW cycle associated with the current operation.

Data Stored (P): Signal that indicates to selector subchannel that the data sent to the main channel has been accepted. The selector subchannel uses this signal to gate various signal levels which are present on the common bus (LW, DBLW, or MC Control Check).

MC Multiplex Data In Gate (P): Signal that indicates to selector subchannel that data is present on the CDBO. The selector subchannel uses the pulse to activate the main control gate of the selector subchannel A register exclusive OR latches.

CPU Response (L): Signal sent from main channel to all subchannels. Any subchannel with an interruption pending now vies for servicing via the priority network. The subchannel with the highest priority has its CSW placed in main storage, which clears the interruption condition for that subchannel. The CPU response signal drops when the CPU receives a release signal from the main channel.

SSC Response (L): Line to each selector subchannel from the main channel priority network. The response signal indicates to the selector subchannel that its request for servicing is being honored and that any signals from main channel apply to this SSC.

CCW Gate (P): Single line to each selector subchannel that permits portions of the CCW (flags, byte count, end count, and command) to be gated to the appropriate registers. The setting of these registers is signaled in the selector subchannel by the setting of the command loaded latch.

Selector Subchannel Select (L): Signal that indicates to selector subchannel that it is being selected for the execution of an instruction.

Start I/O (L): Line that signals a start I/O instruction to the addressed selector subchannel.

Test I/O (L): Line that signals a test I/O instruction to the addressed selector subchannel.

Halt I/O (L): Line that signals a halt I/O instruction to the addressed selector subchannel.

Initial Program Load (IPL) (L): Signal used by selector subchannel that is executing an IPL operation to suppress the end interruption condition.

FLT Mode (L): Signal that places the addressed selector subchannel in FLT mode. The selector subchannel uses the FLT mode signal to suppress data checks and incorrect length indications and to force execution of command chaining.

Simulate I/O Interface (L): Signal that causes an addressed selector subchannel to execute instructions to a simulated I/O device; it causes all nonselected subchannels to appear busy to the main channel.

Diagnostic Reverse Parity (L): Signal that, if present, causes selector subchannel operating in the I/O simulation mode to reverse data parity and suppress data checks.

Machine Reset: Signal that causes all the selector subchannels to execute a master reset of all registers, latches, I/O control units, and devices.

CPU Clock Out (L): Line that indicates to the selector subchannel that the metering circuit of the channel is active. This indication is transmitted from the selector subchannel to the I/O interface. The clock running signal is used by the I/O control units to keep the meters running.

Block Select Channel: Causes the SSC to perform an interface reset by dropping operational out. Block select channel is activated by a machine reset or a master reset.

Enable Stop On Check: Signals the SSC to stop (without a logout) if a machine check or a data check occurs. Active when the log-on-machine-check switch is down and the auto/test switch is in the

test position, or when the CE stop-on-check-circuit pin (01A-B4C5D02) is wired.

Main Channel Stop (L): Signals the SSC that a check condition occurred in the 2870 when 'enable stop on check' was active. The check condition can be a data check, a machine check, a SSC or MSC stopped condition, or some condition wired into the test circuit (pin 01A-C3K4D04) by a CE.

6v Lamp Test (L): Activated by the test indicators pushbutton. The SSC simulate I/O register indicators are tested by the line.

Switch Decode SSC 1, 2, 3, or 4 (L): Four lines that are the decoded outputs of the SSC display switches (unit address switches 2 and 3). One of these lines is always active and causes the indicators in rows H and J to display the status of the addressed SSC. However, a logout condition for an SSC overrides the switch decode, and the SSC being logged is displayed in rows H and J.

Block Indicators SSC 1, 2, 3, or 4 (L): Four lines us used to override the SSC display switches when an SSC is in logout condition. The block indicator lines are made active to all but the SSC being logged, and the SSC being logged is displayed in rows H and J of the CE panel.

Local Storage Interface

Data is transferred to and from local storage via the local storage interface. This interface provides data and control lines between the main channel and local storage (Figure 2-31).

Power Good: Line from main channel to local storage that permits the local storage read/write gates to be generated. Power good is down, while power is being raised, until all voltages are within specifications. This line is dropped before power is dropped.

Read/Write Control: Line from main channel to local storage that causes local storage to read out data.

Storage Sense: Line from main channel to local storage that permits the generation of the local storage strobe pulse. Storage sense and read/write control are activated by the read/write control trigger in the main channel.

Local Storage Address Bits: Ten lines from main channel to local storage that determine the local storage address for a read/write operation. In the main channel, bits 0-7 are labeled "unit address OR bits," bits 8 and 9 are labeled "local storage address bits."

Local Storage Data-In Bits: 36 bits (32 bits plus 4 parity bits) that provide data to each local storage unit. Local storage OR bits 0-31 (plus 4 parity bits) are read into local storage unit 1 (LS1) bits 0-36, and local storage OR bits 32-63 (plus 4 parity bits) are read into local storage unit 2 (LS2) bits 0-36.

Thermistor: Lines from each local storage unit to main channel that carry the output of a thermistor in each array. The output from the thermistor in LS1 controls the temperature-compensated power supply.

Select: Line from main channel to local storage that signals local storage that the main channel is initiating a read/write cycle.

Read/Write: Line from local storage to main channel that is active when local storage is performing a read/write operation.

Local Storage Data Out Bits: 36 lines (bits 0-31 plus 4 parity bits) from each local storage to main channel that carry data from local storage to the main channel. LS1 data-out bits become local storage bits 0-31 (plus 4 parity bits), and LS2 data-out bits become local storage bits 32-63 (plus 4 parity bits).

CHAPTER 3. PRINCIPLES OF OPERATION

This chapter describes the operations of the 2870. Operations are grouped as: basic 2870 operations, I/O instructions, and I/O operations.

The basic 2870 operations group includes 2870-to-main storage operations, main channel trigger sequences, and the I/O interface device service request sequence. These operations are used during the execution of I/O operations as parts of the execution sequence. For example, a start I/O instruction from CPU uses the main storage sequence to fetch the CAW, CCW, and any data needed for a write type operation. The execution of the I/O operation began by start I/O is performed through the use of the trigger sequences and the main storage sequence. For multiplex devices, the device service request sequence is used to select the device each time it desires to transfer data or status.

The I/O instructions and I/O operations descriptions are grouped together by the type of subchannel for which they are performed. The multiplex subchannel start I/O, halt I/O, test I/O, read/write and chaining sequences are all in one group, and the same operations for the selector subchannels are in a separate group.

As a review, Figure 3-1 presents a simplified data flow for both the multiplex and selector subchannels. The diagram shows the flow of data and control information between the principal registers in the 2870. Also shown are the size of the data transfers between the various registers within the 2870, and the size of the data transfers from the 2870 to main storage and the I/O devices. For example, doublewords of data come from the main storage via the SDBO to the data register and are gated from the data register to the SSC A registers, or if the data is for a multiplex subchannel, to the local storage until needed. When needed by a multiplex subchannel, the doubleword of data is gated from local storage to the data register, and from the data register one byte at a time to the MSC I/O bus out via the multiplex data transfer logic. To control I/O operations, the 2870 fetches the CAW and CCWs from main storage. The main storage to 2870 transfer path is again the SDBO to the data register, but the control information is gated from the data register to the control register when it is modified to a format the 2870 can use. After modification, the control information is stored in local storage until needed by the subchannel. When a subchannel needs its control words, they are read from local storage to the control register where they are used to control the subchannel's operations.

MAIN STORAGE OPERATIONS

- Main storage operations begin when the 2870 raises storage request to BCU.
- BCU signals the 2870 to proceed with the storage operation by raising the BCU response line.
- 'BCU response' causes the 2870 to send the main storage address and the storage protect key to BCU.
- 'BCU data request' signals the 2870 to send the data and mark bits to BCU for a store operation.
- 'Accept' from BCU signals the 2870 that data is accepted for a store operation or is coming for a fetch operation.
- 'Advance' from BCU causes the 2870 to ingate the data from the storage bus out.
- To control operations in the 2870, 'storage cycle' and 'storage cycle over' are generated during the main storage sequence.
- FC551.

The 2870 performs two types of main storage operations: fetch and store. A fetch from main storage is performed to fetch CAWs for start I/O operations, fetch CCWs to control channel operations, and fetch data for write data transfers to I/O devices. A store into main storage is performed to store data read into the 2870 for read or read backward operations, store CSWs formed by the 2870, and to store log words formed by the 2870 due to an error condition. Both fetches and stores are initiated in the same manner. The difference between fetches and stores is that store operations are identified by the store signal to BCU, and the fetch or not store operation causes BCU to send data from main storage.

All main storage operations are initiated at the 2870's request. The 2870 requests BCU priority for a main storage cycle by raising the storage request line. When BCU determines that the 2870 can have priority, it raises 'BCU response' to the 2870. The 2870 then proceeds to execute a store or fetch operation.

The timing chart in Figure 3-2 shows the sequence of operations for both stores and fetches.

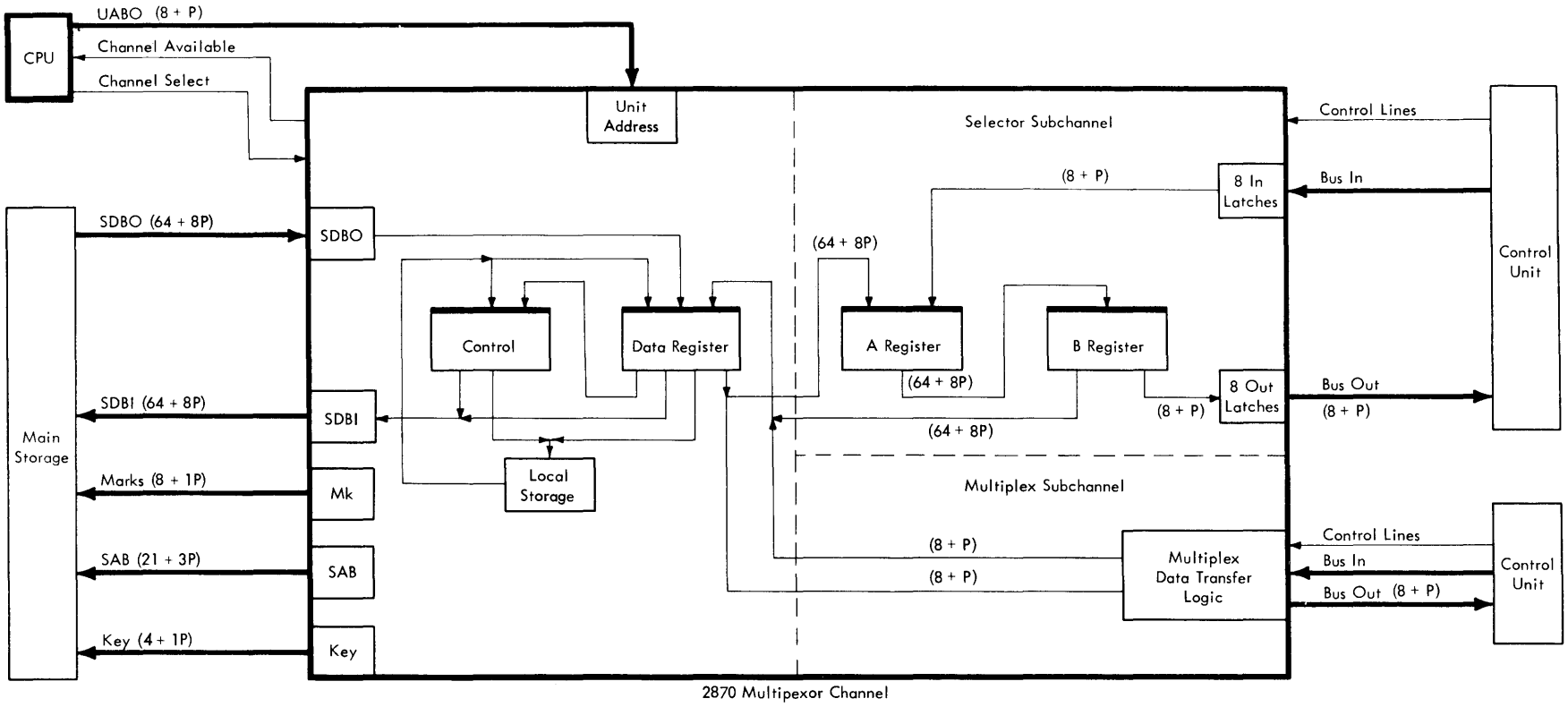


Figure 3-1. Multiplexer Channel Data Flow

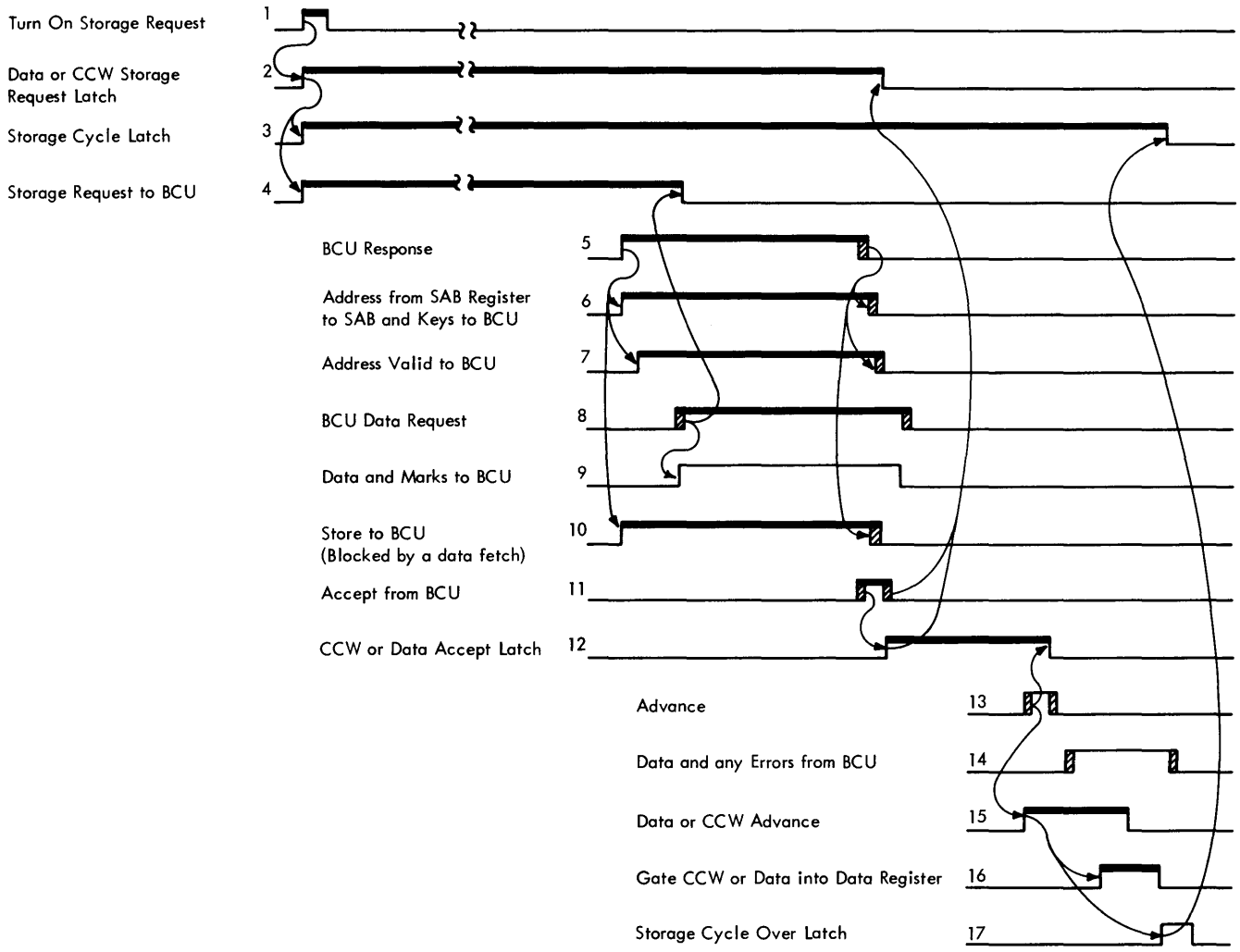


Figure 3-2. Main Storage Timing Sequence

(In the following text, numbers in parentheses refer to Figure 3-2.) Definitions of the storage interface lines are in the Storage or Bus Control Unit Interface section of Chapter 2. To begin the store or fetch operation, some main channel sequence needs to fetch data from or store data into main storage and turns on a storage request latch (1). There are two storage request latches: CCW and data (2). The CCW request latch is used when the 2870 needs to fetch a CAW or CCW from main storage. The data cycle request latch is used when the 2870 needs to fetch or store data, store CSWs, or store log words. The setting of either latch causes the 2870 to raise 'storage request' to the BCU (4), and sets the storage cycle latch in main channel (3). 'Storage request' indicates to the BCU that the 2870 requires priority for a main storage cycle. 'Storage cycle' is used by main channel to block operations that depend on the data being either stored or fetched. This is done because the main channel usually starts a main storage cycle by turning on a request latch and then proceeding with other parts of its operation.

When the BCU assigns priority to the 2870, it signals the 2870 with the 'BCU response' line (5). 'BCU response' causes the 2870 to gate the storage address from the SAB register to the SAB (6), send the storage protection key to BCU (6), raise 'address valid' to BCU (7), and raise the store line to BCU if this is a store operation (10). The storage address and protection keys were loaded into the SAB and keys registers before main channel raised 'storage request.' 'Address valid' signals the BCU

that the address and key bits on the buses are valid. 'Store' is turned on if this operation is a store (CSW, data, log words).

At some time after the BCU sends 'BCU response,' it sends 'BCU data request' (8). 'BCU data request' causes the 2870 to drop its storage request line to BCU. The BCU data request line is raised for both fetches and stores. In a store operation, 'BCU data request' also causes the 2870 to gate data onto the 'storage bus in' and raise the mark lines needed (9).

The rest of the operation depends on the storage unit and BCU. When the BCU no longer needs the address and keys, it drops 'BCU response' (5). The fall of BCU response drops the store line to BCU (10), causes the 2870 to remove the address and keys from the buses (6), and drops the address valid line to BCU (7). At about the same time, the BCU raises 'accept' (11). 'Accept' signals the 2870 that the requested main storage cycle has started and that the next 'advance' signal (13) from BCU is part of that storage cycle. 'Accept' sets either the CCW or data accept latch (FC555) (12) in main channel -- depending on which request latch was set for (2). 'Accept' also resets the request latch that started the main storage cycle (2).

The 2870 now has either the CCW accept or the data accept latch and the storage cycle latch set, and is waiting for the BCU to send 'advance.' ('Advance' indicates to the 2870 that a store operation is completed, or that data fetched from main storage is on the storage bus out.) 'Advance' resets the CCW or data accept latch (12) and triggers either the CCW or data advance singleshots (15) (depending on the operation). While the advance singleshots are timing out, the data or CCW (if a fetch), and any error indications become valid on the storage bus out (14). For a store operation, the advance singleshots are only used to time the turn-on of the storage cycle over latch (17).

For a fetch operation, the advance singleshots time out and cause main channel to ingate the information from the storage bus out to the data register (16) (FC555). Any error indications sent by the BCU are set into latches at the same time. The advance singleshots also set the storage cycle over latch (17) to indicate that the operation is completed. 'Storage cycle over' resets the storage cycle latch and ends the main storage operation. Details of the data or CCW gating that occurs during the main storage cycle can be found in descriptions of multiplex or selector subchannel start I/O, read, or write.

Device Service Request Sequence

- The device service request sequence is used to select an I/O device on the interface when a device requests service by the 2870.

- Multiplex devices use the device service request sequence once for each byte of data transferred, and to present status information (FC807).

- Selector subchannel devices use the device service request sequence only to present status to an idle SSC (secondary status).

- COD-3, -4.

On either the SSC or the MSC I/O interface, a device service request sequence is performed when a control unit raises 'request in.' The device service request sequence selects the control unit and a device by using the I/O interface selection controls and the address supplied by the control unit. Both the MSC and the SSCs have a device service request sequence.

The MSC sequence is used each time a control unit needs to transfer a byte of data over the interface, or to present status. Therefore, MSC device service request leads to either a data handling sequence or a trigger 9 CSW sequence.

The SSC sequence is used only when a control unit presents status to an idle SSC. In this case, the status is considered secondary status and the SSC device service request sequence stacks the status back in the control unit and raises 'interrupt request' to CPU. When CPU honors the pending interrupt with 'interrupt response,' a trigger 7 sequence is performed and a CSW is stored in main storage.

MSC Device Service Request

The device service request sequence causes the MSC to select a control unit and device for an operation over the I/O interface. For multiplex devices operating in byte mode, the MSC device service request sequence is used for each byte of data or status transferred over the I/O interface. This is necessary because the MSC disconnects from the device after each data byte transfer (to allow multiplexing of many devices).

To initiate the MSC device service request sequence, a control unit raises 'request in' (Figure 3-3) (FC807). 'Request in' tests the MSC tie break

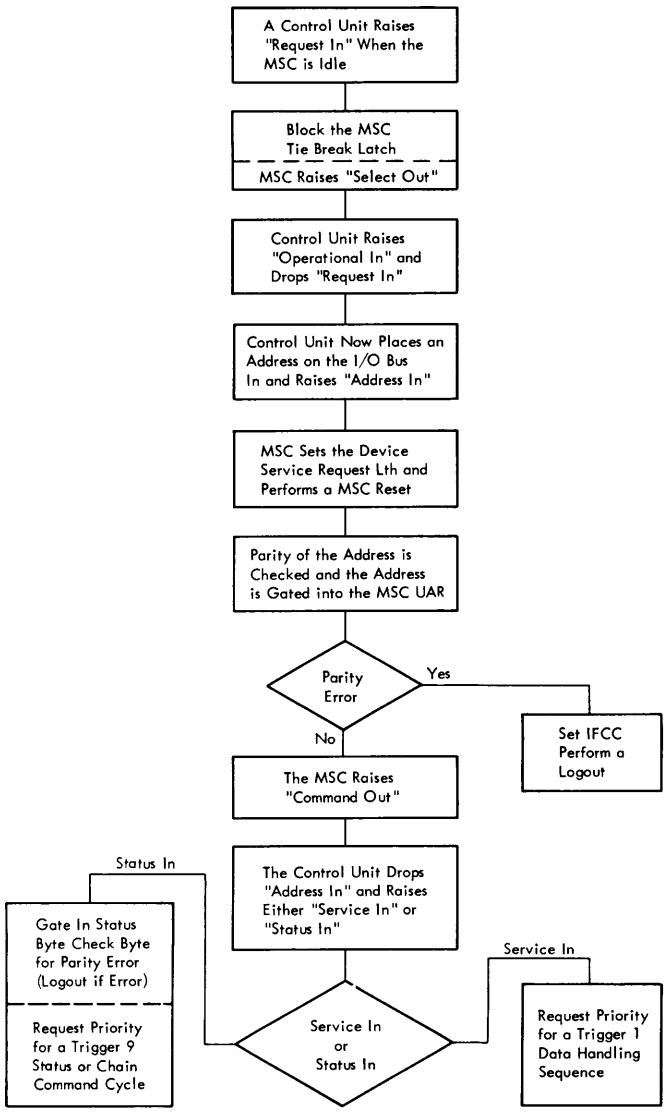


Figure 3-3. MSC Device Service Request

circuit to be sure that device service request does not interrupt a CPU-initiated operation. Assume that the MSC is idle; 'request in' blocks the setting of the MSC-selected latch (Figure IOP 4, B3).

The control unit answers 'select out' with 'operational in,' 'address in,' and an address on the I/O bus in; 'request in' falls. 'Operational in' indicates to the MSC that the control unit is selected. 'Address in' signals the MSC that the address of the selected I/O device is on the I/O bus in, and causes the MSC to latch this address in the MSC UAR. 'Address in' also turns on the device service request latch, turns off the select out latch (Figure IOP 4, D2), and turns on the MSC clock (Figure IOP 4, E5).

At time A1, the MSC is reset. At time A2, the parity of the address is checked and an address-in check is indicated if an error is detected. An address-in check turns on interface control check and causes a logout to be performed. Assume that the parity of the address is good. At A3 time, command out is raised to the control unit (Figure IOP 4, B9). 'Command out' causes the control unit to drop 'address in' and remove the address from the I/O bus in. The fall of 'address in' degates the turn on to the MSC clock (Figure IOP 4, E5). When the MSC clock signals fall, 'command out' to the control unit is dropped. When 'command out' falls, the control unit raises either 'service in' or 'status in.'

Service In: Turns on the data cycle request latch (FC807) and causes the MSC to request priority for a trigger 1 data sequence. 'Service in' indicates that the control unit needs to transfer a byte of data (either read or write). When priority is granted, the trigger 1 sequence (FC201) fetches UCW 0 to determine the type of operation to be performed. UCW 1 is fetched either to supply data for a write, or receive data for a read operation. Trigger 1 controls the data gating in the MSC and also causes the MSC to answer 'service in' with either 'service out' or 'command out.' 'Service out' tells the control unit that a data byte is on the I/O bus out for a write operation, or that a data byte has been accepted for a read operation. 'Command out' is only issued if the data cycle cannot be performed. Details of the read and write operations can be found in the Multiplex Subchannel Read/Sense and the Multiplex Subchannel Write/Control sections.

Status In: Indicates that the control unit needs to present status information to the CPU. (See COD-5.) The control unit status byte is on the I/O bus in. 'Status in' turns on the MSC clock. At time A2, the parity of the status byte is checked, and, if a parity error is detected, a logout with an interface control check on is performed. Assume that parity is correct (FC011). At time A3, the status cycle request latch is set. 'Status cycle request' causes a main channel priority request for a trigger 9 CSW sequence. When priority is granted, trigger 9 examines for interrupt queue full (FC311) or chain command condition (FC313). If command chaining is indicated, it is performed as described in the Multiplex Subchannel Chain Command section. If the interrupt queue is full, 'command out' is raised to stack the status back in the control unit (see COD-6), and the stack status bit is turned on in UCW 2 of the device. If the interrupt queue is not full, a CSW is formed by triggers 9 and 10 and interrupt request is raised to the CPU. When the CPU answers 'interrupt request' with 'interrupt response,' the CSW is transferred to main storage by trigger 11.

During trigger 9 (FC311), UCW 0 is read out and examined for busy subchannel. If the subchannel is not busy, control unit interrupt is set and command out is raised to stack the status in the device. Control unit interrupt causes a CPU interrupt request. When CPU raises interrupt response, a pseudo test I/O is performed (FC317) to relieve the device of status and the CSW is stored by trigger 7; CPU is released with condition code 00.

SSC Device Service Request

The SSC device service request sequence is used when a control unit on the SSC I/O interface needs to present status information to an idle SSC (control unit interrupt sequence). This sequence causes the SSC to select the device, latch the device address in the SSC UAR, stack the status back into the control unit, and raise 'interrupt request' to the CPU. When CPU answers 'interrupt request' with 'interrupt response,' a pseudo test I/O is performed to relieve the control unit of status and trigger 7 forms the CSW, which is sent to CPU.

To initiate the device service request sequence, a control unit raises 'request in' (Figure 3-4) (FC925). If the SSC is not busy, 'select out' is raised to the control unit and the SSC tie break circuit is blocked. 'Select out' causes the control unit to raise 'address in' and place a device address on the I/O bus in.

'Address in' turns on the SSC clock and sets the device service request latch. At time A1, the SSC is reset. At time A2, the parity of the address on bus in is checked and the address is gated into the SSC UAR if parity is correct. A parity error would cause a logout with interface control check indicated. At A3 time, 'command out' is raised to the control unit.

'Command out' causes the control unit to drop 'address in,' remove the address from I/O bus in, place its status byte on the I/O bus in, and raise 'status in.' 'Status in' causes the SSC clock to cycle and turn on the I/O disconnect latch (FC927). The I/O disconnect latch causes the SSC clock to cycle again and turn on the I/O disconnect condition latch. The status byte is not examined at this time.

'I/O disconnect condition' causes the SSC to drop 'select out' and raise 'suppress out' and 'command out' to the control. 'Command out' stacks the status back in the control unit. 'Suppress out' blocks other control units from requesting the SSC I/O interface. At the same time, the interrupt pending latch is set in the SSC. 'Interrupt pending' causes an interrupt request to CPU. The device service request, I/O disconnect, and I/O disconnect condition latches are reset to end the operation. The SSC now waits for CPU to answer the interrupt request.

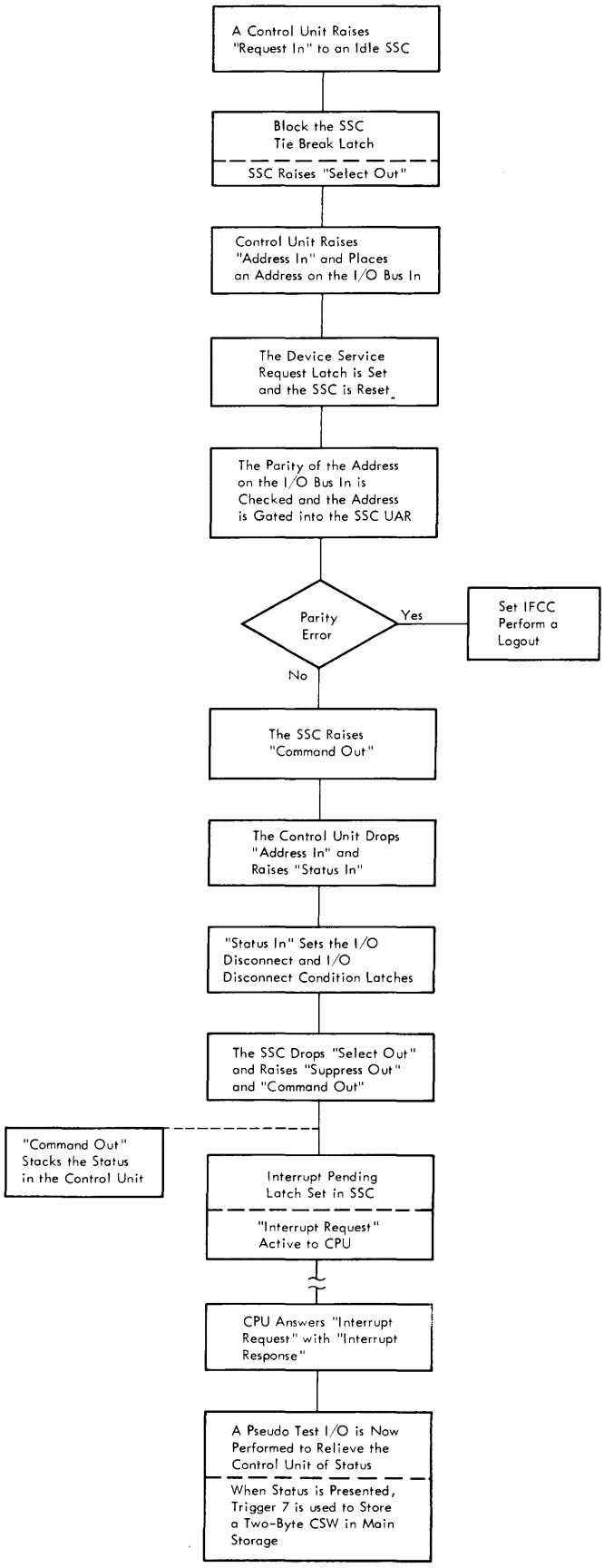


Figure 3-4. SSC Device Service Request

CPU answers interrupt request by raising 'interrupt response' (FC353). 'Interrupt response' to the SSC with the interrupt pending latch set, sets the interrupt response and control unit interrupt latches in that SSC. This indicates to the SSC that CPU has accepted the control unit's interrupt. The SSC makes a priority request.

When priority is granted, the pseudo test I/O latch is set in main channel (FC351). 'Pseudo test I/O' causes the I/O device to be selected (using the address held in the SSC UAR) and 'test I/O' is issued to the device (I/O command of zeros). When the I/O device returns its status, trigger 7 is turned on. Trigger 7 forms a two-byte CSW and sends it to main storage.

MODE TRIGGERS

- The trigger 1 sequence controls data transfers between main storage and the 2870 for both the multiplex and selector subchannels.
- The trigger 2 sequence fetches the new CCW required for a multiplex or selector subchannel CDA operation.
- The trigger 3 sequence forms a new UCW 0 from the CCW fetched by the trigger 2 sequence.
- The trigger 4 sequence fetches data from main storage for a multiplex subchannel write CDA operation when the next CCW is not prefetched.
- Trigger 5 and trigger 6 sequences assemble a CSW for a selector subchannel operation.
- Trigger 7A turns on the halt I/O bit in a multiplex subchannel's UCW 2 prior to performing the trigger 7 CSW sequence.
- The trigger 7 sequence assembles and stores a CSW, for a multiplex or selector subchannel, while the 2870 is attached to the CPU.
- The trigger 8 sequence increments the command address field (+8) of UCW 2, if a control unit presents the device end and status modifier bits when the CC flag is on in the flag register.
- The trigger 9 sequence is used by the multiplex subchannels to stack status, chain commands, or assemble a CSW.
- The trigger 10 sequence completes a CSW assembly began by trigger 9, stores the CSW in UCW 2, and raises 'interrupt request' to the CPU.
- The trigger 11 sequence stores a CSW in main storage (already assembled and stored in local storage) when the interrupt response or test I/O line is raised by the CPU.

Main channel has a group of mode trigger sequences that determine the manner in which I/O operations are executed, CCW's are fetched, or CSW's are formed. A mode trigger is turned on when either main channel or a subchannel determines that an operation can be either partially or completely performed by a mode trigger sequence. The mode trigger is combined with main channel and subchannel status or control conditions to determine such things as adder gating, data flow, and I/O interface signals, The mode trigger operations are sequenced by the main channel clock.

Mode Trigger Selection

When the CPU, main channel, or a subchannel requires use of the main channel, it makes a priority request. When the requesting unit receives its priority response, it gates lines that contain data and control information to the main channel. The main channel takes some of these control lines and ANDs them with the response delayed pulse to turn on a mode trigger.

The control lines that are ANDed with the response delayed pulse and the mode triggers they activate are:

Unit Requesting Priority	Control Line	Mode Trigger Activated
SSC	SSC data cycle	1
	SSC CSW cycle and not channel response = channel select.	5 and 6
	SSC CSW cycle and channel response = channel select.	7
	SSC CC cycle and status bit 33.	8
MSC	MSC data cycle request.	1
	Status cycle to MC and initial select to MC -- MSC halt I/O.	7A
	Status cycle to MC and initial selection to MC -- MSC.	7
	Status cycle to MC and not initial selection to MC.	9 and 10
CPU	MSC interrupt response - interrupt cycle	11

Mode Trigger 1 (Figures 3-5 to 3-12)

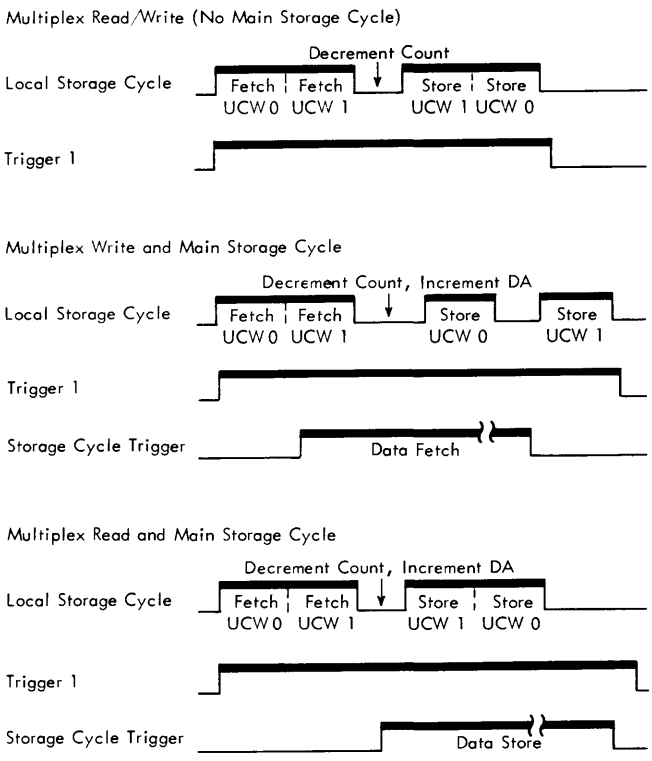


Figure 3-5. Multiplex Trigger 1

Mode trigger 1 controls data transfers between any subchannel and main storage, except for three conditions:

1. A multiplex subchannel initial data fetch for a write or control start I/O instruction.

2. A multiplex subchannel data store operation, when the device has raised status into the channel but the byte count field and the byte counter of UCW 0 are not at zero (this occurs under trigger 9).

3. A multiplex subchannel data fetch for a write CDA operation when the count equals 1 and the next CCW has been prefetched (this occurs under trigger 4).

For both multiplex and selector subchannels, trigger 1 performs data transfers between main storage and the 2870 under the control of UCW 0. UCW 0 contains the data address, count, flags, and operation code for the current operation. The data transfer is performed by reading out UCW 0 to control the transfer (UCW 1 is also read out for multiplex subchannels), updating the count and data address fields of UCW 0, and storing UCW 0 back in local storage (UCW 1 is also stored for multiplex subchannels). The trigger 1 sequence as modified by the CDA flag is described later.

The normal mode trigger 1 sequence (Figure 3-5):

1. Decrements the byte count field of UCW 0 in the subchannel by 8 (SSC) or 1 (MSC).

2. Increments (read/write) or decrements (read backward) the data address field of UCW 0 by 8 if a main storage data store/fetch is required.

3. Increments the byte count field of UCW 0 by 1 (MSC).

4. Tests to determine whether a CDA operation is required at this time.

5. Tests to determine whether the device should be stopped (count equals zero or halt I/O, MSC, or reject).

Mode Trigger 1 and CDA

During the mode trigger 1 sequence, tests are made to determine whether a CDA operation is to take place at this time. These tests examine the following conditions:

1. Read operation is currently in process, CDA flag, and count equals one (MSC) or new CCW line (SSC) (Figure 3-6).

2. Write operation is currently in process, CDA flag, last data fetch is in process for current CCW (SSC -- last word/double last word trigger on) or count less than 8 but greater than 1 (MSC) (Figure 3-7). See COD-13.

3. Write operation is currently in process, CDA flag, all data for the current CCW has been exhausted, and prefetch bit is off (Figure 3-8). See COD-14.

Any one of the above conditions turns on a trigger to perform the CDA sequence. These triggers are described in the following text.

Selector Subchannel CDA Triggers: When condition 1 or 2 is determined during the trigger 1 sequence for a selector subchannel, a data store or fetch into main storage is required, followed by a CCW fetch, and a new UCW 0 is formed from the new CCW

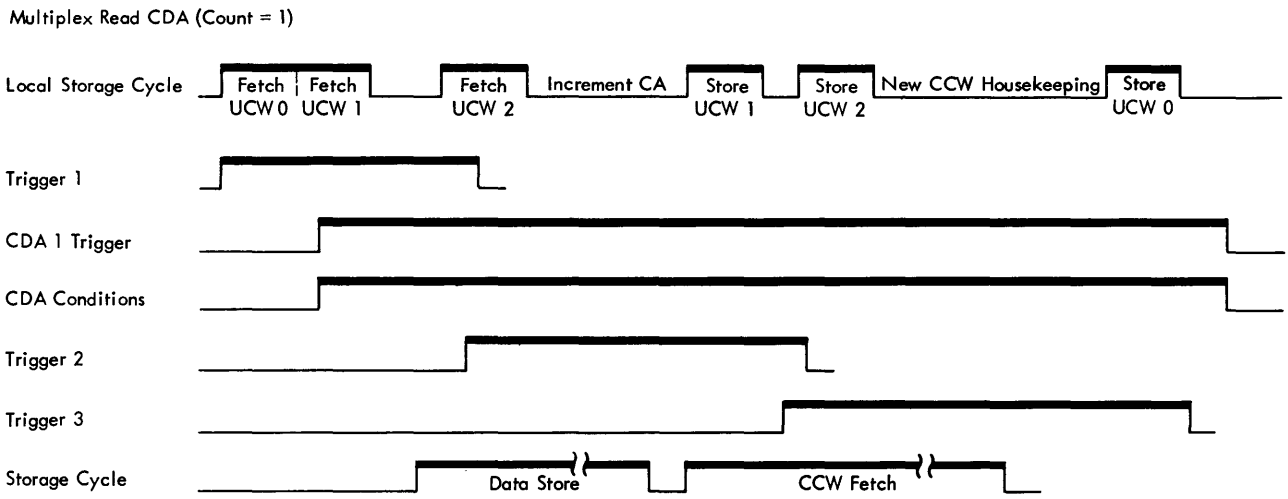


Figure 3-6. Multiplex CDA Trigger 1

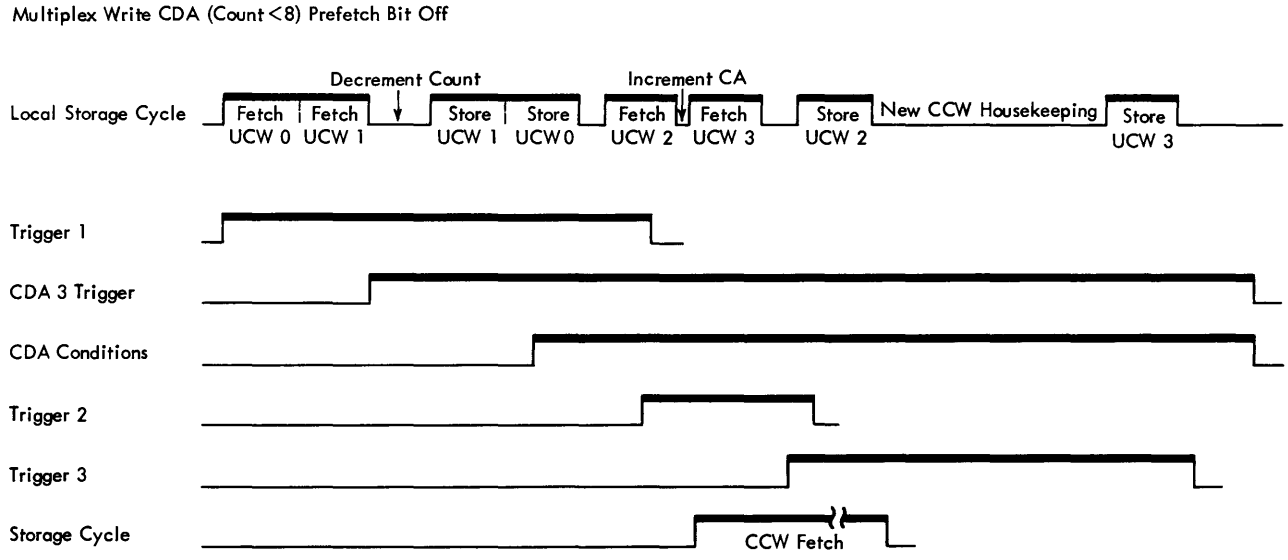


Figure 3-7. Multiplex CDA 3 Sequence

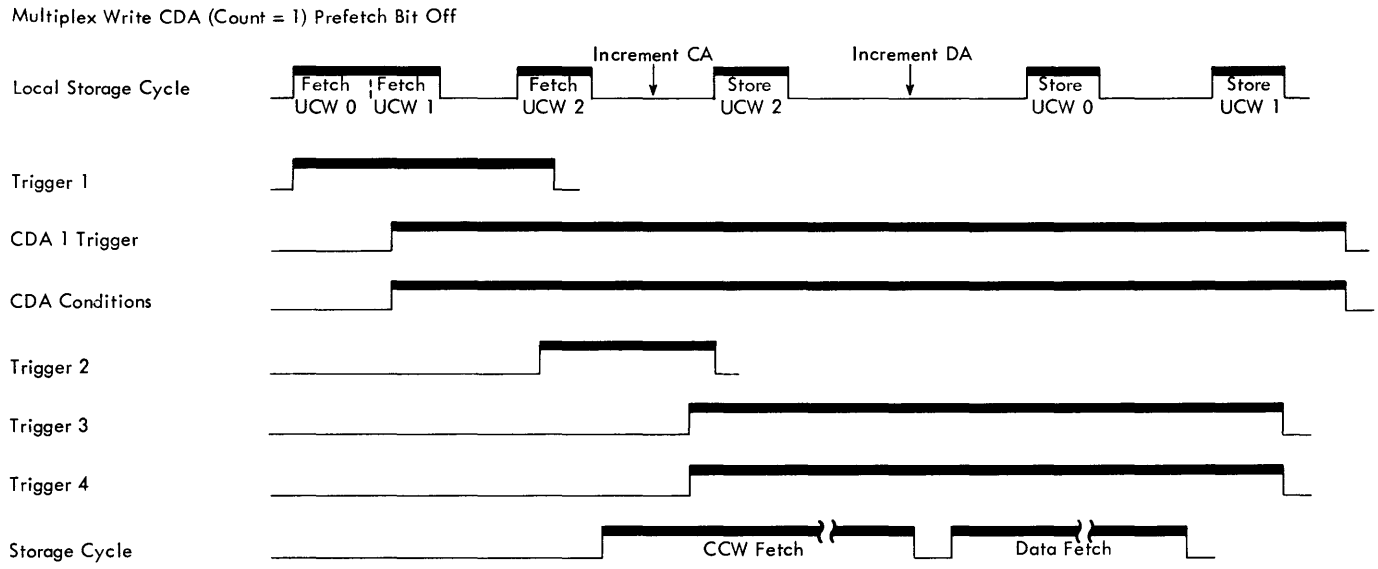


Figure 3-8. Multiplex CDA Trigger 1 (Prefetch Off)

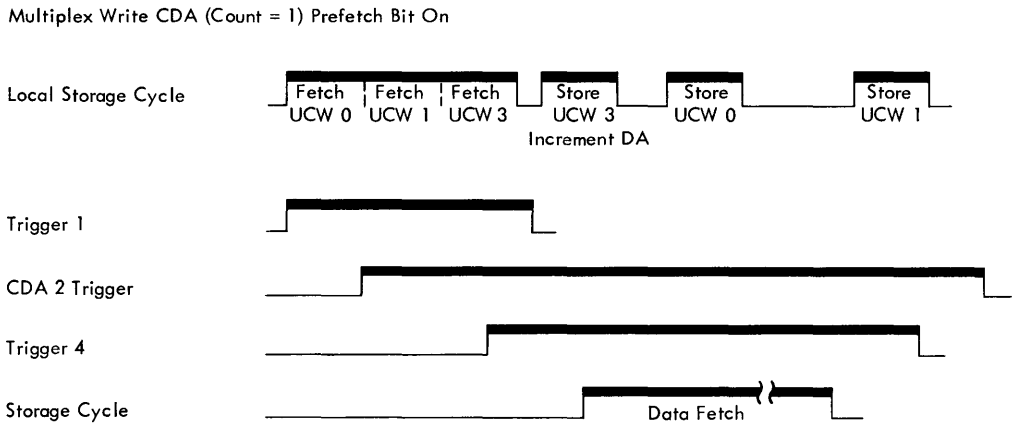


Figure 3-9. Multiplex CDA2 Trigger 1 (Prefetch On)

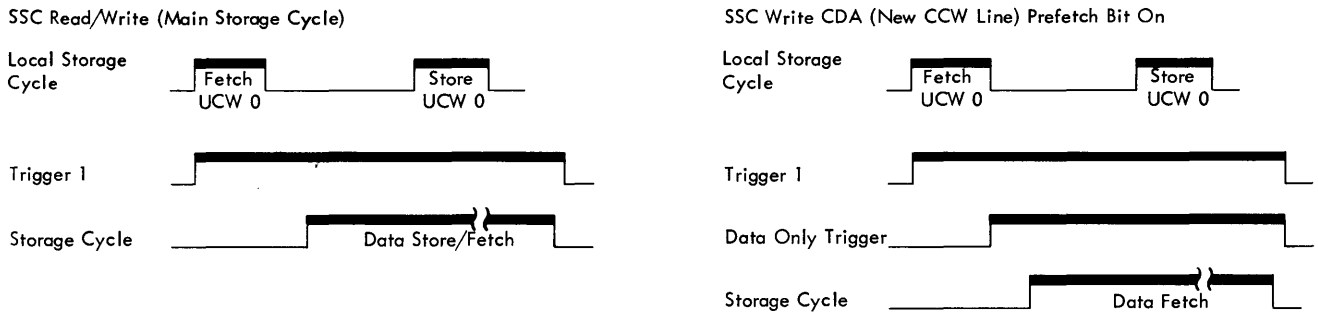


Figure 3-10. SSC Basic Trigger 1 and Data Only Trigger

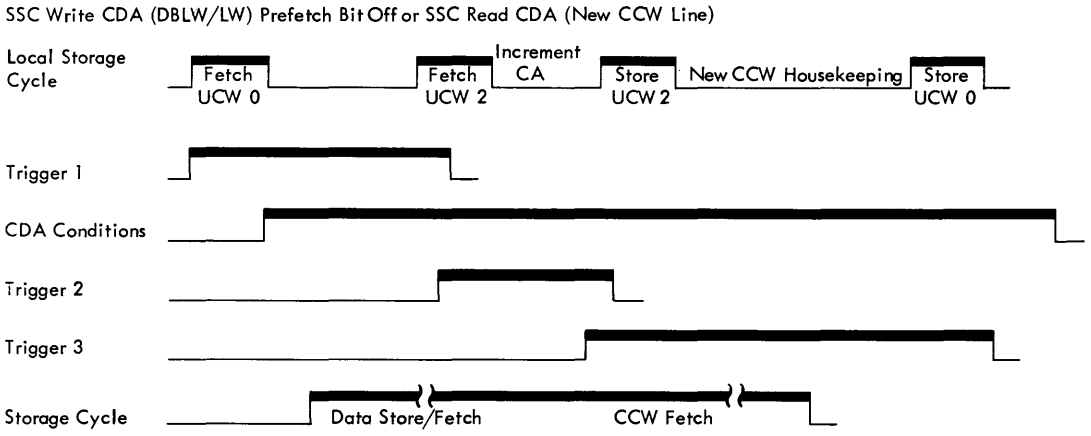


Figure 3-11. SSC Read/Write CDA CCW Fetch

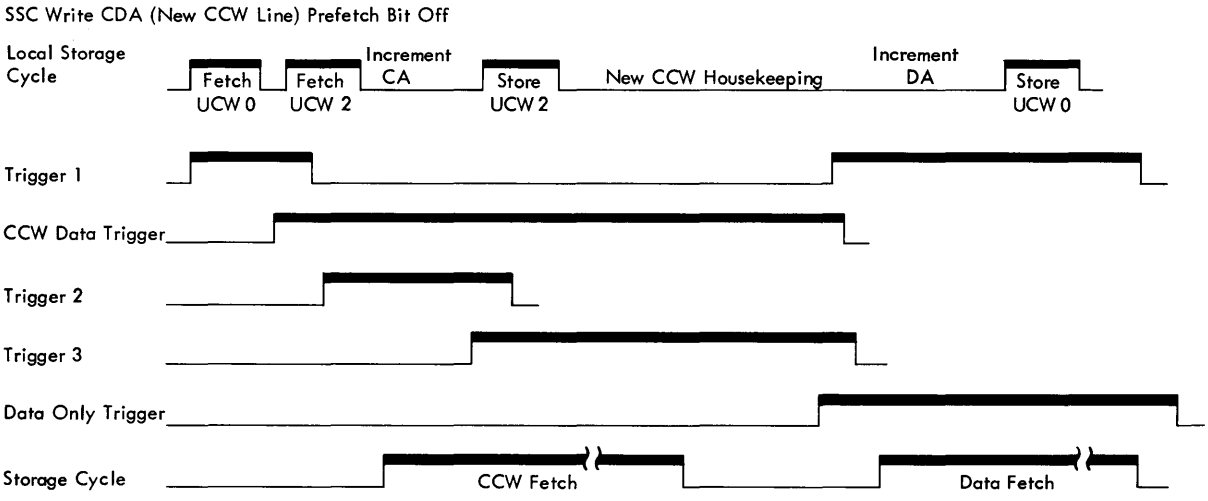


Figure 3-12. SSC/CCW Data Trigger

(FC251). During the trigger 1 sequence the CDA condition trigger is turned on to control this sequence (Figure 3-11).

For condition 2 (FC253), the prefetch bit is turned on (UCW 0, bit 39) to record that a CCW prefetch has occurred. This bit is reset when the first data fetch for that CCW occurs.

Condition 3 (FC255) occurs when an SSC is performing a write CDA operation and is transferring its last doubleword of data for the current CCW, which requires a new CCW and the data associated with it (SSC new CCW line is active). This can occur if the CCW's in a CDA sequence have small byte count fields, causing condition 2 to be missed. Therefore, a prefetch would not have taken place. During the trigger 1 sequence, the CCW data trigger is turned on to control the needed sequence (Figure 3-12).

If the SSC is performing a write CDA operation and the prefetch bit is on when the SSC enters the trigger 1 sequence, the data only trigger is turned on to:

1. Inhibit the turn-on of the CDA condition trigger.

2. Block decrementing the count (Figure 3-10).

Multiplex CDA Triggers: The CDA requirements of the multiplex subchannel are similar to those of the selector subchannel. Two major differences are:

1. The multiplex subchannel prefetches the new CCW when the count is less than 8 (SSC is 16 or less).

2. The multiplex subchannel uses its local storage location word 3 to store its prefetched CCW.

Like the SSC, the multiplex subchannel uses the CDA condition trigger to control its CDA sequences. However, three additional triggers are used by the multiplex subchannel to control various CDA operations. The following chart shows the necessary conditions and functions of the triggers:

Trigger	Prefetch Bit On	Count	Read/Write	Comments
CDA 1 (FC201) (FC203) (FC205)	No	1	Read/Write	CCW fetch and data fetch (Figures 3-6 and 3-8).
CDA 2 (FC207)	Yes	1	Write	Replace the contents of word 0 with word 3 (prefetched CCW); data fetch (Figure 3-9).
CDA 3 (FC209)	No	2-7	Write	Prefetch CCW and store in word 3 (Figure 3-7).

Mode Triggers 2, 3, and 4 (Figure 3-8)

When the controls in the main channel detect that a CDA operation is to take place during a trigger 1 sequence, the main channel causes other mode triggers to be active after trigger 1. The complete CDA operation is performed during the subchannel priority response that causes a trigger 1 sequence. Therefore, during the following mode trigger sequences, no other subchannel can have access to the controls in the main channel.

Mode Trigger 2 (FC207)

1. Transfers the current command address from bytes 1-3 in UCW 2 to bytes 5-7.

2. Increments the current command address by 8 and stores the address in bytes 1-3 of UCW 2.

3. Initiates a CCW fetch.

4. Stores UCW 2.

Mode Trigger 3 (FC209)

Mode trigger 3 performs the following functions for the new CCW:

1. Loads the last three bits of the data address (DAB) into the byte count field of UCW 0 (MSC).

2. Gates the operation code into byte 0 of UCW 0 from the operation buffer latches.

3. Turns on the PCI flag or prefetch bit, if applicable.

4. Gates the new CCW information to the SSC.

5. Stores UCW 0, if no data fetch is required.

6. Adds the DAB to the count field and gates the last three bits of the sum to the SSC.

Mode Trigger 4 (MSC) (FC211)

If the channel is executing a write CDA 1 or CDA 2 sequence (MSC), a data fetch is required. This trigger:

1. Initiates a main storage data fetch.

2. Stores the new CCW in UCW 0.

3. Stores the new data in UCW 1.

CSW Assembly Triggers (FC301 & FC303)

Mode Triggers 5 and 6

Mode triggers 5 and 6 assemble an SSC CSW at the end of a start I/O instruction when the SSC is not connected to the CPU. They also:

1. Fetch UCW 2 into the control register and fetch UCW 0 into the data register.

2. If the prefetch bit is on, gate the residual command address (bytes 5-7 of UCW 2) into bytes 1-3 of UCW 2.

3. Assemble the channel status from UCW 0 and the SSC status into the control register and gate the control unit status into the control register.

4. Correct the residual byte count by subtracting the SSC byte count from the count field, and gate the remainder into the control register.

5. Store UCW 0 and 2.

UCW 2 now contains the CSW. The interrupt line from the SSC is active, causing an interrupt request to the CPU.

Mode Trigger 7 (FC307)

The mode trigger 7 sequence is used by both the SSC and MSC to assemble a CSW if:

1. A CSW is to be stored in response to a start I/O, halt I/O, or test I/O instruction (condition code 01).

2. A pseudo test I/O has been performed (a CPU interrupt response has been received in response to a control-unit-initiated interrupt request).

In all cases, the CPU is connected to the MSC or SSC during the trigger cycle.

The following chart relates the type of operation to the release code and the bytes stored in the CSW:

Operation	Release Code	Bytes Stored	Comments
Start I/O	01	4 and 5	Instruction completed; subchannel is free.
Start I/O	00	None	Chain command -- command immediate.
Test I/O	01	0-7	
Halt I/O	01	4 and 5	Idle/byte mode device halted.
Halt I/O	10	None	Burst mode device halted.
Pseudo test I/O	00	0-7	Interrupt response to control unit interrupt

Mode Trigger 7A (FC309)

If a halt I/O is executed on the MSC interface, the multiplex subchannel executes a mode trigger 7A sequence and turns on the halt I/O bit (bit 5) in UCW 0. The multiplex subchannel then continues in the normal trigger 7 sequence. The halt I/O bit:

1. Causes a halt I/O to the addressed device if that device requests a data transfer sequence (trigger 1).

2. Inhibits a chain command operation for the addressed device.

Mode Trigger 9 (FC311)

The mode trigger 9 sequence is performed when 'status in' is received on the MSC interface and the MSC has been granted priority to the main channel controls. Four operations take place during this sequence:

1. Stack Secondary Status -- If a device presents status to an idle subchannel, the status is stacked (command out to status in) (FC809). If the interrupt buffer full trigger is off, the address of the device is gated to the interrupt register and the trigger is turned on, causing an interrupt request to the CPU.

2. Stack Ending Status -- If a device presents ending status to the subchannel but the interrupt

buffer full trigger is on and the device is not command chaining, the status is stacked. To record that the device has been stacked, the operation proceeds from trigger 9 to a refetch 2 sequence (FC605). This sequence fetches UCW 2, turns on bit 7 (channel end stack bit), and stores UCW 2.

3. Chain Command (FC319) -- If the device presents the channel end and/or device end bit, UCW 0 contains the chain command flag, and no error conditions are present, the multiplex CC latch is turned on. During the multiplex CC sequence, 'service out' is sent in response to 'status in,' and 'suppress out' is sent to the device. If the device end bit is present, the MSC pseudo start I/O and CCW chain command request latches are turned on. These latches cause the main channel controls to fetch a new CCW; the MSC interface reselects the device.

4. CSW Assembly -- If the device presents ending status, the interrupt buffer is not full, and command chaining is not to be performed, the CSW must be assembled for that subchannel. Trigger 10 is turned on to perform the assembly (FC310).

Note: If during conditions 2, 3, or 4, UCW 0 indicates a read operation and the count and the byte counter do not equal 0, a data store sequence is required. The data sequence latch is turned on during the trigger 9 sequence (FC311), and a main storage data store is performed. The byte counter is then reset to 0, so that the sequence cannot take place again.

Mode Trigger 10 (FC315)

The mode trigger 10 sequence takes information from UCW 0 and 2 and places the information into the proper CSW format in the control register. The CSW is stored in UCW 2 and the interrupt buffer full latch is turned on, causing an interrupt request to the CPU.

Note: If the CPU issues a test I/O (FC317) to a subchannel that has stacked the ending status of a device, a test I/O is performed on the multiplex interface. However, since the CSW was not assembled, the subchannel requires a trigger 9-10 sequence, not a trigger 7 sequence. The CSW is stored and the CPU is released during the trigger 10 sequence.

Clearing Channel Interrupts

The channel recognizes three types of interrupts:

1. Control unit initiated

2. PCI

3. Termination of an instruction

Interrupts 2 and 3 are cleared through the trigger 11 sequence (FC351).

PCI Interrupts

The PCI interrupt is cleared only when the CPU responds with interrupt response to the channel interrupt request. When the CPU responds and the CPU priority response is granted, trigger 11 (FC351) is turned on. The trigger 11 sequence:

1. Fetches UCW 0 and 2.

2. Stores UCW 0 and 2 unaltered.

3. Assembles a CSW in the control register.

4. Stores the contents of the control register in main storage (location 64).

5. Releases the CPU (condition code 00).

End Interrupts

If a subchannel has completed an I/O instruction and assembled its CSW (SSC, triggers 5 and 6; MSC, triggers 9 and 10), an interrupt is generated to the CPU. The CPU may clear the interrupt by issuing a test I/O instruction to the subchannel with the outstanding interrupt request, or by interrupt response. In either case, when the CPU has been granted a main channel priority response, the trigger 11 sequence (FC351):

1. Fetches and stores UCW 2 which contains the CSW.

2. Stores the contents of the control register into main storage location 64.

3. Releases the CPU (condition code 00 if interrupt response; condition code 01 if test I/O).

Control Unit Status Modifier Bit (Trigger 8) (FC305)

When an I/O device presents the control unit status modifier and device end bits in its status and the channel recognizes that it is to perform a chain command operation, the channel must increment the command address in UCW 2 and gate the incremented address to the SAB register.

The main channel trigger 8 sequence fetches UCW 2, increments the address by 8, and turns on the pseudo start I/O and CCW chain command required latches. These latches cause the new CCW to be fetched; the device is reselected.

MULTIPLEX SUBCHANNEL START I/O

- CPU initiates a channel program for an I/O device by issuing CPU start I/O and select channel to the addressed channel with the unit address of the device involved.
- The 2870 begins a CAW fetch from main storage and examines the device's UCW 0 for a busy subchannel.
- If the subchannel is not busy, the 2870 gates in the CAW and uses its storage protect key and CCW address fields to fetch the first CCW from main storage.
- UCW 2 is formed from the CAW.
- UCW 0 is formed from the CCW.
- The multiplex initial selection latch is set in MSC and selection of the I/O device begins.
- If the device selection is successful, CPU is released with condition code 00 and the I/O operation begins.
- COD-1.

All references are to Figure IOP 1 in the diagram manual unless otherwise specified.

To initiate an I/O operation, CPU must select the channel. The channel must obtain the command to be executed from main storage, select the I/O device, and initiate the I/O operation at the device (Figure 3-13). These functions are accomplished by the CPU start I/O instruction.

A start I/O instruction to an available (idle) subchannel, causes the selection of the associated device and, when possible, the initiation of the channel command. The channel commands associated with start I/O are: read, read backward, write, sense, and control. For the multiplex subchannels, these operations are grouped as follows:

Read or Input

Read

Sense

Read backward

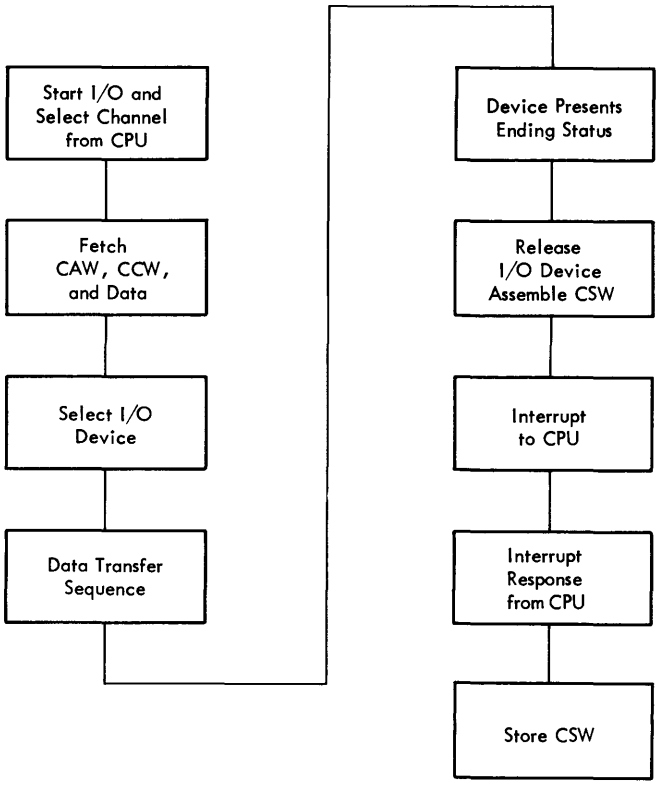


Figure 3-13. Multiplex Subchannel Operations

Write or Output

Write

Control

Acceptance or rejection of the initial command causes the channel to release CPU with a condition code that indicates the result of the instruction.

The start I/O-initial selection sequence (FC101) for a multiplex subchannel begins when start I/O is issued to the 2870 with a device address that designates a multiplex subchannel and its associated device (Figures 3-14 and 3-15). Multiplex subchannel start I/O operations are performed by both the main channel and the MSC. The main channel fetches the CAW and the first CCW from main storage and forms UCW's 2 and 0, respectively. After UCW 0 has been formed, the MSC circuits begin the device selection. If the device is selected and returns an initial status byte of zeros, the command is considered accepted and CPU is released with condition code 00. If the device fails to answer the selection sequence, CPU is released with condition code 11. If the device's initial status byte is not zero, a trigger 7 CSW sequence is performed to store the status byte in the CSW in main storage and CPU is released with condition code 01.

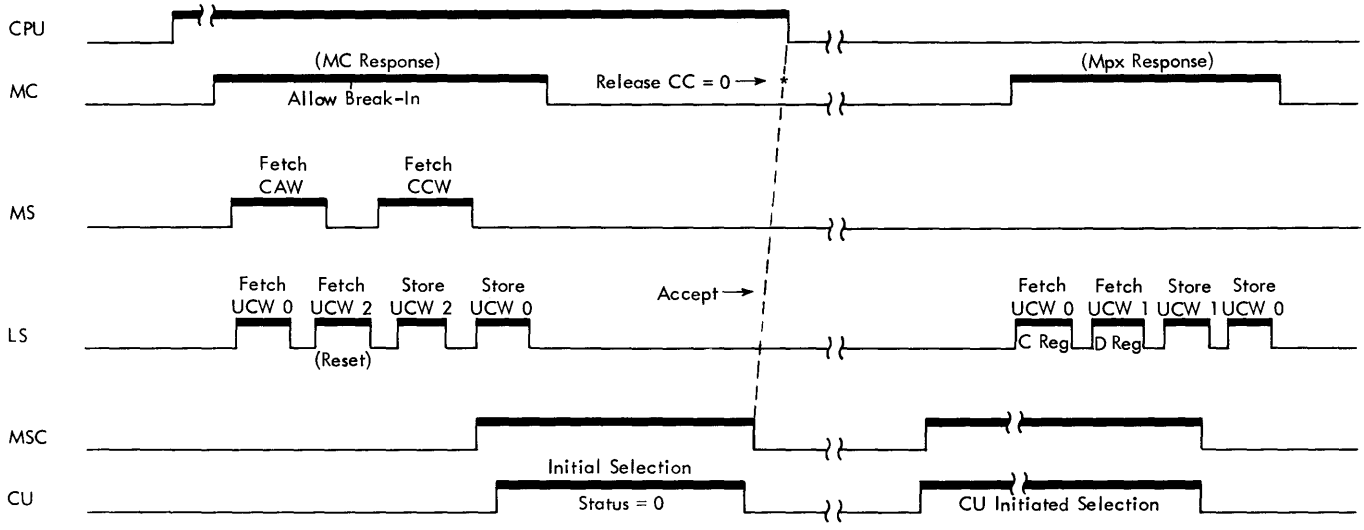


Figure 3-14. Multiplex Subchannel Start I/O (Read)

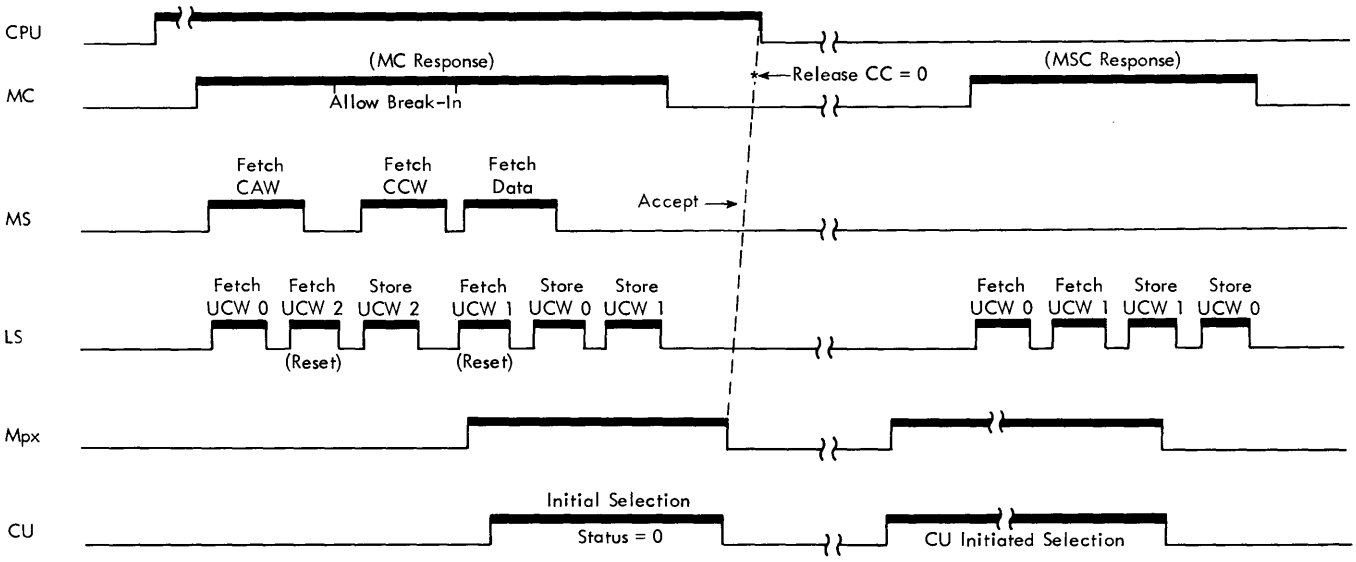


Figure 3-15. Multiplex Subchannel Start I/O (Write)

Start I/O to Channel (Fetch CAW) (FC101)

- CPU sends select channel, start I/O, and a unit address.
- Request main channel priority.
- Set the CAW latch and decode the unit address.
- Read out UCW 0 to examine bits 6 and 7 for idle subchannel (0, 0), and begin the CAW fetch.
- If bits 6 and 7 are on, the subchannel is busy, CPU is immediately released with condition code 10, UCW 0 is stored, and the CAW is blocked from entering the 2870.
- Turn on the CCW request latch and force address 72 into the SAB register (to fetch the CAW) (FC551).
- BCU advance generates CCW advance and late advance to gate the CAW into the 2870.
- Set the storage cycle over latch and test for errors.
- Storage cycle over and no errors sets the CCW required latch to prepare for the CCW fetch cycle (FC105).
- Another subchannel may break in to perform some data or status sequence between the CAW and CCW fetches.
- COD-1.

The CPU activates the start I/O multiplex line to the main channel, places an eight-bit unit address on the UABO, and signals the 2870 with the select channel line. Start I/O and select channel from the CPU generates a main channel priority request to the priority circuit. When priority is granted, 'main channel response' and 'response delayed' become active.

Main channel response sets the 'gate latch,' which causes the unit address to be gated from the UABO through the IUAR to the UAOR (C3). The output of the UAOR feeds a decode circuit that determines the type of subchannel addressed. Positions 0 and 1 of the unit address determine whether the operation is a selector or multiplex subchannel operation. Positions 0 and 1 can be any combination except 11 (11 indicates selector subchannel) for multiplex subchannels. Assume that a multiplex subchannel is addressed.

Main channel response and response delayed are ANDed with 'start I/O' and 'CPU select channel' to set the CAW latch (FC551). The CAW latch causes the main channel clock to be turned on, and the start I/O latch is set (D4).

With the CAW latch set (FC101) and the 'multiplex subchannel decoded' line active from the address decoder, main channel now begins a local storage fetch for the device's UCW 0 and a main storage fetch for the CAW. The two fetches are started in parallel. However, the contents of UCW 0 (which returns first) determine whether or not the 2870 accepts the CAW. When UCW 0 is in the control register, the operation field (bits 6 and 7) is examined for a bit in either position. A bit in either position indicates that the subchannel is busy and cannot accept the start I/O at this time. If the subchannel is busy, the CPU is released with condition code 10, UCW 0 is returned to local storage, and 'block CCW data' is turned on to keep the 2870 from gating the CAW in. Assume that the subchannel is idle (bits 6 and 7 are zeros). UCW 2 is fetched into the control register (to prepare for the new UCW 2 that is to be formed from the CAW) and the main channel clock is turned off.

To begin the CAW fetch (FC551), the address of the CAW (72) is forced into the SAB register, a latch is set to gate in 'BCU response,' and 'CCW request' is set. The CCW request latch activates a storage cycle request to BCU. The BCU replies with BCU response, which indicates that the priority for the main storage cycle has been granted and that BCU is requesting an address on the SAB. The latch set at the beginning of the CAW fetch gates BCU response into the 2870 and causes the CAW address to be placed on the SAB, and 'address valid' is sent to BCU. BCU signals the 2870 that the storage cycle has started by sending the 'accept' pulse (F1), and activating 'BCU data request' (F1). Although data is placed on the SDBI only for a store operation, BCU data request is active for both store and fetch cycles and is used by the 2870 to generate the 'accept pulse gated' line (F1) needed to set the CCW accept latch (E3).

'CCW accept' resets the CCW request latch and ends the storage cycle request. The 2870 now waits for the advance pulse from BCU. 'Advance' leads the data from BCU by about 200 nanoseconds.

'Advance' arrives from BCU and fires a 400-ns singleshot, which generates the CCW advance pulse (F2). 'CCW advance' indicates that the data on the SDBO is valid and should be gated into the 2870's data register. Therefore, 'CCW advance' resets the CCW accept latch, gates the SDBO into the data register (C14) and fires two singleshots in series to produce the CCW late advance pulse (F3). The first singleshot is 500 ns long and 'CCW late advance' is generated when it expires. The duration of 'CCW

late advance' is determined by the second singleshot, which is usually about 100 ns long. This singleshot is adjusted by a procedure contained in the Field Engineering Maintenance Manual, IBM 2870 Multiplexer Channel (60,000/70,000 Series), Form SY27-2302.

'CCW advance' sets the 'CCW in D register' latch (C11). When CCW late advance falls, a 350 ns singleshot (C12) fires to gate the CAW byte 0 from the data register to the control register, and reset the 'CCW in data register' latch. This singleshot also fires a second singleshot (E10), which turns on the 'storage cycle over' latch and gates the remainder of the CAW from the data register into the control register.

'Storage cycle over' indicates that the CAW fetch cycle is complete. A test is made for any errors that may have occurred during the CAW fetch (FC601). If an error occurred during the CAW fetch, the 'storage cycle check' latch will be on. 'Storage cycle over' and 'storage cycle check' are ANDed to generate the 'storage cycle over and check' line to set the 'selection sequence check' latch. 'Selection sequence check' causes the 2870 to release the CPU with condition code 01 and the error condition is stored in the CSW.

'Storage cycle over and no checks' indicates that the CAW fetch was successful and the start I/O operation can proceed (FC105). Therefore, 'storage cycle over and no checks' is ANDed with 'CAW gated' and 'not outstanding request' to set the CCW required latch. 'CCW required' causes the main channel circuits to begin a CCW fetch using the command address just fetched in the CAW.

If during the main storage fetch cycle for the CAW a subchannel raises its priority request line, the 'outstanding request' latch is set. 'Outstanding request' blocks the turn on of 'CCW required' and thus allows the subchannel requesting service to break in and use main channel. The break-in allows all subchannel requests to be serviced before the start I/O CCW fetch is performed.

Outstanding Request (Allow Break-in)

- One of the subchannels has priority request active during the CAW fetch.
- Priority request turns on the outstanding request latch.
- The ending trigger is turned on to reset most of the main channel triggers.
- The CAW is stored in UCW 2.
- The CCW required latch is turned on and the CAW latch is turned off.
- Main channel priority request remains active.
- COD-1.
- When all subchannels requesting priority have completed their operations, the start I/O operation continues.

The outstanding request trigger (FC105) is set if a subchannel requests priority while the CAW is being fetched from main storage. After the storage cycle is completed (with no errors), 'outstanding request' blocks the turn-on of CCW required and allows a break-in sequence to occur. Break-in sets latches to identify the point of return to the start I/O routine, stores the contents of the control register, and then allows the subchannels to break in.

The ending trigger establishes a point of return to the start I/O routine by setting the CCW required latch and resetting the CAW latch. The CAW is stored in local storage in UCW 2.

After the local storage cycle is completed, the main channel busy latch in the priority circuit is reset. The reset of main channel busy resets the main channel priority response latch. Two things now occur: (1) The main channel becomes free for subchannel priority requests; and (2) Main channel priority request becomes active because start I/O and select channel are still active from the CPU.

The subchannel with the highest priority now gains control of main channel and performs its operation. When the operation is completed, priority is granted to the next lower subchannel. When all outstanding requests have been serviced, main channel regains priority and the start I/O operation continues.

CAW in Channel

- Turn off the CAW trigger.
- Fetch UCW 2 from local storage if break-in occurred.
- Reset UCW 0.
- Begin a main storage fetch for the first CCW.
- Form UCW 2 from the CAW.
- COD-1.

The turn-on of 'CCW required' (FC105) conditions an AND circuit to reset the CAW trigger. CCW

required is ANDed with 'not outstanding request' to test whether a break-in occurred. If a break-in occurred, word 2 (CAW) is in local storage and the control register is empty. Therefore, 'not word 2 fetched' and 'not control register full' cause UCW 2 to be fetched into the control register. 'Control register full' and 'not CAW trigger gated' activate the CCW fetch line. 'Control register full' also causes a UCW 0 fetch with 'block' on. 'Block' causes a reset of the contents of UCW 0.

'CCW fetch' and UCW 2 in the control register indicate that the CAW is in the channel and a CCW fetch can be performed. 'CCW fetch' and 'word 2 fetched' turn on the main channel clock and set the CCW request latch. CCW request on initiates a main storage fetch, using the command address in the CAW.

Form UCW 2

The 2870 uses the CAW to form UCW 2. For start I/O operations, the address in the CAW is the residual command address. Therefore, on start I/O operations, nothing is placed in the residual address field and the resulting UCW 2 contains only the address and key of the next command (bytes 0-3). The residual command address field (bytes 5-7) is filled only on write CDA operations.

When the CAW is gated into the control register, the command address is in bytes 1-3. 'CCW fetch' gates bytes 1-3 to the adder (D9) with 'increment' (FC105). The result is the CCW address + 8. The adder is latched and the output of the adder is gated back into bytes 1-3. UCW 2 is stored. After the local storage cycle is completed, the main channel clock is turned off.

CCW Fetch

A CCW fetch is performed in the same manner as a CAW fetch, except that the command address from the CAW is placed in the SAB register (FC551). CCW request activates CCW storage cycle request, which causes a storage request to be sent to the BCU.

When BCU response rises, the address in the SAB register is sent to the BCU and 'address valid' is raised to the BCU. 'Accept' arrives from the BCU to indicate that the next advance pulse from the BCU can be used to gate the CCW into the main channel. Accept turns on the CCW latch, which drops the storage request to the BCU. 'Advance' arrives from the BCU and generates CCW advance.

'CCW advance' resets the CCW accept latch and gates the CCW (on the SDBO) into the data register.

'CCW advance' also fires a singleshot to generate the CCW late advance pulse. 'CCW late advance' sets the 'CCW in D register' latch; and when CCW late advance expires, a 350 ns singleshot gates the CCW into the control register. As the CCW is gated into the control register, a 150 ns singleshot fires and sets the storage cycle over latch (FC557). During the transfer of the CCW from the data register to the control register, the command byte (bits 0-7) is gated through the command encoder, encoded to a two-bit op code, and placed in bits 6 and 7. Bits 0-3 of control register still contain the key field of the CAW. Parity is generated on byte 0.

If an error occurred during the CCW fetch, the storage cycle check latch is turned on. Storage cycle over and check on a CCW fetch sets the selection sequence check latch. If no errors occurred 'storage cycle over and no check' and 'CCW fetch' set the 'CCW in channel' latch to indicate that the CCW is in the control register (FC107). 'CCW in channel' turns off the CCW required latch to end the CCW fetch.

CCW in Channel (Complete Main Channel Operation)

- Form UCW 0.
- For a read operation, reset UCW 1, turn on multiplex initial selection (in the MSC), send the device address to the MSC, and set the ending trigger. (COD-3)
- For a write operation, allow break-in, fetch the first doubleword of data from main storage (put in UCW 1), turn on multiplex initial selection (in the MSC), send the device address to the MSC, and set the ending trigger. (COD-4)
- Ending marks the completion of the main channel operations and the MSC circuits now perform the device selection.
- CPU is not released until the device selection sequence is completed or terminated.

With the CCW in the control register, the main channel forms UCW 0, turns on initial selection in the MSC, and turns on the ending trigger to free main channel from the start I/O operation. 'Initial selection' causes the MSC to begin the initial selection sequence for the addressed I/O device. If the op code specifies a write operation, main channel allows subchannels to break in, and fetches the first doubleword of data before turning on the initial selection and ending latches. The release of CPU depends upon the results of the initial selection sequence.

Form UCW 0

UCW 0 is a modified CCW. As the CCW is transferred from the data register to the control register, the command byte (bits 0-7) is encoded into a two-bit code and placed in control register bits 6 and 7. These bits are:

Bit 6	Bit 7	Operation
0	0	Idle
0	1	Write or control
1	0	Read or sense
1	1	Read backward

The bits (6 and 7) are used by main channel to determine the busy or idle status of the subchannel and the operation to be performed each time the subchannel is addressed.

Bits 0-3 of the control register retain the storage protect key obtained from the CAW. Parity is generated for byte 0.

'CCW in channel' and 'not CCW required gated' turn on the main channel clock (C9) for the UCW 0 formation cycle (FC107). The op code (bits 6 and 7 of the control register) is examined for a forward (read/write) or a backward (read backward) type operation and the result is used to control the form of the DAB used (bits 29-31 of the control register). For a read or write operation, the DAB is used in its true form. A read backward operation requires that the DAB be complemented. The corrected form of the DAB (true or complement) is always placed in the byte count field (bits 45-47), and in the DAB field also (bits 29-31) if a complement is performed. If the 2870 is part of a Model 67 duplex system, the CPU ID bits are also placed in control register bits 37 and 38.

The DAB register is used as an intermediate register in the DAB correction. If a read backward operation is indicated, the DAB is gated to the DAB register in complement form (E8). The complemented DAB is returned to the DAB field and is also gated into the byte count field (bits 45-47) (F8). The complemented DAB provides the byte counter with the correct starting value for the backward count operation necessary for read backward. The complement DAB field provides the correct mark bits for the first main storage cycle performed. For read or write operations, the DAB is sent to the DAB register in true form (E8). However, for read or write it is only necessary to gate the DAB bits from the DAB register into the byte count field (bits 45-47). This initializes the byte counter at the correct starting value.

UCW 0 is now completed and is ready to be put away in local storage. However, if a write operation is indicated, a test is made for any subchannel priority requests (FC109), and a doubleword of data must be fetched and placed in UCW 1.

Read or Read Backward Operations

- COD-3.

For read or read backward operations (FC109), the completed UCW 0 is stored in local storage (D14). To prepare for the data read, UCW 1 is read out of local storage with the block line active. 'Block' prevents the contents of UCW 1 from being read into either the data or control registers. This resets UCW 1. To provide correct parity in UCW 1, the data register is reset to P bits only and then stored as UCW 1.

To begin the initial selection sequence for the I/O device, main channel sets the multiplex initial selection latch in the MSC. The MSC gates the I/O device address from the main channel IUAR to the MSC UAR and begins initial selection (FC801).

To end the main channel's portion of the start I/O operation, the ending trigger is set (F6). 'Ending' resets the main channel busy trigger and allows other subchannels to apply for priority. Although main channel is free for other operations, CPU is not released until the initial selection sequence ends.

Write Operations

- COD-4.

A write operation does not free main channel after UCW 0 is formed. Before main channel can be released, main channel must fetch the first doubleword of data from main storage and place it in UCW 1. Because a second main storage fetch would make the operation too long, any subchannels requiring access to main channel are allowed to break in before the data fetch.

Outstanding Request - Allow Break-in: During the UCW 0 formation, a test is made for a subchannel's priority request and a write op code in the control register. These conditions set the outstanding request latch. After UCW 0 is formed, if the outstanding request latch is on (write op only), UCW 0 is stored in local storage and the ending trigger is set. 'Ending' establishes the point of return to the start I/O sequence by setting the multiplex data required latch, and allows other subchannels to break in by resetting the main channel busy latch. When main channel busy is reset, the subchannel

with highest priority is granted access to main channel and performs its operation. This continues until all requesting subchannels have been serviced. Main channel regains control by requesting priority (main channel priority request becomes active when main channel response is reset). When main channel again has priority, UCW 0 is again read out, the main channel clock is turned on, and the main storage data fetch is begun.

Write Data Fetch: To begin the initial data fetch for a write operation, the old UCW 1 is read from local storage to the data register. A main storage data fetch is signaled to BCU with the data address and key from UCW 0 (still in the control register). As in the CAW or CCW fetches, 'advance' indicates that the data is on the storage data bus out and the main channel uses this signal to gate the data into the data register.

While the doubleword of data is being fetched and placed in UCW 1 (in the data register) (FC111), the multiplex initial selection latch is set in the MSC. This causes the MSC to gate the device address from the main channel IUAR to the MSC UAR and to begin the initial selection sequence for the device. The data address field of UCW 0 is incremented by 8 and UCW 0 is stored. UCW 1 is now full and is stored also. A test is made for any errors that might have occurred during the data fetch.

If an error occurred, storage cycle check turns on the refetch 0 trigger and the error indication (data check) is set in UCW 0. The write operation is performed. However, when the count goes to zero (on the last CCW if CDA is indicated), the CSW formed will have the data check bit on. A data check suppresses chain command operations.

Assume that no errors occurred during the main storage data fetch. Ending is now turned on to release main channel, and multiplex data required is reset. Main channel is now free to perform other operations, but the CPU is not released until the initial selection of the device is completed.

Device Initial Selection

- Multiplex initial selection sets MSC selected and the device address is gated into the MSC UAR.
- The unit address is placed on the I/O bus out, and address out, followed by select out, is raised to the control unit.
- When a control unit recognizes the address, the control unit raises operational in followed by address in, and the control unit's address is placed on the I/O bus in.
- Select out is turned off, and the MSC compares the address in the MSC UAR with the address on the I/O bus in.
- 'Address match' indicates that the correct unit answered, and the I/O command is sent to the control unit with the command out tag.
- The control unit decodes the command and returns initial status and the status in tag.
- 'Status equal 0' gates 'accept' to main channel to release the CPU with condition code 00, and service out is raised to the control unit.
- Read or write operations continue under the control of main channel triggers 1-3 (FC801).
- COD-2.

All references are to Figure IOP 4 in the diagram manual, unless otherwise specified.

To select the MSC for the start I/O operation, the main channel activates the start I/O line to the MSC (A1). 'Start I/O' activates the CPU instruction line in the MSC, which removes the reset to the MSC selected latch (C2). When main channel activates the multiplex initial selection line, the tie-break latch sets the MSC selected latch (A2-B2). 'MSC selected' turns on the MSC clock (A5).

As stated in Chapter 2, the MSC clock is a three-level clock whose main purpose is to time I/O interface delays. The clock sequence continues to step as long as the input line is active. The MSC uses the clock to step through small portions of the I/O interface sequence and usually sets up the conditions for the next clock sequence during the current one. Therefore, when the clock is turned off at the end of a sequence, the turn-on conditions are usually set up for the next sequence.

For the first cycle, the clock is started by activating the MSC selected line to the clock. The MSC selected latch and the A1 MSC clock pulse cause the MSC to be reset. The A2 clock pulse and the MSC selected latch gate the main channel IUAR into the MSC UAR via the MSC unit address OR. The A3 clock pulse sets the initial selection and selected busy latches (B1-B2). With 'selected busy' set, the MSC selected gate to the MSC unit address OR is degated and the MSC clock is turned off (D5). This completes the first clock cycle.

Address Out and Select Out (FC801)

When the initial selection latch is turned on, the device address is gated from the MSC UAR onto

the I/O bus out to the control unit. The reset condition, 'not initial selection,' is removed from the initial selection and not address out latch (C2) to allow the MSC clock A2 delayed turn-off line to set a latch that turns on the MSC clock again (B4). At A2 time, an I/O bus out parity sample (even) is made and unit address check causes a CSW cycle with a channel control check indicated.

If parity is odd, the address out latch (FC803) is turned on (C3) by the A3 clock pulse. The address out I/O interface line is raised to the I/O control unit (C5). This line signals all control units to examine the address on the I/O bus out. If a control unit recognizes the address, it will respond with the operational in line when MSC raises the select out line.

With the address out latch set, the initial selection and not address out latch is reset to allow the initial selection and address out latch to be set (D3). This stops the MSC clock and removes the unit address from the I/O bus out.

The initial selection and address out latch turns the MSC clock back on and sets the select out latch (D3). 'Select out' resets the initial selection and address out latch to turn off the MSC clock (D3). The select out line is raised to the control unit (D5). The addressed control unit captures 'select out' and signals the MSC with 'operational in.' 'Operational in' remains active for the duration of the initial selection sequence.

If the address is not identified, none of the control units captures 'select out' and 'select out' returns to the MSC as 'select in.' 'Select in' with 'select out' active activates 'no selection' to main channel (E3). 'No selection' is sent to the main channel release circuits and the 2870 releases the CPU with condition code 11.

Operational In and Address In (FC803)

When a control recognizes the 'address on bus out' and captures 'select out,' the control unit raises 'operational in' to the MSC. 'Operational in' resets the address out latch (C3). When 'address out' falls, the control unit places its address on the I/O bus in and raises 'address in.' 'Address in' line remains active until the MSC responds with 'command out.' 'Address in' resets the select out latch, and 'select out' to the control unit falls.

The MSC compares the address in the UAR with the address in the MSC bus in OR (from the control unit). If the addresses do not match, or if the I/O bus in has bad parity, an interface control check is indicated and a CSW cycle occurs. However, when the addresses match, 'address match' sets the address match and A3 latch (F3) and the clock is turned off. 'Address match and A3' removes the reset to the address match latch and it is turned on by the A2 delayed turn off line (A6) (when the clock goes off).

Command Out

'Address match' turns on the MSC clock and gates the command byte onto the I/O bus out (FC803). The A2 pulse checks for a possible bus out parity check. If a bus out parity error occurs, command check is set and a CSW is formed with interface control check indicated (FC805).

If parity is odd, the A3 clock pulse sets the command out latch (B7) and 'command out' is signaled to the control unit. 'Command out' remains active until the control unit drops 'address in.'

'Command out' causes the control unit to gate in the command and drop 'address in.' With 'address in' down, the address match and A3 latch is reset (F3), which resets the address match latch (A6) and turns off the clock. With 'address match' reset, the command is removed from the I/O bus out and 'command out' is dropped.

Status In (FC805)

The control unit has decoded the command and determined whether the operation can be performed. A status byte is now placed on the I/O bus in and 'status in' is raised to the MSC. This status byte determines whether the I/O operation will be performed. A zero status byte indicates that the control unit has accepted the I/O command and the operation can proceed. Non-zero status is detected by the MSC, and causes a CSW cycle with the status byte stored in main storage; the CPU is released with condition code 01.

'Status in' from the control unit sets the status in latch (C6), which turns on the MSC clock. At A2 time, a MSC I/O bus in parity check is made. If a parity error is detected, a CSW is stored with the interface control check indicated and the CPU is released with condition code 01.

Assume that the status byte equals 0 and no parity errors occurred. The A3 clock pulse sets the service out (B8) and multiplex accepted (D7) latches. The 'service out' interface line is raised to signal the control unit that the status on the I/O bus in has been accepted. 'Multiplex accepted' resets the initial selection latch (B1) and signals the main channel release circuits to release CPU with condition code 00.

'Release' to the CPU causes 'start I/O' and 'select channel' to fall. This drops the CPU instruction line (A2), which resets the MSC selected latch (A3). Initial selection is now completed.

The execution of the I/O operation is dependent on the I/O device. When the device requires a data transfer, the control unit raises the 'request in' line to the MSC. A device service request sequence is performed on the I/O interface to allow the MSC to send or receive data from the I/O device. This sequence must be performed each time the device wishes to transmit data.

MULTIPLEX SUBCHANNEL READ/SENSE

- Read and sense operations are similar.
- Data or sense bytes are received from the I/O device.
- Bytes are assembled into doublewords and stored in main storage.
- Read-skip is similar to a read operation, except data is not stored in main storage.
- Read backward is similar to a read operation, except data is stored in main storage in reverse order.
- COD-3.

Sense

Read and sense are similar operations: information is transferred from the I/O device to main storage. Sense and read differ only in the type of information transferred when the respective commands are executed. In a sense operation, bytes that contain the correct status of the I/O device and unusual conditions that the device detected in the previous operation are transferred.

The quantity and meaning of the status information associated with the sense operation depend on the type of device. Status information provided in the sense bytes is more detailed than that supplied in the CSW. Explanations of sense status bytes are given in the functional descriptions for the device.

In read and sense operations, all five flags (CD, CC, SLI, skip, and PCI) are inspected. Modifier bits are in bit positions 0-5 for read, and in bit positions 0-3 for sense. The channel does not examine data bytes and does not recognize any difference between the read and sense operations.

Read

- The execution of a multiplex read operation depends upon the device demanding service.
- A multiplex device demands service by the control unit raising the request in line to MSC.
- 'Request in' causes the MSC to perform the device service request sequence to select the I/O device and request a main channel trigger 1 sequence.
- The main channel trigger 1 sequence controls the gating of the data bytes through the MSC to UCW 1 in the data register, takes care of main storage data transfers, updates UCW 0, tests for errors, and signals MSC when to end the sequence.
- A 'device service request' and trigger 1 sequence are performed for each byte of data read in.
- When trigger 1 determines, by the count, that a doubleword of data is assembled in UCW 1, trigger 1 stores the data in main storage.
- When the count for a read operation is exhausted, trigger 1 signals the MSC to raise 'command out' in response to 'service in' and stop the read operation.
- If the trigger 1 sequence detects the CDA flag when the count goes to zero, the CDA-CCW fetch sequence is begun.
- A chain command operation is detected by the trigger 9 (status/chain command) sequence.
- COD-3.

During a read or sense operation, the MSC accepts bytes of data from the I/O device via the I/O interface bus in and transfers the bytes to the main channel data register (Figure 3-16). The data register assembles the bytes into eight-byte doublewords and buffers each byte in local storage. When the eighth byte is received, it is not buffered in local storage. The completed doubleword is stored from the data register into main storage.

Data is stored in ascending order of addresses, starting with the address specified in the CCW. After the doubleword in the data register has been stored in main storage, the same doubleword is stored in UCW 1 of local storage.

During all data transfers (I/O device or main storage), main channel monitors for count equal zero. When count equal zero is detected, the I/O device is given a stop command ('command out' in response to 'service in'), a check is made for chain

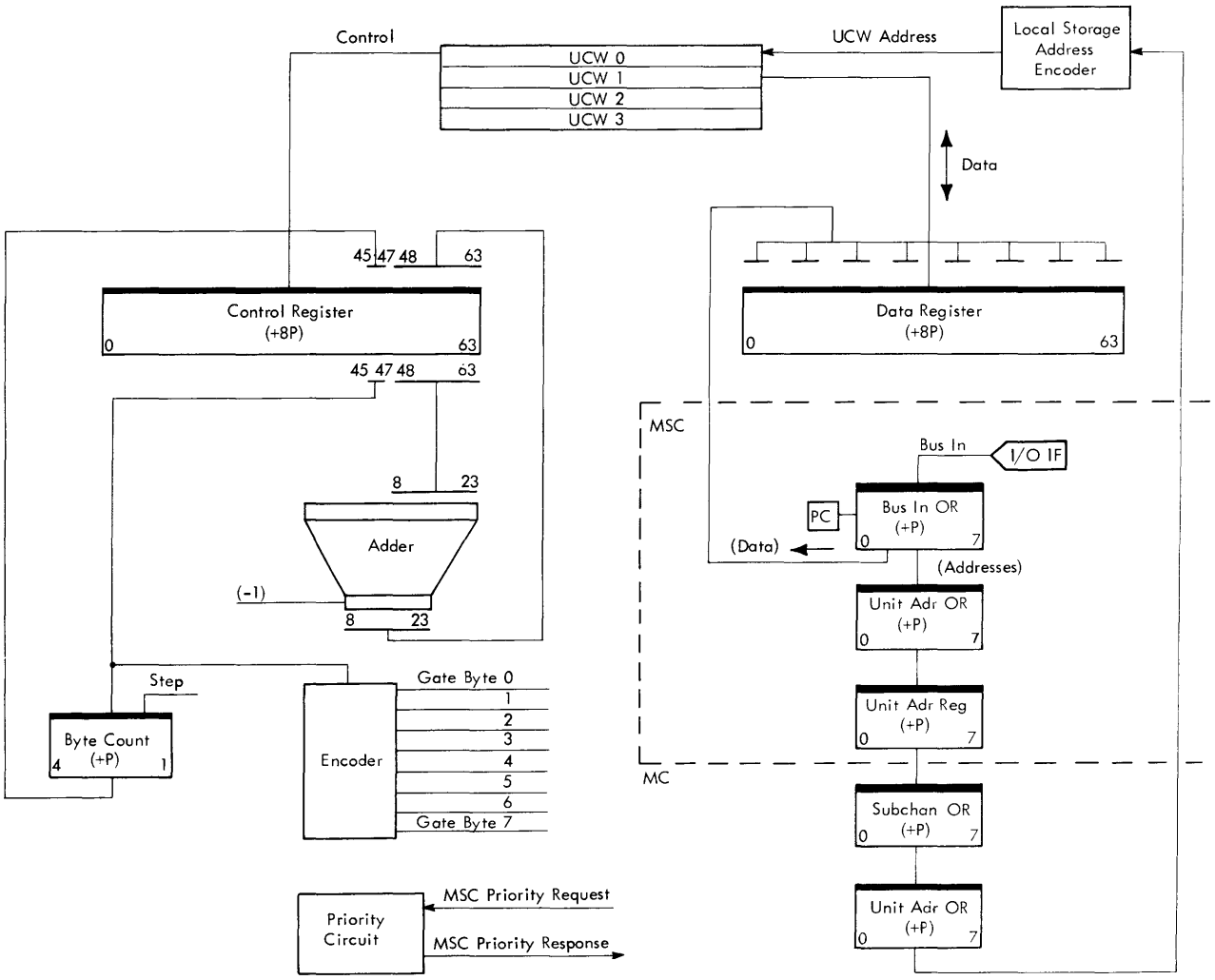


Figure 3-16. Multiplex Subchannel Read/Sense

flags, and either a CSW is formed or main channel performs the chain-CCW fetch.

Service Request (FC807)

After the start I/O initial selection sequence is completed, the multiplex subchannel's control information is stored in local storage and the 2870 waits for the device to request service. The control unit raises 'request in' to signal the MSC that the control unit requires service (Figure IOP 4, A1). The MSC answers 'request in' with 'select out.'

'Select out' is signaled by ANDing 'not MSC selected' and 'request in' to turn on the select out latch (Figure IOP 4, D3). The 'MSC selected' line is tested to be sure that a main channel start I/O-initial selection sequence is not already being performed. A main channel initial selection blocks 'device service request' at this time. 'Request in' also blocks the tie-break circuit so that, if main channel attempts to issue initial selection during this sequence, the initial selection will be locked out.

When the I/O control unit recognizes 'select out,' it raises its 'operational in' line, drops 'request in,' and places its address on the I/O bus in with 'address in.' 'Operational in' signals the MSC that the control unit is selected and is ready for an I/O operation. 'Address in' tells MSC that the address of the selected device is on the I/O bus in and the MSC should gate the address onto the bus in OR. When 'address in' rises, the device service request latch is set, the select out latch is reset, and the MSC clock is turned on.

At time A1, the device service request latch causes an MSC reset to clear MSC for this operation (FC807). The A2 clock pulse gates the device address into the MSC UAR and a parity check is made at this time. If a parity error occurs on the I/O bus in, a CSW is formed with the interface control check bit on.

If the address has correct parity, the command out interface line is raised at A3 time (Figure IOP 4, B7). 'Command out' signals the control unit that the address has been accepted and the control unit can proceed. When the control unit recognizes 'command out,' it drops the 'address in' line and removes the address from the I/O bus in.

The fall of 'address in' turns off the MSC clock, which then degates the command out signal to the control unit (Figure IOP 4, B9). When 'command out' falls, the control unit raises either 'status in' or 'service in.' 'Status in' indicates that the control unit wishes to present a status byte. However, because this is a read data transfer sequence, the control unit raises 'service in.'

'Service in' indicates to the MSC that the control unit has a byte of data on the I/O bus in. With the rise of service in, the MSC data cycle request latch is turned on by the 'operational in and service in' line (Figure IOP 6, A1). With 'device service request' on, the MSC requests main channel priority (Figure IOP 6, A4) (FC201). At this time, the MSC needs main channel's trigger 1 sequence to complete the handling of the read operation.

Trigger 1 (FC201)

'Data cycle request' causes the MSC to request main channel priority (Figure IOP 6, A4). When priority is granted, the priority circuit sends 'MSC response' and 'response delayed.' 'MSC response' and 'response delayed' are ANDed with 'data cycle request' to turn on trigger 1 and fetch UCW 0 (for the device) from local storage into the control register (Figure IOP 6, A3).

To fetch UCW 0, the device address is gated from the MSC UAR through the subchannel OR to the main channel UAOR. The main channel UAOR is gated onto the address lines to local storage. When the address is gated into the UAOR, a parity check is made. If a parity error occurs, the operation is terminated and a logout is performed. Because a local storage address check is considered a non-recoverable error, when the logout is completed the entire machine (including local storage) is reset. However, if the address has correct parity, a fetch is also begun for UCW 1 (to the data register) (Figure IOP 6, A3).

Because local storage handles only one fetch or store operation at a time, UCW 0 is fetched to the control register before UCW 1 is fetched to the data register. When UCW 0 is gated into the control register, the control register full latch is set. Main channel now waits for UCW 1 to be fetched. The completion of UCW 1 fetch into the data reg is signaled by the fall of 'local storage read/write extended.'

'Control register full' and 'not local storage read/write extended' turn on the main channel clock to control the trigger 1 sequence (Figure IOP 6, B4). At time T0, the subchannel count (in UCW 0) is examined. If the count is equal to zero, the count equal zero trigger is set. Count equal to zero indicates that the read operation was completed on a previous cycle and that the I/O device must be signaled to stop. 'Count equal zero' is sent to the MSC and causes the MSC to raise 'command out' to the control unit (Figure IOP 6, D2). The control unit interprets 'command out' in response to 'service in' as a stop command, and it immediately drops 'operational in' and 'service in' to disconnect itself from the interface. The MSC now resets the command out and device service request latches to end the sequence. Main channel stores UCW's 0 and 1 (Figure IOP 6, E2), turns off the main channel clock, and turns on the ending trigger to terminate the operation (Figure IOP 6, E2). A check is made for the SLI flag, and if SLI is not on, the incorrect length bit (4) is set in UCW 0. The ending could also have been caused by a previous halt I/O command to this subchannel (UCW 0 bit 5), or a control check, program check, or protect check in UCW 0. However, assume that the count is not zero, the halt I/O bit (5) is off, and reject does not exist (bits 41, 42, 43 = 0).

A non-zero count field indicates that more data transfers are required. Trigger 1 now sets up the main channel registers to control the read in of the data byte that is on the I/O bus in.

Because this could be the last byte of a doubleword, the DAB (bits 29-31) is set in the DAB register (Figure IOP 6, C3). Note that for

all main storage data transfers after the first, the DAB contains zeros. For the first main storage transfer, the DAB enables the marks encoder to set only the correct bytes into main storage if the data field does not begin on a doubleword boundary. For all main storage transfers, the DAB register is gated to one half of the marks encoder while the byte count register is gated to the other half. The combination of DAB and byte count bits results in activating the correct mark bits for any type of beginning or ending partial doubleword transfers to main storage.

The count field (bits 48-63) is gated to the adder, decremented by 1, and then set back in the control register (Figure IOP 6, B6). If the count goes to zero on this decrement, main channel causes the 'stop command' to be issued to the I/O device on the next data cycle.

The data address is gated from the control register to the adder (Figure IOP 6, B6) and is incremented by 8. This is done in case this sequence is also going to perform a main storage data transfer (byte count equal seven condition). Note that although the data address is incremented by 8 for each byte of data transferred, the new data address is not gated back into the control register unless a main storage data transfer is performed.

The PCI flag is examined also (FC201). If bit 36 (PCI) is on and the interrupt queue register is empty, the device address is gated from the UAOR to the interrupt queue register, the PCI and interrupt latches are set and 'interrupt request' is raised to CPU. If the PCI flag is on and an interrupt is pending in the queue for this device ('UAOR = queue'), the PCI flag is reset. If the queue is full and the UAOR address does not match the queue address, the PCI flag remains on and is tested on each succeeding data transfer cycle.

The byte count is now gated into the byte count latches and stepped by + 1 (Figure IOP 6, D8) (FC203). This points the byte count to the data register position we wish to gate the next data byte into. The output of the byte count field (control register 45-47) is sent to the gate encoder circuit to bring up the proper data register gate.

The data byte is now gated, from the MSC I/O bus in, into the proper data register location. The byte count register contents are then transferred to the byte count field (bits 45-47) of the control register, and main channel activates the 'service out' line to MSC.

'Service out to MSC' sets the MSC service out latch and 'service out' is raised to the control unit (Figure IOP 6, F6). 'Service out' indicates to the control unit that the data byte is accepted and the control unit can remove the data from the I/O bus in and disconnect from the I/O interface. The control unit disconnects from the I/O interface by dropping both 'operational in' and 'service in' (FC809). When MSC recognizes the fall of both 'operational in' and 'service in,' it resets the service out and device service request latches to end the device service request sequence. During the MSC service out sequence, MSC checks for a possible data parity error. If a data parity error occurred, the data check bit (44) is set in UCW 0. Meanwhile, the main channel trigger 1 sequence is continuing in parallel.

If the byte count equals seven (FC203), a doubleword is assembled in the data register and a main storage data transfer must be performed. Byte count equal seven activates the data store line. 'Data store' sets the data cycle request and storage cycle latches to cause a main storage data transfer. A normal 2870-to-BCU storage sequence is performed and the data register contents (UCW 1) are placed on the storage data bus in when 'BCU data request' rises. On this cycle, the incremented data address (+8) is returned to the data address field of UCW 0 (bits 8-31). Although the contents of UCW 1 are stored in main storage, UCW 1 is also returned to local storage without being reset. The contents of UCW 1 will be changed as each new data byte is gated into it. This same main storage sequence would have occurred if the count was decremented to zero on this cycle (a count of zero indicates that the data transfer is complete).

A test is made for any data parity errors which might have occurred during this cycle. If a data parity error occurred, the data check bit (44) is set in UCW 0. Note that a data check does not stop the read operation, nor does it interrupt a chain data address sequence. Data check blocks chain command operations, and causes the CSW formed at the termination of all data transfers to have the data check bit on. After the test for data errors, UCW 0 is stored in local storage and the ending trigger is set. 'Ending' frees main channel for other operations; the trigger 1 sequence is complete.

Each time the I/O device has a byte of data to transmit, the device service request and trigger 1 sequences are executed. This continues until the count is decreased to 1. On the next data transfer cycle, the count goes to zero and the CDA flag is tested. If the CDA flag is on, the next CCW is fetched during this sequence because this is the last data byte transfer for the current CCW. The details of the CDA-CCW fetch are found in the read-CDA description. If the CDA flag is off, the last byte of data is transferred over the I/O interface into the data register and the last main storage

transfer is performed. The 2870 has completed the read operation and waits for the device to present its ending status byte.

The read operation at the I/O device can end in two ways: either the device presents status information on the cycle following the last data transfer, or the device requests one more data transfer and the 2870 detects a count of zero and answers with 'command out' (stop command) (FC809). If a 'stop command' is given, the device must raise 'request in' and 'status in' to present its ending status information (FC807).

When the I/O device presents its ending status information, main channel's trigger 9 is turned on (FC811) to handle the formation of a CSW and to check for the chain command flag. If the chain command flag is on in UCW 0 and the device end bit is on in the status byte, the multiplex pseudo start I/O latch is set to cause the multiplex start I/O-CCW fetch sequence to be performed. The CCW fetch sequence is described in the multiplex chain command section. If chain command is not indicated, the trigger 9 sequence performs part of the CSW sequence and turns on trigger 10. Trigger 10 completes the CSW assembly, places the CSW in UCW 2, and turns on interrupt request to CPU. When CPU answers the interrupt request with 'interrupt response,' the CSW is transferred to main storage under trigger 11. The storing of the CSW marks the end of the read operation.

Read Backward

A read backward operation is performed in the same manner as a read operation, except that the data is stored in main storage in reverse order. To assemble the data bytes in storage in the original sequence, the bytes are stored in descending order of addresses, starting with the highest storage address instead of the lowest address of the data area.

On Figure IOP 6, read backward is performed in the same manner as read, except for the data address update and byte encoder gating. 'Read backward' causes the data address to be decremented by 8 (FC201) (Figure IOP 6, B6). The output of the byte count field (control register bits 45-47) is inverted to cause the data bytes to be gated into the data register in reverse order. Because a complement DAB initializes the byte count and DAB fields during the start I/O sequence, the data bytes begin and end at the correct addresses and the byte count equal seven signal still controls main storage data transfers. As in the read operation, 'count equal zero' terminates the read backward operation.

Read-Skip

A read-skip operation is performed in the same manner as a read operation, except that data is not stored in main storage (FC203). When the byte count equals seven, indicating a complete doubleword has been assembled in the main channel data register, the flags of UCW 0 in the control register are inspected.

If the skip flag is on (a 1 in bit position 35), a storage cycle is not requested. UCW 1 is stored from the main channel data register into local storage. A test is made for data checks; if there are no data checks, UCW 0 is stored in local storage. The ending trigger is turned on and the operation is terminated.

Chain Data Address (Read/Read Backward)

- If the CDA flag is on (bit 32 of UCW 0) a new CCW is fetched when the last data byte is transferred for the current CCW.
- The new CCW is modified to form a new UCW 0, and the operation continues.
- Trigger 1 sequence handles the data byte transfer and stores the last doubleword of data in main storage.
- The CDA-1 trigger is turned on to set CDA condition and to identify the operation as a multiplex CDA-CCW fetch.
- Trigger 2 sequence commences the CCW fetch and forms a new UCW 2.
- Trigger 3 sequence forms and stores a new UCW 0.
- COD-11.

After performing the data transfer specified by a CCW, the operation (read or read backward) initiated by start I/O can be continued by chaining (fetching a new CCW). Every data byte transfer is performed by the device service request and trigger 1 sequences. Each time a trigger 1 sequence (FC203) is performed, the count field of UCW 0 is examined for the count equal 1 condition. 'Count equal 1' indicates that this is the last data byte transfer for this CCW. If the count equals 1 and the CDA flag is on (bit 32 of UCW 0), the CDA-1 trigger is turned on (Figure IOP 6, A11) (FC205). The CDA-1 trigger initiates the chaining sequence by turning on the CDA condition latch (Figure IOP

6 (E11) and blocking the normal setting of the ending trigger at the completion of the trigger 1 sequence.

With CDA-1 and CDA-condition set, the normal trigger 1 data read sequence is performed. However, during this sequence, CDA condition blocks the 'command out' (stop command) signal which would normally be sent to the control unit on this cycle. Therefore, the device is not released by the CDA sequence. During this trigger 1 sequence the last main storage data transfer is performed for the current CCW. The final main storage data transfer is caused by the count of UCW 0 going to zero on this cycle. Also during this sequence, UCW 1 is not stored in local storage as in a normal read operation, but remains in the data register and is stored by trigger 2.

After the main storage cycle for the data is completed, 'CDA condition' gates bits 6, 7, 36, and 44 of the control register to buffer latches, resets the control register full latch, and begins a local storage fetch for UCW 2 (Figure IOP 6, C26). Bits 6, 7, 36, and 44, the operation code (6, 7), PCI, (36), and data check (44), are saved in the buffer latches to be inserted in the new UCW 0 to be formed by the trigger 3 sequence (FC205). 'Control register full' is reset to allow UCW 2 to be read into the control register. When the word 2 fetched line becomes active, trigger 2 is turned on to begin the CCW fetch sequence and the main channel clock is turned off.

Trigger 2

The trigger 2 sequence fetches the new CCW from main storage using the address contained in UCW 2, updates UCW 2, stores the new UCW 2 in local storage, and turns on trigger 3 (FC207).

Trigger 2 is turned on when 'word 2 fetched' becomes active. When UCW 2 is gated into the control register, the control register full latch (just turned off by trigger 1) is set again. A check is made to be sure that the data store cycle, performed under trigger 1, is completed and that no errors occurred. If no errors occurred, 'control register full' and 'not storage cycle' (main storage) restart the main channel clock (Figure IOP 6, A21). At this time, the command address field (bytes 1-3) of UCW 2 is gated from the control register to the adder (Figure IOP 6, B22). From the adder, the command address is gated to the residual command address field (bytes 5-7) of the control register. This is done to preserve the old CCW address in UCW 2 in case an error occurs. The CCW request latch is set to begin the storage request for the new CCW (Figure IOP 1, E11). Also at this time, UCW 1 (left in the data register by the trigger 1 sequence) is stored in local storage.

To perform the CCW fetch, 'storage request' is raised to BCU (FC551), the command address is gated to the SAB register, and a normal BCU-to-2870 storage fetch sequence is performed to fetch the new CCW. To complete the trigger 2 sequence, a new UCW 2 must be formed.

Bytes 1-3 of the old UCW 2 (command address field) are still in the adder (Figure IOP 6, B22), and have also been gated to bytes 5-7 of the control register to form the new residual command address field. The contents of the adder are incremented by +8 to form the new command address (Figure IOP 6, C22). This new address is gated into control register bytes 1-3 as the new command address field of UCW 2. UCW 2 is now updated; therefore trigger 2 is reset, trigger 3 is set, UCW 2 is stored, and the main channel clock is turned off (Figure IOP 6, B24).

Trigger 3

When the new CCW arrives from main storage, it is gated into the data register by 'CCW advance,' and from the data register to the control register by 'CCW late advance' (FC551). Because this is a CDA operation, the operation code (bits 6 and 7), PCI (bit 36), and data check (bit 44) bits are gated into the control register with the new CCW. This causes the old operation code to be saved and propagates the PCI and data check indications. The storage cycle over latch is now set. If no errors occurred, 'storage cycle over and no check' becomes active. 'Storage cycle over and no check' and trigger 3 turn on the main channel clock. A new UCW 0 must now be formed from the CCW.

As in the start I/O sequence, the op code determines the form of the DAB bits used to form UCW 0. The op code (bits 6 and 7) is examined for read or read backward (FC209). For a read operation, the DAB (bits 29-31) is gated in true form to the DAB register (Figure IOP 6, E22). A read backward operation causes the DAB to be set in the DAB register in complement form. The corrected form of the DAB (true or complement) is always gated from the DAB register to the byte count field (bits 45-47) of the control register, and to the DAB field also (bits 29-31) if read backward is specified. The new UCW 0 now has the correct DAB field to control the mark gating for the first main storage data cycle and the correct starting value in the byte counter. UCW 0 is stored in local storage. When the 'word 0 fetched line' becomes inactive, the ending latch is set to free main channel for other operations.

The read or read backward operation continues with data storage starting at the new data address. When the count is again 1, a test is made for the CDA flag in this new CCW. If the CDA flag is also on in this CCW, another CDA-CCW fetch sequence is performed. If chaining is not indicated, the operation ends in the same manner as the read operation. Notice that CDA does not release the device by issuing a 'stop command' at the end of the first CCW. Therefore, the device remains selected and continues its read or read backward operation regardless of the fact that the 2870 has chained CCW's.

MULTIPLEX SUBCHANNEL WRITE/CONTROL

- Write and control commands are executed by the main channel in the same manner.
- The control unit detects the difference between write and control operations.
- Write operation requires transfer of data from main storage to the selected I/O device.
- Control operation may not involve data transmission.
- COD-4.

Control

A control command is executed in the same manner as a write command. The difference between write and control operations is detected by the control unit. The channel does not distinguish between write and control commands. Execution of a control command does not usually require data transmission across the interface.

After the main channel designates the specific control operation in the command byte, the addressed I/O unit performs the operation without intervention from the channel. The operations that can be performed by a control command depend on the particular device selected. For example, a control command can initiate a rewind, backspace, or forward space operation on a magnetic tape unit.

If the command code does not specify the entire control function, the data address field of the CCW designates the memory location that contains the required additional information. The CD, CC, SLI, and PCI flags are examined for a control command.

Write

- The execution of a multiplex write operation depends on the device demanding service.
- A multiplex device demands service by the control unit raising the request in line to the MSC.
- 'Request in' causes the MSC to perform the device service request sequence to select the I/O device and request a main channel trigger 1 sequence.
- The trigger 1 sequence controls the gating of data bytes from UCW 1 through the MSC to the device, takes care of main storage fetches, updates UCW 0, tests for errors, and signals MSC when to end the sequence.
- When the count for a write operation is exhausted, trigger 1 signals the MSC to raise 'command out' in response to 'service in' and stops the operation.
- COD-4.

In a write operation, data is transferred from main storage to the selected I/O device. The CCW designates the initial address in main storage from which data will be transferred. Data is fetched in ascending order of addresses. The write CCW is examined for CC, CD, SLI, and PCI flags (FC201).

The intercommunication between the MSC and control unit that is required to initiate an I/O operation is the same for a write operation as that previously described for a read operation. See "Multiplex Subchannel Read/Sense."

When service in is raised from the control unit, the operational in and service in line (Figure IOP 6, A1) turns on data cycle request latch (FC807). The data cycle request latch generates a request for main channel priority circuits (Figure IOP 6, A4). 'MSC response' and 'response delayed' from the priority circuits indicate that the requested priority has been granted. Trigger 1 is turned on (FC201), and UCW 0 is fetched from local storage into the control register (Figure IOP 6, A3). Trigger 1 fetches UCW 1 from local storage into the main channel data register. When UCW 0 is gated to the control register, the control register full latch is turned on. This latch turns on the clock (Figure IOP 6, B6).

The count of UCW 0 in the control register is examined. If the count equals 0, the count equal 0 latch is turned on. A 0 count indicates an end to data transmission, and 'command out' is turned on to stop the operation. 'Command out' response to 'service in' always means stop, and signals the control unit that the channel is ending the current operation.

UCW 1 in the data register and UCW 0 in the control register are stored in local storage. The ending trigger is turned on and the operation is terminated (Figure IOP 6, E2). However, if the count is not equal to 0 and the byte count equals 7, the data fetch and data cycle request latches are turned on (Figure IOP 6, E6) (FC203).

With the data cycle request latch set, the storage cycle request line is raised to the BCU to obtain a doubleword of data. The BCU grants the request and the data storage cycle is executed. The data fetch latch gates the data from the storage data bus out (SDBO) to the data register. The count is gated to the adder, decremented, and gated back to the count field of UCW 0 in the control register.

The DAB (bits 29-31) of UCW 0 in the control register is gated to the DAB register (Figure IOP 6, C3). The data address of UCW 0 is gated from the control register to the adder (Figure IOP 6, B6), and is incremented by 8 to create the new data address. This incrementing of the data address occurs for each byte of data transferred. The new data address is not gated back to the data address field of UCW 0 until a data transfer is made from main storage.

As in the case of the read operation, the byte count operation is being executed as a parallel operation. The byte count is gated from the control register to set the byte count latches (Figure IOP 6, D8). The byte count is increased by 1 (Figure IOP 6, D8) and is gated back to the byte count field of UCW 0 in the control register. 'Service out' is turned on to the control unit to indicate that the requested data has been provided on bus out.

Meanwhile, UCW 1 is stored from the data register (Figure IOP 6, C6). The data in the data register is gated to the I/O bus out (Figure IOP 6, D6). UCW 0 with its updated address and count is stored back in local storage. The ending trigger is turned on and the operation is terminated.

Write CDA, Count Less than Eight, and Do Prefetch CDA 3

- When count is less than 8, a new CCW is fetched and stored in UCW 3.
- Command address is flushed to residual command address.
- Command address is incremented by 8.
- New command address is gated back to the control register.
- CCW fetch latch is set and a CCW fetch cycle is initiated.
- The new CCW is modified to a UCW format and is stored in UCW 3.
- COD-13.

If the CDA flag is on (a 1 in bit position 32) and the count is less than 8, the CDA 3 trigger is turned on (Figure IOP 6, D10) (FC205). With the CDA 3 trigger set, CDA condition latch is turned on (Figure IOP 6, E12). 'CDA condition' gates the turnoff of 'control register full' and fetches UCW 2 into the control register (Figure IOP 6, F12). Trigger 2 is turned on and the clock is turned off (Figure IOP 6, D27).

When UCW 2 is gated into the control register, the control register full latch, which was just turned off, is again turned on and the clock is restarted. 'Fetch UCW 3' is generated and 'block' is turned on (FC207). 'Block' prevents UCW 3 from being gated into the control register. Since a fetch must precede a store, this local storage cycle was taken to allow the CCW, which is prefetched, to be stored in local storage UCW 3.

The command address of UCW 2 in the control register is gated to the storage address bus (SAB) register and to the adder (Figure IOP 6, B22). This command address is flushed to the residual command address field of UCW 2 in the control register. The CCW request latch is turned on to initiate a storage cycle for the new CCW (Figure IOP 1, E1). The command address in the adder is incremented by 8 (Figure IOP 6, C22) to form the new command address.

This new command address is gated back to the command address field of UCW 2 in the control register; UCW 2 is stored in local storage and trigger 3 is turned on (Figure IOP 6, A24). The clock is turned off and trigger 2 is reset (FC209). When the storage cycle over latch is set, an error check is made. If there are no errors, the clock is turned on. The DAB register is gated to bits 29-31 and the byte count field in the control register (Figure IOP 6, D22). The new CCW, now in UCW form, is stored in UCW 3, the ending trigger is set, and the operation is terminated (Figure IOP 6, E14).

Write CDA, Count Equals One, Prefetch Bit On, and CDA 2

- When the count equals 1, the prefetched CCW in UCW 3 is fetched into the control register.
- Service out is turned on.

- The new CCW is stored in local storage as UCW 0.
- A doubleword of data is stored in local storage as UCW 1.
- COD-12.

As stated in Chapter 1, after performing the transfer of data specified by a CCW, the activity initiated by start I/O can be continued by chaining (fetching a new CCW). In a write operation after the multiplex data cycle request latch is turned on (FC201), trigger 1 is set for the data transfer sequence and UCWs 0 and 1 are fetched. The main channel clock is turned on and UCW 0 is examined. If both the CDA and prefetch flags (bits 32 and 39) are on and the count equals 1, the CDA 2 latch is turned on (FC205). UCW 3 (containing the prefetched CCW) is read out of local storage into the control register (Figure IOP 6, E12). Service out is raised and trigger 4 is set (Figure IOP 6, F6); then the main channel clock is turned off.

The main channel clock is restarted and the data fetch request latch is turned on to initiate a data cycle (FC211). The data address is gated from UCW 3 in the control register to the adder and is incremented by 8 (Figure IOP 6, C22). The incremented data address is transferred back to the control register as the new data address. The control register contents are stored in local storage as UCW 0. The data word in the data register is stored in local storage as UCW 1. The ending trigger is turned on and the operation is terminated.

MULTIPLEX SUBCHANNEL CHAIN COMMAND

- To begin chain command operation, the control unit raises 'request in.'
- The MSC performs a device selection sequence and the control unit answers with 'status in' and a status byte.
- MSC requests priority for a trigger 9 CSW cycle.
- Trigger 9 reads out UCW 0, detects the chain command flag, stores any remaining data, and examines the status byte.
- If interrupt status is not present, trigger 9 turns on the multiplex chain command latch; then the multiplex pseudo start I/O and the MSC-CCW-CC required latches are set.
- 'Multiplex pseudo start I/O' and 'MSC-CCW-CC-required' cause main channel to fetch the next CCW in the same manner as for start I/O.
- While the main channel is fetching the next CCW, the MSC begins to reselect the I/O device.
- If the device returns status equal to 0 during the reselection, the chained command is considered accepted.
- Non-zero status returned during reselection causes the I/O operation to terminate and a CSW is formed by triggers 9 and 10, or the status is stacked in the device.
- COD-15.

A chain command operation begins as though the I/O device were requesting service for a data transfer (FC807). The control unit raises the 'request in' line on the I/O interface. 'Request in' causes the MSC to perform the device service request sequence. This sequence proceeds as though the device were going to request a read or write data transfer. However, instead of raising 'service in,' the I/O device raises 'status in' and places a status byte on the I/O bus in.

'Status in' causes the MSC to make a main channel priority request for a MSC status cycle (FC811). When priority is granted, trigger 9 is turned on (FC311). Trigger 9 fetches UCW 0 to the data and control registers. UCW 0 is examined for data left from an input type operation (count = 0, byte count not = 0), and the chain command flag. Data left from an input operation is stored in main storage during this trigger 9 sequence. Chain command causes the multiplex CC latch to be set; trigger 9 is turned off.

With trigger 9 off and the multiplex CC latch on, 'service out' and 'suppress out' are raised on the I/O interface and the multiplex pseudo start I/O and the MSC-CCW-CC-required latches are set.

'Service out' causes the control unit to disconnect from the interface. 'Suppress out' blocks any other control units from requesting service until the MSC reselects the device we are working with. At this time, the device end bit (in the status byte) sets the CC sync and CC control latches in the MSC, and causes the MSC to begin reselecting the I/O device. However, this reselection differs from start I/O in that the command out cycle is not performed until main channel signals that the CCW is ready to be used. This is signaled by the setting of the CC command loaded latch.

While the MSC is beginning reselection, the ending latch is set to free main channel. However, main channel priority request now becomes active because the multiplex pseudo start I/O latch is on. This allows the SSCs to break into main channel for any necessary data transfers and also drops the

priority level of the chain command operation to the main channel level.

When main channel receives priority, the device's unit address is gated to the UAOR and UCWs 0 and 2 are read out of local storage. 'Multiplex pseudo start I/O' and 'MSC-CCW-CC-required' cause the start I/O-CCW fetch sequence to begin as though this were a start I/O. However, initial selection is not sent to the MSC (not necessary because MSC is already effectively selected), and both 'multiplex pseudo start I/O' and 'MSC-CCW-CC-required' are turned off as they become unnecessary. As in start I/O, the new I/O command is examined for input or output type. An input type command (read) is allowed to complete reselection without interruption. However, an output type (write) command must first allow the SSCs to break in, next fetch the first doubleword of data, and then complete the reselection. To signal the MSC to complete the reselection, 'CC command loaded' is set after the CCW modification for input operations or after the first doubleword of data is fetched for output operations.

'CC command loaded' causes the MSC to gate the new I/O command from the CC command register to the I/O bus out and raises 'command out.' The control unit examines the command and returns 'status in' and a status byte. The status byte is examined. If it is zeros, 'service out' is signaled to the control unit, the last chain command control latches are reset, and the 2870 waits for the I/O device to demand data service. Non-zero status causes the MSC to request a trigger 9 CSW cycle and either a CSW is formed and stored in UCW 2, or, if the interrupt queue register is full, the stack status bit is set in UCW 2 and the status is stacked back in the control unit.

Chain Command Operations

'Request in' from the control unit (FC807) blocks the turn-on for the MSC selected latch and turns on the select out latch. When the control unit recognizes 'select out' in response to 'request in,' it raises 'operational in' and 'address in' and places its device address on the I/O bus in.

'Operational in' and 'address in' turn on the MSC clock and set the device service request latch; 'select out' to the control unit falls. At A1 time, 'device service request' causes the MSC to be reset. At A2 time, the I/O bus in is gated into the MSC UAR and parity of the address is checked. A parity error causes a logout with interface control check indicated. Assume that the address has correct parity. At A3 time, the MSC raises 'command out.' The control unit now drops 'address in' and the address on the I/O bus in. The fall of address in turns off the MSC clock and degates the 'command out' signal.

When 'command out' falls, the control unit raises 'status in' and places a status byte on the I/O bus in. Assume that this status byte has only 'channel end' and 'device end' on. 'Status in' turns on the MSC clock again. At time A2, the parity of the status byte is checked. If a parity error is detected, a logout is performed with interface control check indicated. Assume that parity is good. At time A3, status cycle request is turned on and a MSC priority request is made to main channel. When priority is granted, trigger 9 is turned on.

Trigger 9 (FC811 & FC311)

All references in this section are to Figure IOP 43, unless otherwise specified.

UCW 0 is fetched at the same time trigger 9 is turned on (A4). Main channel now begins to perform a normal trigger 9 CSW assembly. The op code, data check, and PCI bits (6, 7, 36, 44) are saved in buffer latches (B2). UCW 0's channel status bits are moved into their special latches (B2).

If the op code field of UCW 0 indicates read or read backward, the count field is zero, and the byte count is not zero, the data sequence latch is set (E2). 'Data sequence' indicates that an input (read) operation was terminated by the device and UCW 1 still has data that must be stored in main storage. UCW 1 is fetched into the data register and the DAB and byte count are gated from the control register to their respective registers (B7). To prevent any more data storage requests, the byte count field of the control register is now reset (C7). A main storage cycle request is made by setting the data cycle latch (C7) (FC551). UCW 1 is stored back into local storage. When BCU response rises, the data register contents are sent to main storage with the marks encoded from the byte count and DAB registers. UCW 0 is stored in local storage (E6). The chain command flag causes the multiplex chain command latch to be set (D6) and trigger 9 to be reset (E8) (FC313). The CSW assembly turns into a chain command operation and the CSW operations are ignored.

Because the multiplex chain command latch is on, 'service out' and 'suppress out' are raised to the control unit (E8) (FC319). Further, if the 'device end' bit is on in the device status byte, the multiplex pseudo start I/O and the MSC-CCW-CC-required latches are set in main channel (D8). 'Ending' is turned on to free main channel for other subchannel data transfers (E8).

'Service out' causes the I/O control unit to drop all "in" lines and disconnect from the I/O interface. 'Suppress out' blocks all control units from requesting service during this sequence (FC809). When the MSC sees 'operational in' and 'status in' fall, it sets the CC sync and CC control latches (FC801) because 'device end' is present. 'CC sync' blocks the turn-on of MSC selected (Figure IOP 4, B2). 'CC control' is ORed with 'MSC selected' to cause the MSC to begin reselection of the I/O device (Figure IOP 4, A3).

At this time, conditions are set up in main channel to cause a start I/O type CCW fetch (because multiplex pseudo start I/O and MSC-CCW-CC-required are on) (FC319). The MSC is ready to begin reselecting the I/O device (because CC sync and CC control are set). Main channel is now available to the SSC's for data or CCW transfers. Main channel priority request is active because the MSC pseudo start I/O latch is set.

CCW Fetch

When priority is granted to main channel, 'multiplex pseudo start I/O' (FC101) causes the MSC UAR contents (address of device performing chain command operation) to be gated to the main channel UAOR. The MSC-CCW-CC-required latch (FC103) causes UCW 2 to be read from local storage for a CCW fetch (FC105) 'MSC-CCW-CC-required' is ORed with 'CCW required' to cause a CCW fetch sequence to begin. While the CCW is being fetched, UCW 2 is being updated and stored in local storage. When the new CCW arrives, a new UCW 0 is formed from it. (Details of the CCW fetch and the UCW 0 and 2 operations are in the CCW Fetch and CCW in Channel sections of "Multiplex Subchannel Start I/O.") This operation is different in that 'initial selection' is not sent to the MSC (because it is already selected), and 'multiplex pseudo start I/O' causes the MSC-CCW-CC-required latch to be reset when 'CCW in channel' is set. Also, the new I/O command is gated into the CC command register (instead of the command register) when the CCW arrives.

The chain command CCW fetch operation differs in one other respect. Because the MSC begins to reselect the I/O device in parallel with the main channel CCW fetch, a CC command loaded signal is used to tell the MSC when to complete the device selection sequence (FC109). This signal is sent instead of the multiplex initial selection signal (sent after main channel has completed its operations). 'CC command loaded' causes the MSC to gate the I/O command from the CC command register to the I/O bus out and signal 'service out.'

As in a start I/O operation, a break-in is allowed if a write data fetch must be performed. As stated previously, 'initial selection' is not sent to the MSC, but 'CC command loaded' is sent after the write data fetch is over. Details of the break-in and write data fetch operations are in the Write Operations section of "Multiplex Subchannel Start I/O."

At the end of the CCW fetch sequence, the multiplex pseudo start I/O and (if on) the multiplex CC data required latches are reset, and the ending trigger is set. Ending frees main channel for other operations.

Device Reselection

All references in this section are to Figure IOP 4, unless otherwise specified.

When the CC sync and CC control latches are set (FC801), the MSC begins to reselect the I/O device. 'CC sync' blocks the turn-on of the MSC selected latch (B2). 'CC control' is ORed with the output of the MSC selected latch to cause the MSC to begin an initial selection sequence (A3).

The MSC clock is turned on (A5). At time A1, the MSC is reset (A5). At time A2, 'CC control' blocks the gating of the MSC UAR because the UAR already contains the address of the device we wish to select (placed there during the device service request sequence) (B4). The device reselection now proceeds in the same manner as a start I/O device selection described in the Device Initial Selection section of "Multiplex Subchannel Start I/O." However, when the device has returned its address and 'address match' has been determined, the MSC needs 'CC command loaded' to remove the reset to the address match and A3 latch (F3). Therefore, the MSC waits at this point in the reselection until main channel finishes the CCW fetch and possible write data fetch.

When main channel completes its operations, it signals the MSC with 'CC command loaded.' 'CC command loaded' allows the address match and A3 latch to set (FC803) (F3), and causes the MSC to gate the contents of the CC command register to the I/O bus out. 'Command out' is raised to the control unit (B9).

As in start I/O, when the control unit receives 'command out,' it examines the command on the I/O bus out, and returns 'status in' with a status byte on the I/O bus in. The status is examined. If it is zero, the I/O command is considered accepted and MSC returns 'service out.' The 2870 now waits for the I/O device to demand data service.

If the status byte is not 0, the I/O command is considered rejected and the MSC requests priority for a trigger 9 CSW cycle.

MULTIPLEX SUBCHANNEL HALT I/O

- CPU sends 'select' and 'halt I/O' with a unit address for a device.
- If an interrupt is pending for the addressed device, CPU is released with condition code 00 (FC131).
- If no interrupt is pending for the device, the multiplex initial select latch is set and main channel is released.
- If the MSC I/O interface is in burst mode, the address out line is raised to disconnect the burst mode device from the I/O interface and CPU is released with condition code 10.
- If the MSC I/O interface is in byte mode, an initial selection sequence is begun to select the I/O device and issue 'halt I/O' to it.
- When 'halt I/O' is issued to the addressed device, the trigger 7-7A sequence is executed to place a two-byte (bits 32-47) CSW in main storage and CPU is released with condition code 01.
- During the initial selection sequence, it is possible for the device to return status information stored in the CSW (CU Busy); CPU is released with condition code 01.
- Regardless of the status of the device, the halt I/O bit (5) is turned on in UCW 0 of the addressed device.
- If 'select in' returns during the device selection sequence, the CPU is released with condition code 11.

All references are to Figure IOP 3 in the 2870 FE Diagram Manual (Form Y27-2153) unless otherwise specified.

The CPU initiates the halt I/O instruction by raising the halt I/O line to the channels (A1), placing an eight-bit unit address on the unit address bus out, and signalling the 2870 with the select channel line (A1). 'Halt I/O' and 'select channel' generate a main channel priority request (A3). When priority is granted, 'main channel response' (FC111) and 'response delayed' become active.

'Main channel response' causes the unit address to be gated from the unit address bus out, through the initial unit address register, to the unit address OR (A4). 'Response delayed' sets the halt I/O latch (B1) (FC103 & FC131) and turns on the main channel clock (B1). The unit address OR is compared with the contents of the interrupt queue register. If the addresses match and PCI is not indicated, CPU is released with condition code 00. Condition code 00 indicates to the CPU that the addressed device has an outstanding interrupt, and would transfer status information to main storage if 'interrupt response' or 'test I/O' were activated by CPU. If the addresses do not match, the 'multiplex initial select' (D1) and 'ending' (C4) latches are set. 'Ending' frees the main channel for other operations and 'multiplex initial select' attempts to begin a device selection sequence in the MSC. Two conditions are possible on the MSC I/O interface: the interface can be in burst mode or in multiplex mode.

Halt I/O with MSC I/O Interface in Burst Mode

When halt I/O is issued for a multiplex device, it is possible for the MSC I/O interface to be in burst mode. If the I/O interface is in burst mode, the MSC waits for 'service in' to fall (so that halt I/O does not cause a data byte to be lost), and then raises the address out line on the I/O interface. 'Address out' without 'select out' causes the burst mode device to disconnect from the I/O interface immediately. This interface disconnect signal is given regardless of the address of the device operating in burst mode. When the device drops 'operational in,' the MSC requests main channel priority for a triggers 7 (FC307) and 7A (FC309) status sequence.

The trigger 7A sequence turns on the halt I/O bit (5) (FC309) in UCW 0 of the addressed device, to cause the device to receive a 'stop command' ('command out' in response to 'service in') the next time it requests service on the I/O interface.

The trigger 7 sequence does not form a CSW when a burst mode device is halted. The burst mode indication from the MSC is retained and used to block trigger 7 from sending status to CPU, and causes main channel to release CPU with condition code 10 (FC113). Condition code 10 tells CPU that a burst mode I/O device was halted on the MSC I/O interface. No interrupts remain pending and the MSC I/O interface is blocked until CPU drops 'halt I/O' and 'CPU select channel.'

The setting of the multiplex initial select latch in main channel causes several things to occur in the MSC. First, an attempt is made to set the MSC

selected latch (A7) by raising the 'multiplex initial select' (A5) and 'CPU instruction' (B6) lines. Then, if the MSC selected latch is blocked by a burst mode operation on the MSC I/O interface-- 'operational in' blocks the tie break circuit (A5), the MSC busy logic begins to time out (D2). If 'operational in' remains up for 64 usec after 'multiplex initial select' becomes active, the interface busy latch is set (D2). 'Interface busy, ' 'operational in' and 'not service in' condition an AND circuit to set a latch to activate the 'halt I/O and MSC busy' line (FC801) (E2). The same AND circuit also causes 'address out' to be raised on the MSC I/O interface (E4). When the I/O device on the interface recognizes 'address out' without 'select out' it immediately disconnects itself from the I/O interface by dropping all "in" tags.

The fall of 'operational in' degates the AND circuit that causes the halt ('address out') to allow another AND circuit to raise the 'halt I/O and MSC busy to main channel' line (F2). 'Halt I/O and MSC busy to main channel' sets the status cycle request latch (F3). 'Status cycle request' becomes active to main channel and also causes an MSC priority request to main channel (F3). When MSC priority response and response delayed are raised by the priority circuit, 'sample status cycle' and 'initial selection to main channel' are also raised. The three lines: status cycle, sample status cycle, and initial selection are ANDed to turn on trigger 7 (F4) (FC307), and are also ANDed with 'halt I/O' to turn on trigger 7A (G4).

The turn on line to trigger 7 also signals local storage to fetch UCW 0 for the addressed I/O device (FC307). The trigger 7A sequence waits for the completion of the UCW 0 fetch, then turns on the main channel clock to (FC309): set bit 5 in UCW 0 (in the control register), generate parity for byte 0, and at time T2, store UCW 0 back into local storage. When the storing of UCW 0 is completed, trigger 7A is turned off.

Meanwhile, trigger 7 attempts to form a two-byte CSW (bytes 4 and 5) in the normal manner (see Figure IOP 41). However, the 'halt I/O and MSC busy' line is active and blocks the turn on of the status cycle trigger (Figure IOP 41, E1). Without the status cycle trigger, no main storage cycle can be performed and status bytes are not stored. 'Halt I/O and MSC busy' also causes CPU to be released with condition code 10 (Figure IOP 41, A5). When CPU recognizes the release, it drops 'halt I/O' and 'CPU select channel' to end the operation.

Halt I/O with MSC I/O Interface in Multiplex Mode

If the MSC I/O interface is in byte mode, 'halt I/O' causes the MSC to attempt to select the addressed I/O device and issue the halt I/O to it. Selection of the I/O device is done in the same manner as for a start I/O instruction. These results are possible from the initial selection sequence:

1. The addressed device can fail to answer or the wrong device can answer. Either condition results in a CPU code 11 release.
2. The addressed device may answer with the 'status in' line (FC803). This causes a trigger 7 CSW assembly (to store the status byte) (FC307) with the halt I/O set in UCW 0 bit 5 by the trigger 7A sequence (FC309).
3. The device may be idle and answer the selection sequence normally. In this case, 'address out' is raised without 'select out' to cause the I/O device to disconnect from the interface. A triggers 7 and 7A sequence is also performed for this case with zeros for device status, and zeros for channel status unless a channel error occurs (FC803).

As in start I/O, main channel activates the multiplex initial select line to MSC (A5) (FC801). 'Multiplex initial select' causes MSC to activate the CPU instruction line (B6). If the MSC is idle, 'multiplex initial select' and CPU instruction activate the set (AND circuit A2) and drop the reset to the MSC selected latch (A7). This sets the MSC selected latch. 'MSC selected' turns on the MSC clock (A9).

For the first clock cycle, the A1 pulse resets the MSC to prepare for the halt I/O device selection sequence. At time A2 the unit address is gated from the main channel IUAR to the MSC UAR (B9). The A3 gate sets the initial selection (B6) and selected busy latches (B9). With 'selected busy' set, the MSC selected line to the MSC unit address OR is degated and the MSC clock is turned off (A9). This completes the first clock cycle.

Address Out and Select Out

When the initial selection latch (B6) is turned on (FC801), the device address is gated from the MSC UAR onto the I/O bus out to the control unit (C9). The reset condition, 'not initial selection' is removed from the initial selection and not address out latch (B6) to allow the off condition of the MSC clock A2 delayed line to set it and turn on the MSC clock again. At A2 time, the parity of the address on the I/O bus out is checked. If parity is even (error), a logout is performed with a channel control check indicated.

If parity is odd, the address out latch is turned on (C8) (FC803) by the A3 gate line. The address out I/O interface line (C9) is raised to signal all control units to examine the address on the I/O bus out. If a control unit recognizes the address, it responds with the 'operational in' line when MSC raises the select out signal on the next clock cycle.

'Address out' also resets the initial selection and not address out latch and removes the reset to the initial selection and address out latch (C6). The reset of 'initial selection and not address out' turns off the MSC clock. When the A2 delayed line falls, the initial selection and address out latch is set and the MSC clock is turned on again (C9). At A3 time, the select out latch is set (D6).

'Select out' resets the initial selection and address out latch to turn off the MSC clock (D6). The select out I/O interface line is raised to the control units. 'Select out' signals the control unit that recognized the address on the I/O bus out, to ''capture'' 'select out' and to raise its 'operational in' or 'status in' line to the MSC.

If the I/O address was not identified by a control unit, 'select out' returns to the MSC as 'select in.' 'Select in,' with 'select out' active, activates the no selection line (FC103) to main channel and CPU is released with condition code 11 (FC113).

It is possible for the control unit to raise either 'status in' or 'operational in' in answer to 'address out' and 'select out' from the MSC. 'Operational in' indicates that the control unit is able to proceed with the initial selection sequence. 'Status in' is accompanied by a status byte that has the CU busy bit on. Control unit (CU) busy indicates that the control unit can not accept a command because it either has an I/O operation still in progress, or status conditions exist in the control unit. If any status conditions exist, they are in the status byte.

Operational In and Address In - Issue Halt I/O

When a control unit recognizes the address on the I/O bus out and captures the select out signal, the control unit raises 'operational in' to the MSC (FC803). 'Operational in' resets the address out latch (C7), and 'address out' to the control unit falls. When the control unit sees 'address out' fall, it places its address on the I/O bus in and raises the 'address in' line to the MSC. 'Address in' resets the select out latch, and 'select out' to the control unit falls (D6).

'Address in' and 'operational in' now turn on the MSC clock for the address compare cycle. When the control unit gates its address into the MSC bus in OR (via the I/O interface bus in), a direct compare between the MSC UAR and the MSC bus in OR is performed. If the addresses do not match or if the bus in OR has bad parity, incorrect selection is signaled and a logout is performed with an interface control check indicated. However, a match of the addresses is signaled by the address match line.

'Address match and A3' would normally turn off the MSC clock to prepare for the command out cycle of the selection sequence. However, halt I/O blocks the turn off of the MSC clock at this time. The 'address match and A3' condition now sets the MSC halt I/O and halt condition latches (F7). 'Halt condition' activates the halt condition line, to raise the 'address out' line on the MSC I/O interface (C8). 'Address out' without 'select out' is interpreted as a halt I/O command by the control unit. The control unit responds to halt I/O by dropping all of its "in" lines to MSC. The fall of 'operational in' allows the MSC clock to be turned off (E6).

Meanwhile, when the MSC halt I/O latch was set, the 'device halted' line (F8) became active to set the status cycle request latch (F3). 'Status cycle request' becomes active to main channel and also causes an MSC priority request to main channel (F4). When MSC priority response and response delayed become active, 'sample status cycle' and 'initial selection to main channel' are also raised to main channel (F3-G3). The three lines: status cycle, sample status cycle, and initial selection are ANDed to turn on trigger 7 (F4), and are also ANDed with halt I/O to turn on trigger 7A (G4).

The 'turn on' line to trigger 7 also causes local storage to read out UCW 0 for the addressed I/O device (FC307). The trigger 7A sequence waits for the completion of the UCW 0 fetch, then turns on the main channel clock to set bit 5 in UCW 0 (FC309) (halt I/O bit), generate parity for byte 0, and at time T2 store UCW 0 back into local storage. When UCW 0 is stored, trigger 7A is turned off. This sequence turns on the halt I/O bit in UCW 0 in case the I/O device tries to request a data cycle. If the I/O device requests a data cycle, the halt I/O bit causes the MSC to issue a 'stop command' to the device.

Meanwhile, trigger 7 forms a two-byte CSW (bytes 4 and 5). See Figure IOP 41. However, the device halted line (generated by 'MSC priority response' and 'MSC halt I/O') blocks the gating of byte 4 (device status). Therefore, byte 4 of the CSW contains 0s, and byte 5 contains any channel status (usually 0s also) (FC307). The CPU is released with condition code 01. Any ending status the device may have is presented later as secondary status and is handled by the device service request and trigger 9 sequences.

Status In - Assemble CSW

If the control unit returns 'status in' (instead of 'operational in') in response to 'address out' and 'select out,' an immediate status cycle request is made by the MSC (FC803). When 'status in' is

raised by the control unit at this point in the device selection sequence, it is accompanied by a status byte that has the control unit (CU) busy bit on. 'CU busy' indicates that the control unit cannot accept an I/O command because it either has an I/O operation still in progress, or status conditions exist in the control unit. Any outstanding status indications are in the status byte.

When the MSC is granted priority, the trigger 7 and 7A sequences are executed. As in the other halt I/O operations, the trigger 7A sequence turns on the halt I/O bit in UCW 0 (FC309). For this sequence, the halt I/O bit is used to halt the I/O device when it makes its next service request. Because valid control unit status information is now present in the MSC, a two-byte CSW is formed by trigger 7. Byte 4 has the CU busy bit, plus any other outstanding status indications and byte 5 has 0s unless the 2870 develops status information during this sequence. The CPU is released with condition code 01.

'Status in' to the MSC resets the address out latch and sets the status in latch. 'Status in' turns on the MSC clock (FC805). At time A2, the parity of the status byte is checked. If a parity error exists (even), an interface control check bit is set in the channel status byte of the CSW (G7). At A3 time, the status cycle request line is made active to the status cycle request circuit (H6). 'Status cycle request' becomes active to main channel (F3) and causes a main channel priority request (F4). When MSC priority response and response delayed become active, 'sample status cycle' and 'initial selection to main channel' are also raised (F3). These lines cause triggers 7 and 7A to be set in main channel (F4).

The 'turn on' line to trigger 7 causes UCW 0 to be read from local storage (FC307). The trigger 7A sequence waits for the completion of the UCW 0 fetch, then turns on the main channel clock. During this clock cycle: bit 5 is set in UCW 0, parity is generated for byte 0, and at time T2, UCW 0 is stored back into local storage. After UCW 0 is stored, trigger 7A is turned off and trigger 7 continues. The halt I/O bit just set in bit 5 will cause the addressed I/O device to receive a stop command ('command out' in response to 'service in') on the next device service request it makes. This causes the I/O device to be halted even though the control unit rejected the device selection sequence (by raising 'status in').

Meanwhile, the trigger 7 sequence begins to form a two-byte CSW (see Figure IOP 41). Because the MSC has a valid byte of status information, the MSC bus in OR is gated into byte 4 of the data register (Figure IOP 41, 3B). Marks 4 and 5 (FC307) are forced to allow the two bytes of status information to be gated into bytes 4 and 5 of the CSW (Figure IOP 41, 3C). The status cycle trigger is set to cause a request to BCU (FC551) for a main storage cycle with the CSW address (64) forced (Figure IOP 41, 3F) (FC553). Bytes 4 and 5 of the data register are gated into the control register (Figure IOP 41, 7B). The main channel now waits for BCU to grant priority for the main storage cycle. After bytes 4 and 5 have been stored, the main channel clock is turned off and CPU is released with condition code 01 (Figure IOP 41, 7C).

MULTIPLEX SUBCHANNEL TEST I/O

- CPU sends 'select' and 'test I/O' with a unit address for a device.
- If an interrupt is pending for the addressed device, the trigger 11 sequence is performed to store UCW 2 (CSW) into main storage; CPU is released with condition code 01.
- If no interrupt is pending for the device, UCW 0 is read out and examined for busy or idle subchannel.
- Subchannel busy causes UCW 2 to be read out and examined for status stacked in the control unit.
- If status is stacked in the control unit, a device selection sequence is performed and 'test I/O' is issued to relieve the control unit of the stacked status; CPU is released with condition code 01.
- 'Subchannel busy' and 'status not stacked' cause CPU to be released with condition code 10.
- 'Subchannel idle' causes a device selection sequence to be performed (as in start I/O) with a test I/O command (0s) issued to the device.
- A test I/O command causes the device to return a status byte; CPU is released with condition code 00 if the status is zero, or condition code 01 if status is non-zero.
- If the MSC is in burst mode, CPU is released with condition code 10.
- Any error in the device selection causes CPU to be released with condition code 11.
- COD-7, -8, -10.

All references are to Figure IOP 2 in the 2870 FE Diagrams manual (Form SY27-2301), unless otherwise specified.

CPU initiates a test I/O instruction by raising the test I/O line to the channels (A2), placing an eight-bit unit address on the unit address bus out, and signaling the 2870 with the select channel line (A1). This causes a main channel priority request to the priority circuits (A4) (FC101). When priority is granted, 'main channel response' and 'response delayed' become active (A2).

'Main channel response' and 'response delayed' turn on the clock (C4), gate the unit address from the unit address bus out into the initial unit address register (D4), and set the test I/O latch (FC121) (B2). At this time, the address in the initial unit address register is sent to the unit address OR and compared with the contents of the interrupt queue register (if an interrupt is pending). An address match condition (not PCI), indicates that a CSW is already formed for the device and it is stored in UCW 2. If the addresses do not match, three conditions are possible: the subchannel and device are busy performing an I/O operation, the subchannel is busy because status is stacked in the control unit or device, or the subchannel is idle and the device has either zero or non-zero status.

Test I/O to a Subchannel with a Pending Interrupt

- COD-7.

An address match between the interrupt queue register and the address supplied with the test I/O (FC121), indicates that a CSW has already been formed for this device and is stored in UCW 2. The lines 'address match and interrupt' and 'test I/O' are ANDed to fetch UCW 2 to the control register (C4). When the local storage cycle for UCW 2 is over, the main channel clock is turned off (A4) and trigger 11 is turned on (B4) (FC351).

Trigger 11 fetches UCW 0 into the data register (Figure IOP 42, 4B). At time T6, byte 0 of UCW 0 is reset to remove subchannel busy indications (Figure IOP 42, 4D), and UCW 0 is stored back into local storage.

While UCW 0 is being altered, UCW 2 is stored back into local storage (Figure IOP 42, 4A), and the status cycle trigger is turned on to cause a main storage cycle request (Figure IOP 42, 2D). The CSW address (64) (FC553) is forced into the SAB register, and the CSW is sent to main storage when BCU response is received. After the main storage cycle is over, CPU is released with condition code 01 (FC351, Figure IOP 42, 4E).

Test I/O to a Busy Subchannel

- COD-8

If the address in the interrupt register and the unit address received with the 'test I/O' do not match (FC121), UCW 0 is read out. The operation code (bits 6 and 7) is examined for a bit in either position. A bit in either position indicates that the subchannel is busy. The subchannel can be busy either because a previous I/O operation is still in progress, or because the 2870 has stacked status in the device. If status has been stacked, UCW 2 will have bit 7 on. Therefore, subchannel busy causes the refetch 2 sequence to be performed.

The refetch 2 sequence (FC605) reads out UCW 2 from local storage to the control register (Figure IOP 44, 4D). Bit 7 of UCW 2 is examined to tell whether status information is stacked in the device. Bit 7 off, means that the subchannel is still busy with some previous I/O operation and causes CPU to be released with condition code 10 (Figure IOP 44, 4E).

"Bit 7 on" means that the device presented status to the 2870 some time in the past, and the 2870 stacked the status in the device.

To relieve the I/O device of its status, the multiplex initial select latch is turned on (F2) to begin the MSC initial selection sequence (FC801). The ending trigger (F2, D2) is now set to free main channel for other operations (FC605).

The addressed I/O device is selected just as in start I/O. However, 'test I/O' blocks the gating of any I/O command to the I/O bus out (FC805) during the 'command out' cycle, and the device receives an I/O command of all zeros (+P bit). The all zero command is interpreted as a test I/O command by the device and causes it to immediately raise 'status in' and place the stacked status on the I/O bus in. In this case, the status byte is not zero (FC805), and the MSC makes a status cycle request to main channel.

Because this is a test I/O operation to a device with stacked status, a CSW must be formed and stored in main storage. 'Test I/O stack status' is active to the MSC (turned on by bit 7 in UCW 2), and blocks the 'initial selection to main channel' line. Therefore, when 'main channel response' and 'response delayed' become active, 'status cycle,' 'sample status cycle,' and 'not initial selection to main channel' are ANDed to turn on trigger 9.

Device Selection Error: If the I/O device fails to answer the initial selection sequence ('select in'

returns for 'select out') (FC803), or if the wrong I/O device answers (address mismatch); CPU is released with condition code 11 (error) (FC113). Code 11 indicates to the CPU that the addressed I/O device is unavailable.

Trigger 9

- COD-8.

All references in this section are to Figure IOP 43 unless otherwise specified. Trigger 9 now begins to form a CSW. UCW 0 is fetched into both the data and control registers (FC311), to make the CSW formation easier. The op code, data check, and PCI bits (6, 7, 36, 44) are gated into buffer latches to save them (B3). The channel status bits of UCW 0 are moved from the data register into their correct CSW positions in a set of special status latches as follows: Bit 36 to 40 (PCI), Bit 4 to 41 (IL), Bit 41 to 45 (ctrl chk) and bits 46 and 47 are reset (B3). If the data address program check bit (40) is on, it is reset and the program check bit (42) is set in the control register (E1). A non-zero count in UCW 0 turns on bit 41 of the control register unless the SLI flag is on (F2). Because this is a CSW formed for test I/O to a subchannel with status stacked, the op code (bits 6 and 7) is reset to free the subchannel, and UCW 0 is stored back into local storage (A5). The special status latches are used to hold byte 5 of the CSW until the trigger 10 sequence is ready for it.

The adder holds the residual count field of UCW 0 for the CSW. During trigger 9 the adder is loaded with bytes 5-7 of UCW 0 (B2) and latched (B5). During the trigger 10 sequence, the adder contents are used to supply the CSW residual count unless the prefetch bit was on in UCW 0. If the prefetch bit was on (C1), UCW 0 is still in the data register during trigger 10 and the UCW 0 count field is taken directly from the data register (C11).

If the op code field of UCW 0 indicates a read or read backward, the count field is not zero, and the byte count is not equal to the DAB, the data sequence latch is set (E2) (FC311). 'Data sequence' indicates that an input operation was terminated by the device and UCW 1 still has data to be stored in main storage. UCW 1 is fetched into the data register and the DAB and byte count are gated from the control register to their respective registers (B7). To prevent another data storage cycle, the byte count field of the control register is now reset (C7). A main storage request to BCU is made by setting the data cycle latch (C7). UCW 1 is stored back into local storage. When 'BCU response' rises, the data register contents are sent to main storage with the marks encoded from the byte count and DAB registers. Also at this time, the adder is latched to hold bytes 5-7 of UCW 0 (byte 5 is channel status and bytes 6 and 7 are the residual count) (B7). When the main storage cycle is completed, 'control register full' is turned off (FC313). UCW 2 is fetched, and trigger 10 is set (D7).

Trigger 10

- COD-8.

All figure references in this section are to IOP 43 unless otherwise specified.

Trigger 10 completes the CSW formation and stores the CSW in main storage (FC315). The turn-on of trigger 10 turns off trigger 9 and resets the main channel clock by turning it off (E7). The completion of the local storage cycle (UCW 2 fetch) turns on the main channel clock for the trigger 10 sequence (A9).

The command address field (bytes 1-3) and count field (bytes 6 and 7) can be formed in two ways. Either the previous operation was a write which had prefetched a CCW or it was a read, write, or read backward. The operations differ in the way in which bytes 1-3 and 6, 7 of the CSW are formed in the control register.

For a write operation with a prefetched CCW, UCW 0 is still in the data register and UCW 2 is in the control register. Prefetch indicates that the new CCW has not been used and the information in UCW 0 concerns the old CCW. Therefore, the CSW formed must use the residual command address field of UCW 2 for its command address (one higher than the last CCW executed). The address field correction is performed by releasing the latch line to the adder (B9), and allowing bytes 5-7 of UCW 2 (gated into the adder by the turn-on of trigger 10) to appear at the adder output. The output of the adder is now transferred to bytes 1-3 of the control register (B11). The residual count is transferred from the data register (UCW 0) to the control register (C11) to complete the special handling for write prefetch.

Read, read backward, and write use the same method to form bytes 1-3, 6, and 7 of the CSW. Bytes 1-3 of UCW 2 are not changed. Bytes 6 and 7 are loaded from the adder. During trigger 9, bytes 5-7 of UCW 0 are placed in the adder (FC311) (B3) and latched up (B7). When the main channel clock is turned on for trigger 10, the adder contents (residual count) are transferred to bytes 5-7 of the control register (B1). This path is used because it is possible for a data storage cycle to have occurred (for read or read backward) during trigger 9. If a data cycle had occurred, UCW 0 would not

be in the data register during the trigger 10 sequence.

Byte 4 of the CSW is loaded by gating the MSC bus in OR to byte 4 of the data register (C11), and from the data register to byte 4 of the control register (E12). 'Service out' is raised on the MSC I/O interface to disconnect the control unit and device (C11). Byte 5 of the CSW is filled by gating the special status latches, loaded during trigger 9, into byte 5 of the control register (E11). It is possible that a control (41), program (42), protection (43), or data (44) check occurred if a data storage sequence was performed. If the main channel check latches contain any of these errors, they are ORed into byte 5 of the control register. Because this is a test I/O stack status operation (FC317), the stack status bit (7) is reset (A15), the CSW address (64) (FC553) is forced into the SAB register (A14), and a main storage request is made to BCU (B14). When BCU response rises, the CSW is transferred to main storage. After the main storage cycle is over, CPU is released with condition code 01 and the ending latch is set (A15) (FC317). Release causes CPU to drop 'test I/O' and 'select channel' to end the operation. Ending resets main channel to free it for other operations.

Test I/O to an Idle Subchannel

- COD-10.

All references are to Figure IOP 2 in the diagram manual, unless otherwise specified. If the address in the interrupt queue register and the unit address received with 'test I/O' do not match, UCW 0 is read out (FC121). The operation code (bits 6 and 7) is examined for a bit in either position. If bits 6 and 7 are off, the subchannel is not busy; UCW 0 is stored in local storage. To select the idle device and issue the test I/O command to it, the multiplex initial select latch is set (F2). The ending latch is turned on to free main channel for other operations (F2, D2).

The addressed I/O device is now selected just as in start I/O. However, 'test I/O' blocks the gating of an I/O command to the I/O bus out during the 'command out' cycle. The device receives an I/O command of all zeros (+P bit), which is interpreted as a test I/O command by the device. A test I/O command causes the I/O device to immediately raise 'status in' and place a status byte on the I/O bus in. The status byte is examined.

If the status byte contains all zeros (FC805), 'multiplex accept' is sent to main channel. Multiplex accept causes main channel to reset the initial selection latch and release CPU with condition code 00. When the CPU receives release it drops 'test I/O' and 'select channel' to end the operation.

A non-zero status byte causes MSC to make a status cycle request to main channel (FC805). When main channel priority is granted, 'MSC response' and 'response delayed' cause 'status cycle,' 'sample status cycle,' and 'initial selection' to become active to main channel. These lines are ANDed to turn on trigger 7 and fetch UCW 0 from local storage (FC307).

Trigger 7 begins to form a CSW (bytes 0-7). The byte of status information is gated from the MSC bus in OR into byte 4 of the data register (Figure IOP 41, 3B). 'Test I/O' blocks the normal forcing of marks 4 and 5 (Figure IOP 41, C1), to allow all eight marks to be sent to CPU with the CSW. The status cycle trigger is turned on to raise 'storage request' to BCU, and the CSW address (64) is forced into the SAB register (FC553) (Figure IOP 41, E3). To disconnect the I/O control unit and device from the I/O interface, 'service out' is raised (Figure IOP 41, A7) (FC805). The control register is reset to be sure that the CSW only contains information in bytes 4 and 5 (bytes 0-3 and 6-7 are 0). After the control register is cleared, byte 4 (the device status) and byte 5 (any channel status indications) are gated into the control register (Figure IOP 41, B7) (FC307).

When BCU response becomes active, the control register contents are transferred to the CSW (location 64 in main storage). When the main storage cycle is completed, CPU is released with condition code 01 and the main channel clock is turned off (Figure IOP 41, D7). The release signal causes CPU to drop 'test I/O' and 'select channel' to end the operation.

Device Selection Error: If the I/O device fails to answer the initial selection (FC103) ('select in' returned for 'select out'), or if the wrong I/O device answers (address mismatch), CPU is released with condition code 11 (error) (FC113). Code 11 indicates to the CPU that the addressed I/O device is unavailable.

Test I/O with the MSC in Burst Mode

When test I/O is issued to a multiplex device, it is possible for the MSC I/O interface to be in burst mode (FC801). When the multiplex initial select latch is set an attempt is made to set the MSC selected latch. If the MSC selected latch is blocked by a burst mode operation, the MSC busy logic begins to time out. If 'operational in' remains active on the MSC I/O interface for more than 64 usec, the busy logic times out and sets the interface busy latch.

'Interface busy' indicates that the MSC I/O interface is in burst mode. CPU is released with condition code 10 (FC113). The release signal causes CPU to drop 'test I/O' and 'select channel' to end the operation.

SELECTOR SUBCHANNEL START I/O

- CPU initiates execution of an I/O operation by raising 'start I/O' and 'channel select' to the addressed channel.
- Channel fetches the channel address word (CAW) from main storage location 72.
- CAW provides the storage protect key and address of the first channel command word (CCW).
- UCW 2 is formed from the CAW.
- Main channel fetches the CCW from main storage.
- The addressed selector subchannel (SSC) starts selection of the device after the CAW is fetched (in parallel with the CCW fetch).
- UCW 0 is formed from the CCW.
- After the CCW is fetched and UCW 0 is formed, main channel raises the CCW gate to the addressed SSC.
- CCW gate causes the SSC to gate the command, flags, byte count, and end count into the SSC registers.
- SSC completes selection of the I/O device.
- When the device starts execution of the operation, the CPU is released.
- COD-16.

All references are to Figure IOP 20 in the diagram manual, unless otherwise specified.

A start I/O instruction to an available subchannel causes selection of an addressed device and, when possible, the initiation of a channel command. The channel commands associated with start I/O are: read, read backward, write, sense, and control. For SSC operations, these commands are grouped:

1. Read
   a. Read
   b. Sense
   c. Read backward
2. Write
   a. Write
   b. Control

Acceptance or rejection of the initial command causes the channel to release the CPU with the proper condition code.

SSC initial selection begins when start I/O is issued to the 2870. SSC start I/O operations are performed in both the subchannel and the main channel (Figure 3-17). The main channel fetches the CAW and CCW from main storage and forms UCW 0 and 2, respectively (FC101). After the CAW arrives, the SSC begins selection of the addressed device in parallel with the main channel CCW fetch. When the CCW arrives, the SSC completes selection of the device, and the CPU is released with the proper condition code (0, if the command is accepted).

Start I/O to Channel (Fetch CAW)

- CPU sends 'select channel,' 'start I/O,' and a unit address.
- Main channel priority is requested.
- CAW latch is set and the unit address is decoded.
- CCW request latch turns on and address 72 is forced into the SAB register (to fetch the CAW).
- BCU advance generates 'CCW advance' and 'CCW late advance' to gate the CAW into the channel.
- Storage cycle over latch is set and test is made for storage cycle errors.
- 'Storage cycle over and no errors' sets the CCW required latch.
- Another subchannel may break in to perform some data or status sequence between the CAW and CCW fetches.
- COD-16.

The CPU raises the start I/O multiplex line to the channel, places an eight-bit unit address on the UABO, and activates the CPU select channel line to the 2870 (A1). 'CPU start I/O' and 'select channel' are ANDed with 'not initial select,' 'not release,' and 'not main channel response' to activate a main channel priority request (FC101). When priority is granted, 'main channel response' and 'response delayed' become active.

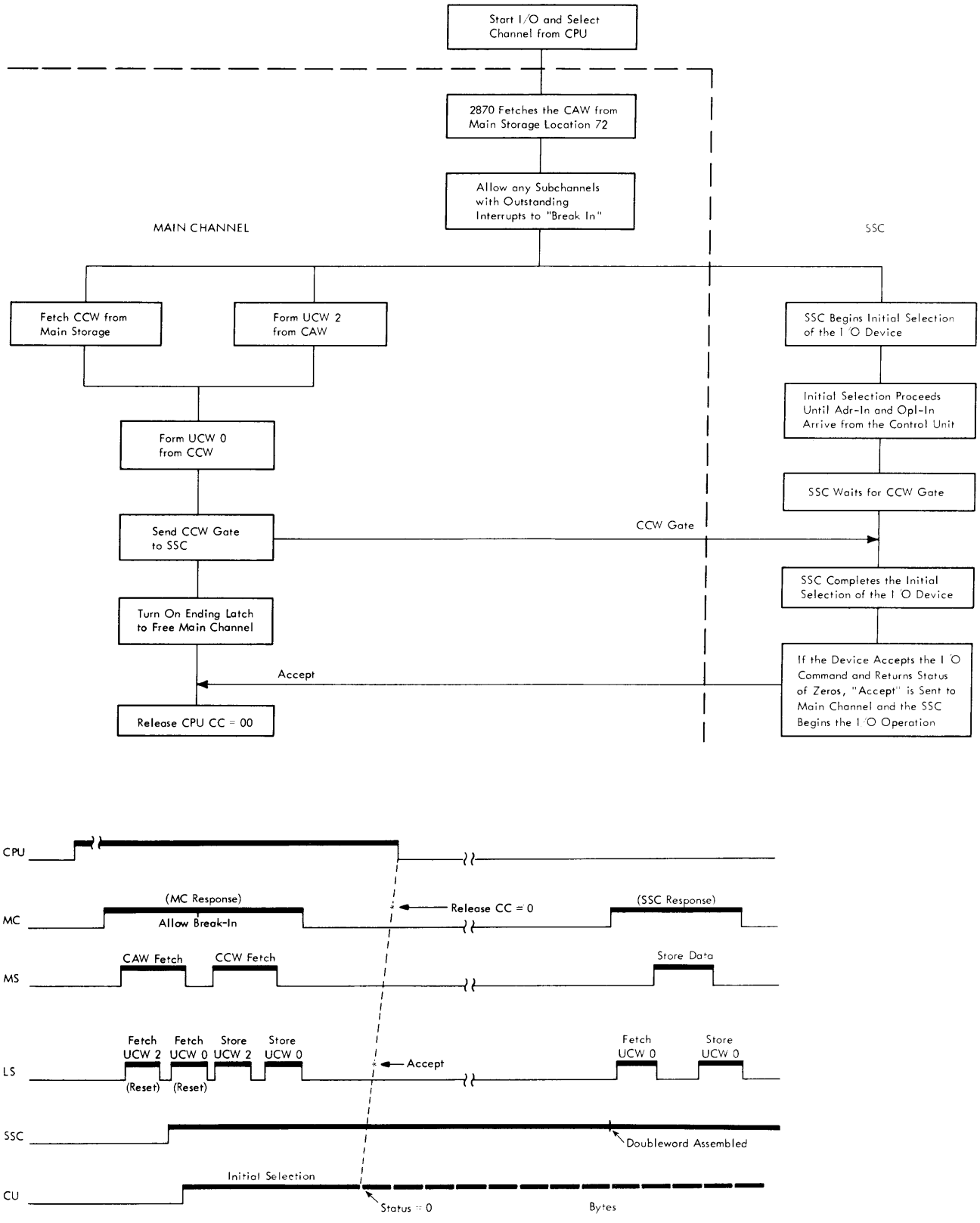


Figure 3-17. Selector Subchannel Start I/O

Main channel response causes the unit address to be gated from the UABO through the IUAR to the UAOR (B4). The output of the UAOR is sent to a decode circuit that determines the addressed subchannel (MSC or SSC 1-4). Main channel response and response delayed are ANDed with 'start I/O' and 'CPU select channel' to set the CAW latch. When the CAW latch is on and the start I/O latch is off, the main channel clock is turned on (C4).

Assume that the subchannel address has bits 0 and 1 on (SSC decoded). Bits 2 and 3 must be examined to determine whether the addressed SSC is busy, not busy, or not installed. Each SSC provides to the address decoder a line to indicate when the SSC is busy, and an entry block is wired to indicate that an SSC is installed.

At main channel clock T0 time, 'CAW' and 'SSC decoded' (C2) condition three AND circuits to test the result of the unit address decoding. If the addressed SSC is valid and busy, the CPU is released with condition code 10 (C2). If the unit address is invalid (not installed), the CPU is released with condition code 11 (C2).

'SSC valid and not busy' (the operation can proceed) sets the CCW request latch (D2), causes UCW 2 to be read from local storage (D2), forces the address of the CAW (72) into the storage address bus register (D4) (FC551), and turns on a latch (C3) to gate 'BCU response.' The turn-on of CCW request indicates that a storage request must be made to the BCU to fetch the CAW; address 72 is forced into the SAB register. The main channel clock is turned off because the storage to channel operation is now dependent on BCU timing.

'CCW request' and 'not CCW accept' (E3) cause a storage request to be sent to the BCU (D4). 'Storage request' indicates to the BCU that the channel is requesting priority for a storage cycle. When 'BCU response' rises (BCU has granted priority to the channel), the SAB register contents are sent to the BCU and the address valid latch is set (C4). 'Address valid' indicates to the BCU that the SAB lines have a valid storage address. The BCU now sends 'BCU data request.'

Because this is a CAW fetch, data is not placed on the SDBI at this time. 'Accept' (pulse) arrives from the BCU, and indicates that the CAW fetch is started and that the next advance pulse from the BCU is part of the CAW fetch. 'Accept' and 'BCU data request' are ANDed to turn on the CCW accept latch (E3). With 'CCW accept' on, the storage cycle request is ended (D4). The channel now waits for advance to arrive from the BCU. Advance is a pulse from the BCU to the channel, which leads the data from the BCU by about 200 ns.

'Advance' arrives from the BCU and fires a 400 ns singleshot, which generates the CCW advance pulse (E3). 'CCW advance' indicates that the data on SDBO is valid and should be gated into the channel data register. Therefore, 'CCW advance' resets the CCW accept latch (E3), gates the SDBO into the data register, and fires a 500 ns singleshot, which then fires another singleshot (E3). 'CCW late advance' is generated when the 500 ns singleshot expires and is active for about 100 ns (E4). The second singleshot just referred to is adjusted to the requirements of the CPU the 2870 is attached to. For exact timings, see the 2870 FE Maintenance Manual, (Form SY27-2302).

'CCW late advance' sets the 'CCW in D register' latch (A5). When CCW late advance falls, a 350 ns singleshot (A7) fires to gate the CAW from the data register to the control register (A8) (FC557). The gate line which transfers the CAW into the data register also fires a singleshot to turn on the storage cycle over latch (B6).

'Storage cycle over' indicates that the CAW fetch is complete (FC105). A test for errors is now made. If an error occurred during the CAW fetch, the storage cycle check latch is turned on (B7). 'Storage cycle over' and 'storage cycle check' activate the 'storage cycle over and check' line (B7) to set the selection sequence check latch (C7). 'Selection sequence check' causes the CPU to be released with condition code 01 (C8) (FC601), and a CSW to be stored with the error condition indicated.

'Storage cycle over and no check' (B7) is ANDed with 'CAW trigger gated and not outstanding request' to set the CCW required latch (FC105) (C7). If an outstanding request condition exists, CCW required is not immediately set and the subchannel that is requesting service is allowed to break in and use the main channel circuits (Figure 3-6).

Outstanding Request (Allow Break-In) (FC105)

- One subchannel has a priority request active.
- 'Priority request' turns on the outstanding request latch.
- Ending trigger is turned on to reset most of the main channel triggers.
- Store the CAW in UCW 2.
- CCW required latch is turned on and CAW latch is turned off.

- Main channel priority request remains active.
- When all subchannels requesting priority have completed their operations, the start I/O operation continues.
- COD-16.

The ending trigger establishes a point of return to the start I/O routine, saves the CAW in UCW 2, and clears the main channel for the next operation.

To establish the point of return to the start I/O routine, 'ending' and 'CAW trigger gated' turn on the CCW required latch which turns off the CAW latch. The CAW is stored in UCW 2 (FC155).

After the local storage cycle is completed, the main channel busy latch is reset. The reset of main channel busy causes the main channel priority response latch to be reset. Main channel priority request now becomes active because 'start I/O' and 'select channel' are still active from the CPU (A1).

The subchannel with the highest priority now gains control of the main channel and performs its operation. When the operation is completed, priority is granted to the next lower subchannel. When all outstanding requests have been serviced, the main channel regains priority and the start I/O operation continues.

CAW in Channel

- CAW trigger is turned off.
- UCW 2 is fetched from local storage if break-in occurred.
- UCW 0 is reset.
- SSC begins the initial selection sequence.
- UCW 2 is formed from the CAW.
- CCW is fetched from main storage.
- COD-16.

The turn-on of 'CCW required' (FC105) conditions an AND circuit to reset the CAW trigger (C8). CCW required is ANDed with 'not outstanding request' to test whether a break-in occurred. If a break-in occurred, word 2 (CAW) is in local storage and the control register is empty. Therefore, 'not word 2 fetched' and 'not control register full' cause UCW 2 to be fetched into the control register (D8). 'Control register full' and 'not CAW trigger gated,' activate the CCW fetch line. 'Control register full' also causes a UCW 0 fetch with 'block' on. Block causes a reset of the contents of UCW 0.

'CCW fetch' and UCW 2 in the control register indicate that the CAW is in the channel and a CCW fetch can be performed. 'CCW fetch' and 'word 2 fetched' turn on the main channel clock and set the CCW request latch (D2). 'CCW request' on initates a main storage fetch, using the command address in the CAW.

An SSC select latch is set (E7) and 'SSC select' and 'start I/O' are sent to the addressed SSC. Main channel also begins to form UCW 2 from the CAW. Three operations are now being performed by the 2870: a CCW fetch from main storage, the formation of UCW 2 in the control register, and SSC begins the I/O interface initial selection sequence.

SSC Begins Initial Selection

'SSC select' and 'start I/O' cause the SSC to begin the start I/O initial selection sequence on the SSC I/O interface (FC901). This initial selection sequence proceeds, in parallel with the CCW fetch, until the control unit has answered SSC's address out and select out with address in and operational in (FC903). To continue the selection sequence, the SSC now needs the I/O command. Therefore, the SSC must wait if the CCW operations are not complete. The main channel indicates the completion of the CCW operations by raising the 'CCW gate' (C11) to the addressed SSC (FC903). When SSC receives CCW gate, the command, flags, byte count, and end count are gated into the SSC and the initial selection sequence continues.

Form UCW 2

The 2870 uses the CAW to form UCW 2. UCW 2 contains the storage protect key, the address of the command in the channel (residual command address field, bytes 5-7), and the address of the next command (command address field, bytes 1-3). The address of the next command is eight bytes higher than the residual command address. To derive the next command address from the residual command address, the residual command address is placed in the adder and is incremented by 8 (FC105).

For start I/O operations, the address in the CAW is the residual command address. Therefore, on start I/O operations nothing is placed in the residual command address field and the resulting UCW 2 only contains the address and key of the next command (bytes 0-3).

When the CAW is gated into the control register, the command address is in bytes 1-3. 'CCW fetch' gates bytes 1-3 to the adder (E8), with 'increment.'

The result is the CCW address +8. The adder is latched and the output of the adder is gated into bytes 1-3 of the control register (E8). UCW 2 is stored (F8). After the local storage cycle is completed, the main channel clock is turned off (F8).

CCW Fetch

A CCW fetch is performed in the same manner as a CAW fetch, except that the command address from the CAW is placed in the SAB register (FC551) (D7). CCW request (D2) activates 'CCW storage cycle request,' which causes a storage request to be sent to the BCU (D4).

When BCU response rises, the address in the SAB register is sent to the BCU and 'address valid' is raised to the BCU (C4). 'Accept' arrives from the BCU to indicate that the next advance pulse from the BCU can be used to gate the CCW into the main channel. 'Accept' turns on the CCW except latch (E3), which drops the storage request to the BCU (D2). 'Advance' (E1) arrives from the BCU and generates CCW advance (E3). 'CCW advance' resets the CCW accept latch (E3) and gates the CCW (on the SDBO) into the data register (A8).

'CCW advance' also fires a singleshot to generate the CCW late advance pulse (E4). 'CCW late advance' sets the 'CCW in D register' latch (A5) (FC551); and when 'CCW late advance' expires, a 350 ns singleshot gates the CCW into the control register. As the CCW is gated into the control register, a 150 ns singleshot fires and sets the storage cycle over latch (B6).

If an error occurred during the CCW fetch, the storage cycle check latch (B6) is on. 'Storage cycle over and check' on a CCW fetch sets the selection sequence check latch (FC107) (C6). If no errors occurred, 'storage cycle over and no check' and 'CCW fetch' set the 'CCW in channel' latch (A11) to indicate that the CCW is in the control register. 'CCW in channel' turns off the CCW required latch (C6) to end the CCW fetch.

CCW in Channel (Complete Main Channel Operation)

- UCW 0 is formed.
- CCW gate is sent to the SSC.
- DAB, end count, flags, and command are sent to the SSC.
- Ending latch is turned on to reset the main channel.
- SSC completes the initial selection.
- COD-16.

With the CCW in the control register, the main channel forms UCW 0, sends 'CCW gate' to the SSC, and turns on the ending trigger to release the main channel from the start I/O operation. 'CCW gate' causes the SSC to complete the I/O interface selection sequence.

When the SSC completes the start I/O initial selection and is able to perform the command, 'accept' is sent to the main channel. Accept causes the 2870 to release the CPU with condition code 00. If the I/O interface selection is not made (select in is returned for select out), the SSC sends 'no selection' to the main channel. 'No selection' causes the 2870 to release the CPU with condition code 11.

For 'accept' or 'no selection,' the SSC does not need to establish priority in the main channel. However, if the control unit returns status or if the subchannel detects an error, the SSC brings up 'CSW cycle' and 'priority request.' A CSW is formed in the main channel and is stored in main storage location 64; the CPU is released with condition code 01.

Form UCW 0

UCW 0 is a modified CCW. As the CCW is transferred from the data register to the control register, the command (bits 0-7) is encoded into a two-bit code and is placed in control register bits 6 and 7. These bits are:

Bit 6	Bit 7	Operation
0	0	Idle
0	1	Write or control
1	0	Read or sense
1	1	Read backward

Bits 0-3 of the control register also retain the storage protect key (obtained from the CAW).

For SSC operations, the count and data address fields must also be modified. The DAB (data address field bits 29-31) must be complemented if a read backward operation is to be performed. After the DAB (bits 29-31) is corrected (if necessary), the count and DAB are added to provide a major count (held in UCW 0) and an end count (held in the SSC). Also, if the 2870 is attached to a channel control unit, the address prefix bits are placed in bits 37 and 38.

'CCW in channel' and 'not CCW required gated' turn on the main channel clock for the UCW 0 formation cycle (FC107). 'SSC decoded' is ANDed with 'CCW in channel' to identify the sequence as UCW 0

for an SSC (SSC CCW in channel). 'Gate DAB to DAB BC' is activated to allow the DAB to be gated into the DAB register (A10). The DAB is gated to the DAB register in true form for a read or write operation (B10) and is gated in complement form for a read backward operation (B10). 'SSC CCW in channel' and 'read backward' cause the DAB to be gated into the control register DAB field (bits 29-31) (B10).

The correct DAB (true or complement) is added to the CCW count. Bits 29-31 and bytes 6 and 7 of the control register are added (B10). The result of the addition is returned to bytes 6 and 7 of the control register (C10). If an adder overflow occurs, the overflow bit is placed in bit 47 and bit 46 is turned on to maintain correct parity in byte 5. The count field is then examined.

If the count is between 8 and 16 (FC107) or equal to 16, 'double last word' is sent to the SSC (B11). For a count between 8 and 1, 'last word' is sent to the SSC (C11). Last word or double last word indicates that the operation is short (one or two double words) and the SSC prepares to end or chain to a new CCW (depending on the flags set).

'CCW gate' is sent to the SSC and UCW 0 is stored in local storage. 'CCW gate' causes the SSC to gate the following control information into the SSC registers (FC107):

1. Command byte from the data register into the SSC A register.
2. Count field bits 61-63 (end count) from the control register to the SSC end count backup register.
3. DAB from the DAB register to the SSC byte count backup register.
4. CD, CC, and SLI flags from control register positions 32-34 to the SSC flag A register.
5. Double last word or last word.

The ending trigger (D11) is turned on. The ending trigger resets the main channel to free it for any other operations which may be pending. The SSC now completes the initial selection of the device.

The CPU is released when selection of the device is completed, and the operation is performed by the SSC and the control unit. The main channel is necessary only for fetching data (write operation) or storing data (read/read backward operation), or for CSW operations.

Selector Subchannel Initial Selection

- 'SSC select' and 'start I/O' set 'SSC selected' and gate the unit address into the SSC UAR.
- The unit address is placed on bus out, and 'address out' followed by 'select out' are raised to the control unit.
- When a control unit recognizes the address, the control unit raises 'operational in' followed by 'address in,' and the control unit address is placed on bus in.
- If the address in the SSC UAR matches the address on bus in, the SSC attempts to set the address match and A3 latch.
- 'Address match and A3' is held reset until the main channel sends 'CCW gate.'
- 'CCW gate' causes the SSC to gate in the CCW command, flags, byte count (DAB), and end count.
- The command is sent to the control unit with the command out tag.
- Control unit decodes the command and returns initial status and the status in tag.
- 'Status equal 0' gates 'accept' to the main channel to release the CPU with condition code 00.
- For a read operation, 'service out' is sent to the control unit when 'accept' is raised. (See COD-17.)
- A write operation initiates the trigger 1 sequence to fetch two double words of data into the SSC A and B registers. (See COD-18.)
- Read or write operations continue under the control of triggers 1-3.
- COD-16.

When the main channel fetches the CAW and no priority requests remain active (break-in sequence), the SSC select signal is raised to the addressed SSC. 'SSC select' and 'start I/O' remove the reset to the SSC selected latch (A14), and 'SSC select' removes the set to the tie break latch. The result is the setting of the SSC selected latch (A14) (FC901).

'SSC selected' turns on the SSC clock (A16), resets the SSC (B16), and gates the four low-order bits (4-7 + P) of the unit address into the SSC UAR. The four low-order bits are combined with the four prewired high-order bits of the UAR to form the unit address byte. A3 gate from the SSC clock

turns on the SSC busy (B16) and initial selection (B13) latches. 'Busy' turns off the SSC clock and blocks any further CPU selects to this SSC until the operation is completed.

Address Out and Select Out

'SSC initial selection' (B13) and 'not operational in' gate the unit address byte to the I/O interface bus out (B16) (FC901). With SSC initial selection on and the SSC clock off, the SSC initial select B latch (B14) is reset, which turns on the SSC clock (B15). At A2 time, the address on bus out is parity-checked (odd) and unit address check (C15) is set if an error occurs. A unit address check causes an I/O disconnect (E14), and a CSW cycle with a channel control check is indicated.

'A3 gate' turns on the address out latch (C14) to send 'address out' to the I/O interface (C16). 'Address out' turns on the SSC initial select B latch, which turns off the SSC clock. All control units examine the address on bus out for a bit-for-bit match condition. An address match condition causes the control unit to prepare for a selection sequence.

'Address out' and 'SSC clock off' set a latch (D14) to turn on the SSC clock (D15). 'SSC initial selection' and 'A3 gate' turn on the select out latch (FC903) (D14) and 'select out' is raised to the I/O interface (D16). 'Select out' also resets the latch (D14), holding the clock on. The addressed control unit captures 'select out' and signals the SSC with 'operational in' (FC903).

If the address is not identified, none of the control units captures 'select out' and 'select out' returns to the SSC as 'select in.' 'Select in' with 'select out' active activates 'no selection' (E16). 'No selection' is sent to the main channel release circuits and the 2870 releases the CPU with condition code 11.

Operational In and Address In

When a control unit recognizes the address on bus out and captures 'select out,' the control unit raises 'operational in' to the SSC (E13) (FC903). Operational in resets the address on bus out (B15) and the address out latch (C13). The fall of 'address out' causes the control unit to place its address on bus in and raise 'address in.'

SSC compares the address on bus in with the contents of its UAR. If the addresses do not match or if bus in has bad parity, an interface control check is indicated and a CSW cycle is performed. 'Address in' and 'operational in' turn on the SSC clock (A18). 'Address match' and A3 gate attempt to turn on the address match and A3 latch (B19); however, if the command loaded latch is not set, (A19) the address match and A3 latch is held reset.

'Command loaded' is not set until the SSC receives 'CCW gate' from the main channel (A17). Therefore, the SSC must wait until the main channel completes the CCW fetch operation.

Command Out

The main channel sends CCW gate to the SSC after UCW 0 is formed from the CCW. 'CCW gate' causes the SSC to gate in the following information:

1. Command byte from the data register to the SSC A register (A20).
2. End count from bits 61-63 of the control register to the SSC end count backup register (A20).
3. DAB from the DAB register to the SSC byte count backup register (A20).
4. CD, CC, and SLI flags from bits 32-34 of the control register to the SSC flag A register (A20).

Two singleshots are also fired (in series) (A17 and A18) to set the command loaded latch (A19).

The turn-on of 'command loaded' removes the reset to the address match and A3 latch (FC903) (B19). 'Address match and A3' is turned on by 'operational in,' 'address in,' and 'address match' (A17 and B17). 'Address match and A3' removes the reset to the address match latch (B17) and turns off the SSC clock (A17 and A19).

'Address match' turns on the SSC clock (B19) and gates the command byte to bus out (C20) (FC907). The A2 pulse checks for a possible bus out parity check (C18). If a bus out parity error occurs, 'command check' is set (C19). The A2 pulse also gates the byte count from the byte count backup register to the byte count latches (C20) to initialize the byte counter for the subsequent read or write operation. 'A3 gate and address match' set the command out latch (D19) and 'command out' is sent to the control unit.

'Command out' causes the control unit to gate in the command and drop 'address in.' With address in down, the address match and A3 latch (B19) is reset, which resets the address match latch (B17). With address match reset, the command is removed from bus out.

Status In

The control unit has decoded the command and determined whether the operation can be performed. A status byte is now placed on bus in and 'status in' is raised to the SSC (FC907). If status equals 0, the operation proceeds.

'Status in' removes the reset from the latch (D18) that activates the 'status in and not I/O disconnect' line (D18). The SSC clock is turned on and

the A2 pulse brings up 'status in check' (E18). If a bus in parity check occurred (on the status byte), 'status in check' is set (E19) and an interface control check is indicated. 'Status not equal 0' (E17) and 'A3 gate' turn on I/O disconnect. A CSW is stored and the CPU is released with condition code 01.

Assume that the status equals 0. 'A3 gate' and 'status equal 0' bring up 'go condition' (E18) (FC907). 'Go condition' sets the accept (E18) and data cycle latches (F17). 'Accept' is sent to the main channel to cause a CPU release with condition code 00. The 2870 now continues the operation with the BCU.

If this is an input (read) operation, 'go condition' turns on the service out latch (G19) and 'service out' is raised to the control unit. The operation now continues under the read/write operation diagram (Figure IOP 23).

Before an output (write) operation can proceed, two double words of data must be buffered in the SSC A and B registers. 'Data cycle' and 'output operation' fire a 200 ns singleshot, which sets the data cycle request latch (F20) (FC905). 'Data cycle request' sets the data cycle response latch (F18). 'Data cycle response' activates the SSC data cycle line, which turns on trigger 1 (Figure IOP 23, A1). Two trigger 1 sequences (FC251) are performed to fetch two double words of data into the SSC A and B data buffers. 'Output operation' and 'A and B register full' activate 'first service out,' which sets the service out latch (G19). 'Service out' is sent to the control unit, and the operation continues under the read/write operation diagram (Figure IOP 23).

SELECTOR SUBCHANNEL READ/SENSE

- Read and sense operations are similar.
- Data or sense bytes are received from the control unit.
- Bytes are assembled into doublewords and stored in main storage.
- Read-skip is similar to a read operation, except that data is not stored in main storage.
- Read backward is similar to a read operation, except that data is stored in main storage in reverse order.
- COD-17.

Sense

As in the MSC, read and sense are similar operations. In both operations, information is transferred from the I/O device to main storage. Sense and read differ only in the contents of the bytes of data transferred under each command. A sense operation transfers bytes that contain the status of the I/O device and any unusual conditions that the device detected in the previous operation. The quantity and meaning of the status information associated with the sense operation depend on the type of device. The status information provided in sense bytes is more detailed than that supplied in the CSW. An explanation of the sense status bytes can be found in the manual for the device.

In read and sense operations, all five flags (CD, CC, SLI, skip, and PCI) are examined. Modifier bits are held in bit positions 0-5 for read and bit positions 0-3 for sense. The 2870 does not examine the bytes transferred and does not recognize any difference between the read and sense operations.

Read

All references in this section are to Figure IOP 23 in the diagram manual.

During a read or sense operation, the SSC accepts bytes of data from the I/O device via the I/O interface bus in and gates them into the SSC A register (FC905). (Figure 3-18.) When a doubleword is

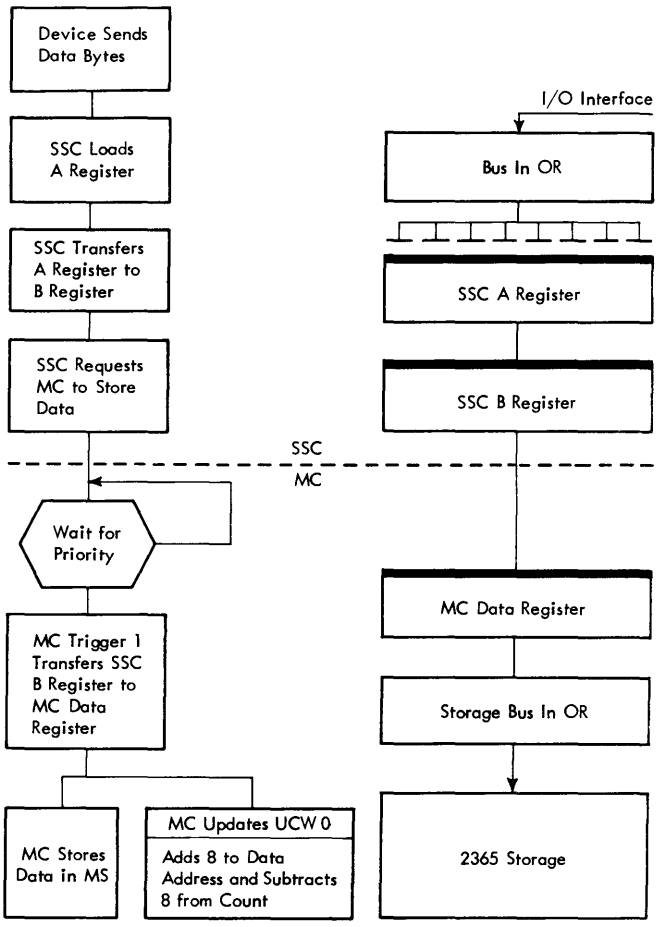


Figure 3-18. Selector Subchannel Read/Sense

assembled (A register full), the completed doubleword is transferred to the SSC B register and main channel priority is requested. When priority is granted, the main channel trigger 1 sequence (FC251) transfers the doubleword to the data register and from the data register to main storage. Data is stored in an ascending order of addresses, starting at the address specified by the CCW. UCW 0 contains the data address and flags necessary to control the storage operation and count field to signal the end of the operation. UCW 0 is updated (data address incremented, and count decremented by 8) during each main storage operation.

During the start I/O sequence, UCW 0 and 2 are formed and the SSC byte count, end count, and flag registers are initialized (FC907). When the initial selection sequence is completed and accept is sent to the main channel, 'service out' is raised as a signal for the control unit to begin the data transfer. Bytes of data (from the I/O control unit) come across the I/O interface and are gated into the SSC A register (in their proper byte locations) by the byte counter. The byte counter steps (+1) for each service in/service out signal exchange. When the byte counter steps from 7 to 0 (FC913), the A register full latch is set. 'A register full' gates the contents of the A register to the B register and turns on 'B register full' (FC915).

'B register full' and 'input operation' (A1) turn on the data cycle request latch (A2). 'Data cycle request' turns on the data cycle response latch (FC915) (A3) and requests priority for the SSC (A3). 'Data cycle request' activates the SSC data cycle line to the main channel (B1). When priority is granted, SSC data cycle, SSC response, and response delayed are ANDed to turn on trigger 1 (B2) and fetch UCW 0 from local storage (FC251). 'Trigger 1' and 'SSC decoded' identify the sequence as SSC trigger 1.

UCW 0 contains the data address, flags, and major count needed to control the main channel. Therefore, when the local storage fetch (UCW 0) is complete, 'control register full' turns on the main channel clock (B3).

With the main channel clock on, the following parallel operations are started:

1. DAB bits are gated to the DAB register.
2. The major count is gated to the adder and decremented by 8.
3. SSC B register contents are gated to the data register.

The CCW DAB (bits 29-31 of the control register) designates the byte location in main storage at which data storage is to start. Each time data is sent to main storage, the DAB is gated from the control register, through the DAB register, to the marks encoder to activate the proper mark lines to main storage. For the first data transfer, the DAB field contains the DAB taken from the CCW. During the main channel sequence for the first data transfer, the DAB is reset to zeros to cause the following sequences to transfer full doublewords. When the operation ends, the DAB field is ignored and the marks encoder is gated by the SSCs byte counter.

Because the SSC transfers data into main storage in doublewords, the count field of UCW 0 is gated to the adder and decremented by 8 (C3). The result is returned to the count field of the control register (F3).

'Trigger 1 SSC' gates the contents of the SSC B register into the data register (C3) (FC251).

'Not read-skip' and 'trigger 1 SSC' (D1) turn on the DCR trigger (E1) and gate the data address field of the control register into the SAB register (D4). 'DCR on' generates a storage request to the BCU (E4) and sets the storage cycle trigger. A normal channel-to-BCU storage sequence is performed and the data register contents are placed on the storage data bus in when 'BCU data request' rises.

The data stored line is activated to the SSC to reset the B register full latch (E6). For a read or sense operation, the data address is incremented by 8 (A7) and is returned to the control register (B7). UCW 0 is stored in local storage and 'control register full' and the MC clock are turned off (C7). If the storage cycle is completed without errors, 'storage cycle over and no check' and 'clock off' turn on the ending trigger (C7) to free the main channel. The main channel now waits for the next operation.

When the A register full latch is turned on again, the operation is repeated. This operation continues until either the main channel count is exhausted or the control unit presents ending status.

The SSC monitors for the end of an operation by checking the last word trigger (set when the main channel detects a count less than 8). 'Last word' indicates that the SSC is assembling the last double word in the A register. With 'last word' on, the SSC compares the end count register and the byte count latches to determine the stopping point. Any bytes sent from the control unit after the SSC has detected 'byte count equal end count,' receive 'command out' (stop command) from the SSC.

A control unit can end the operation at any time by returning 'status in' in response to 'service out.' (See COD-23.) Data remaining in the A register is stored in main storage, the control unit status is gated into the A register, and the SSC initiates a CSW cycle.

Read Backward

A read backward operation is performed in the same manner as a read operation, except that the data is stored in main storage in a descending order of addresses, starting with the highest storage address.

On Figure IOP 23, read backward is performed in the same manner as read, except for the data address update. 'Read backward' causes the data address to be decremented by 8 for each double word of data stored (A7) (FC251). In the SSC, the output of the byte counter is inverted to cause the data bytes to be placed in the SSC A register in reverse order. Because a complement DAB initializes the DAB register and is also used in the count plus DAB operation, 'byte count equal to end count' during last word ends the operation in the same manner as during read.

Read-Skip

A read-skip operation is performed in the same manner as a read operation, except that data is not stored in main storage. When a doubleword of data is assembled in the SSC A register, the A register contents are transferred to the B register and priority is requested. When priority is granted, UCW 0 is fetched and trigger 1 is turned on (Figure IOP 23, B2).

The flags of UCW 0 are inspected as part of the trigger 1 sequence. With the skip flag on, the turn-on of the DCR latch is blocked (Figure IOP 23, D1) (FC251), and the data address is not gated to the SAB register (Figure IOP 23, D4). A storage cycle is not requested.

A test is made for any data checks which might have occurred during the transfer of data from the control unit, through the SSC, to the data register. If there are no data checks, UCW 0 is stored, the ending trigger is turned on, and the data storage operation is terminated.

Each time the A register full latch is turned on, the operation is repeated. This continues until either the CCW count is exhausted, or the control unit presents ending status.

Chain Data Address (Read)

- If the CD flag is on (a 1 in bit position 32), a new CCW is fetched during the last doubleword transfer from the SSC to main channel.
- The new CCW is modified to form a new UCW 0, and the SSC byte count, end count, and flag registers are initialized.
- UCW 0 is stored and the operation continues.
- Trigger 1 sequence handles the data transfer.
- Trigger 2 sequence commences the CCW fetch and forms a new UCW 2.
- Trigger 3 sequence forms UCW 0 and gates the new end count, byte count, and flags to the SSC.
- COD-19

All references in this section apply to Figure IOP 24 in the diagram manual.

After performing the data transfer specified by a CCW, the activity initiated by start I/O can be continued by chaining (fetching a new CCW). Every SSC to main storage data transfer is performed by the trigger 1 sequence. Each time a trigger 1 sequence is performed, the count field of UCW 0 is decremented and examined for last word condition (count less than 8). 'Last word' is turned on to indicate to the SSC that the last double word of data is now being read into the SSC A register.

When the byte count equals the end count with 'last word' on, the count equal 0 latch is set in the SSC to indicate that the SSC has exhausted the present CCW. If the CD flag is on (SSC flag register) for a read operation with count equal 0, the SSC raises the SSC 'new CCW' line to the main channel (FC253).

'New CCW' causes the trigger 1 sequence to fetch UCW 2 and to prepare for a trigger 2 (fetch CCW) sequence. Trigger 2 fetches the CCW, updates UCW 2 (increment command address by 8), and turns on trigger 3. Trigger 3 modifies the CCW to form UCW 0 and initializes the SSC end count, byte count, and flag registers. At the completion of the trigger 3 sequence (FC255), UCW 0 is stored in local storage, and the ending trigger is set to free the main channel. The SSC continues the read operation.

As previously explained under SSC read, after 'SSC data cycle' and 'SSC priority response' become active, trigger 1 is set and UCW 0 is fetched (FC251) (B2). Main channel clock is turned on (B3) and the count is decremented (C3). The contents of the SSC B register are transferred to the main channel data register (B3). 'New CCW' and 'trigger 1 SSC' set the retain storage (FC253), CDA priority, and CDA condition triggers (E2). 'CDA condition' is set to block the turn-on to the ending trigger at the completion of the trigger 1 sequence.

The DCR (B5) and storage cycle (C6) latches are set to request a storage cycle (BCU) for the data held in the data register. The storage address is

gated from the data address field of the current UCW 0 to the SAB register (B8). Because a new CCW is to be fetched, the operation code (bits 6 and 7), the PCI (bit 36), and the data check (bit 44) are gated from the control register to a buffer. The normal channel-to-BCU sequence is performed, and the last double word of data is stored in main storage.

A data address update is performed (incremented by 8), and the result is returned to the control register (FC253). 'Data stored' is sent to the SSC to reset the B register full latch. 'CDA condition' causes a UCW 2 fetch and turns off 'control register full' (F8). 'Word 2 fetched' turns off the main channel clock and turns on trigger 2 (A9). With trigger 2 on, trigger 1 is turned off.

'Trigger 2,' 'storage cycle over' and 'not check condition' turn on the main channel clock (B11) and the CCW required latch (C11). 'CCW required' initiates a CCW fetch from main storage. The command address field of UCW 2 provides the CCW address. A new UCW 2 must be formed.

Bytes 1-3 of the control register (command address) are placed in the adder (C11). From the adder, the command address is gated to bytes 5-7 of the control register to become the new residual command address (C11). Next, the contents of the adder are incremented by 8 (D11) and the result is placed in bytes 1-3 of the control register to become the new command address (E11). UCW 2 is now updated; therefore, trigger 2 is reset (E10), trigger 3 is set (E12), UCW 2 is stored (E11), and the main channel clock is turned off (E11).

When the CCW arrives from main storage, 'storage cycle over' is set. If no errors occurred during the storage cycle, 'storage cycle over and no check' becomes active. 'Storage cycle over and no check' and trigger 3 turn on the main channel clock (A14). A new UCW 0 must be formed.

As the CCW is gated from the data register (FC255) to the control register, the operation code (bits 6 and 7), the PCI bit (bit 36), and the data check bit (bit 44), are gated from the buffer to their respective bit positions in the control register. The DAB is gated to the DAB register in correct form (true for read and complement for read backward). For a read backward, the DAB is gated back into the DAB field of the control register (D14). The corrected DAB and the count are added (B14) and the result (major count plus end count) is gated to control register bits 48-63 (C14).

If an overflow occurs during this add operation, the overflow bit is placed in bit 47, and bit 46 is turned on to correct parity. The count is examined for last word (Count $<$ 8) or double last word (8 $<$ count $\leq$ 16) and the condition (if present) is indicated to the SSC (D13). 'CCW gate' is sent to the SSC to cause the end count, byte count, and flags to be gated into the SSC registers. UCW 0 is stored (E14) and the ending trigger is set (E14). 'Ending' resets trigger 3 and frees the main channel for a new operation (FC255).

With the new CCW in UCW 0, the read operation continues. When this count is exhausted, the trigger 1 sequence again examines the flag field of UCW 0. If the CDA flag is on again, the CDA sequence is repeated. If CDA is not indicated, the 2870 either accepts the device's status and ends the operation, or, if the chain command flag is on, the 2870 chains to a new CCW and performs the command indicated.

SELECTOR SUBCHANNEL WRITE/CONTROL

- A write operation transfers data from main storage to the selected I/O unit.
- Control and write commands are executed by the channel in the same manner.
- The I/O control unit detects the difference between write and control operations.
- Write operations require data transfer, but control operations may not.

Control

A control command is executed in the same manner as a write command. The difference between a write or control operation is detected by the control unit. Execution of a control command does not usually require data transmission across the interface. After the channel designates the specific control operation in the command byte, the addressed I/O unit performs the operation without intervention from the channel.

The types of operation that can be performed by a control command depend on the device selected. For example, a control command can initiate a rewind, backspace, or forward space operation on a magnetic tape unit. If the command code does not specify the entire control function, the data address field of the CCW designates the main storage location that contains the required additional information. CD, CC, SLI, and PCI flags are examined during a control operation.

Write

- Start I/O sequence forms UCW 0 and 2, and initializes the SSC end count, byte count, and flag registers.

- After the device is selected, two double words of data are fetched from main storage and are placed in the SSC A and B registers.

- Bytes of data are sent from the SSC B register to the I/O control unit until a double word is transferred (byte count equal 0).

- When the B register full latch is reset (by byte count equal 0), the A register contents are transferred to the B register and a main channel data cycle is requested.

- Main channel trigger 1 sequence fetches a double word of data from main storage and transfers it to the SSC A register.

- During the trigger 1 sequence, the data address in UCW 0 is incremented by 8 and the count is decremented by 8.

- A write operation is terminated by the SSC when the byte count equals the end count on the last word.

- A control unit may end the operation at any time by raising 'status in' and presenting a status byte.

- COD-18.

All references in this section are to Figure IOP 23 in the diagram manual.

During the start I/O sequence for a write operation, UCW 0 and 2 are formed and the SSC end count, byte count, and flag registers are initialized (FC907). To begin an SSC write operation, two successive trigger 1 sequences are performed to buffer two doublewords of data in the SSC A and B registers.

When the A and B register full latches are on, 'service out' is sent to the control unit (FC907). The control unit returns 'service in' and a byte of data is sent to the control unit (FC913). The operation continues with the service in/service out signal exchange for each byte of data transferred. The SSC byte counter controls the gating of the bytes of data and signals the end of a doubleword by raising 'byte count equal 0.' 'Byte count equal 0' gates the A register contents to the B register and turns on SSC data cycle and SSC priority request to the main channel (FC915). Priority response sets trigger 1 (B2), and UCW 0 is read from local storage (B2).

The main channel clock is turned on to control the time sequence of trigger 1 (B3). The count is gated to the adder, decremented by 8 (C3), and the result is returned to the control register (F3). Before the count is decremented, it is examined for 'count less than 24' (D1) (FC251). 'Count less than 24' indicates that the last double word of data will be fetched from main storage during this sequence.

The DCR latch is set (E1) and the data address is gated to the SAB register (D4). 'Storage request' is sent to the BCU (E4) and the data fetch latch is set (E3). A normal BCU-to-main channel data fetch sequence is performed. As in the CAW or CCW fetch, 'advance' (FC551) indicates that the data is on storage bus out, and the channel gates this data into the main channel data register.

'Advance' also conditions an AND circuit to activate 'data in gate' to the SSC (G4). 'Data in gate' turns on the A register full latch (D6) and gates the double word of data from the data register to the SSC A register (D8).

While the data fetch is in operation, the data address is updated. The data address is gated from the control register to the adder (A7), incremented by 8, and the result is stored in the data address field of the control register (B7) (FC251). After the data address field is updated, UCW is not needed. Therefore, UCW 0 is stored in local storage and 'control register full' is turned off. The main channel clock is turned off and the main channel waits for the completion of the main storage cycle.

'Main storage over and no check' indicates that the double word of data has been fetched and gated into the SSC A register. 'Main storage over and no check' turns on the ending trigger (C7) to free the main channel for other operations.

A write operation continues transferring data bytes until either the SSC or the control unit issues a signal to end the operation. SSC ends the data transfer when the byte count equals the end count on the last word. If a control unit raises 'service in' after the byte count equal end count condition is detected, the SSC responds with 'command out.' A control unit interprets 'command out' in response to 'service in' as a stop command. The control unit terminates an I/O operation by presenting 'status in' and a status byte on bus in.

Selector Subchannel Write CDA

- If the CD flag is on (a 1 in bit position 32), a new CCW is also fetched during the data fetch cycle in which the main channel count becomes less than 16.

- If the original CCW count is greater than 16, main channel initiates the CDA sequence (FC257).

- When the original CCW count is less than 16, the SSC initiates the CDA sequence after the first double word of data has been transferred across the I/O interface.

- The new CCW is modified to form a new UCW 0, and bit 39 is set to indicate that UCW 0 contains a prefetched CCW.
- Trigger 1 performs the data fetches.
- Trigger 2 sequence begins the CCW fetch and updates UCW 2 (FC259).
- Trigger 3 sequence forms a new UCW 0, sets bit 39 (prefetch), and stores the new UCW 0 (FC261).
- While the SSC exhausts the byte count for the present CCW, the SSC makes a priority request for both data and the new CCW.
- 'SSC new CCW' and 'priority response' cause UCW 0 to be read from local storage and the new end count, byte count, and flags are sent to the SSC.
- Two doublewords of data are placed in the SSC A and B registers and the write operation continues under control of the new count, data address, and flags.
- COD-20, -21.

All references in this section are to Figure IOP 24 in the diagram manual.

After performing the data transfer specified by a CCW, the activity initiated by start I/O can be continued by chaining (fetching a new CCW). Each main storage to SSC data fetch is performed under the control of the trigger 1 sequence. Each time a trigger 1 sequence is performed, the count field is decremented by 8 and examined for double last word (count less than 16) or last word (count less than 8) condition. The double last word indicates that the SSC has the last doubleword of data in the A register. Last word indicates that the last doubleword of data is in the SSC B register and that the operation must end when the byte count equals the end count. However, if the CD flag is on for a write operation (FC257), a new CCW can be fetched when the count becomes 16 or less (double last word).

A write CDA CCW fetch can be initiated by either the SSC or main channel. If the initial count field of UCW 0 is greater than 16 (FC257), main channel initiates the CCW fetch sequence during the data fetch cycle for the last double word of data (Count goes from > 16 to < 16).

A special case occurs when the initial UCW 0 count is less than 16. Because the SSC already has all data for this operation (loaded before the write operation began), the SSC initiates the CCW fetch after the first double word of data is transferred. This delay is necessary to insure that a new CCW is not fetched before the current operation begins.

As in read CDA, trigger 2 is turned on to initiate the CCW fetch and update UCW 2 (FC259). When the new CCW arrives, the trigger 3 sequence (FC261) forms a new UCW 0 which replaces the old UCW 0 in local storage. To indicate that UCW 0 now contains the next CCW's information, bit 39 (prefetch) is set in UCW 0.

When the SSC transfers the last data byte for the old CCW, the CDA flag causes an SSC priority request for another data fetch cycle. Priority response and 'SSC data cycle' cause UCW 0 to be read out and turns on trigger 1. The SSC write chain data latch is on because this is the end of a write CDA CCW. The prefetch bit in UCW 0 sets the data only latch and causes main channel to send CCW gate to the SSC (FC263). CCW gate causes the SSC to gate in the new byte count, end count, and flags from UCW 0. The trigger 1 sequence fetches data for the SSC, the prefetch bit is turned off, and the write operation continues.

SELECTOR SUBCHANNEL CHAIN COMMAND

- If the chain command flag is on when the SSC receives device end, a chain command cycle is performed.
- A new CCW is fetched from the address held in UCW 2.
- UCW 0 is formed from new CCW.
- SSC reselects the device with the command, flags, end count, and byte count taken from the new CCW.
- COD-22.

If the SSC flag register contains the chain command (FC919) (CC) flag, the SSC monitors for the device end bit in any status bytes presented by the control unit. Assume that a data transfer operation is completed, and the control unit presents a status byte with channel end and device end. The SSC gates in the status byte and examines it and the SSC flag register for command chaining conditions.

If command chaining is indicated (CC flag and device end), the SSC requests main channel priority for a chain command cycle. When the SSC receives priority, main channel reads out UCW 2 to determine the address of the next CCW. UCW 2 is updated and a main storage request for the new CCW is made.

When the new CCW arrives, it is gated into the data register. From the data register, the CCW is gated into the control register. During the data-to-control-register transfer, byte 0 is encoded into a two-bit operation code and the key field of UCW 2

is retained. At this time, the control register contains the keys, operation code, data address, flags, and original count from the CCW.

For SSC operations, the count is modified by adding the DAB to it and placing the result in the count field of the control register. The new UCW 0 is now formed. The CCW gate signal gates the new flags, end count, and command byte (from byte 0 of the data register) into the SSC; UCW 0 is stored. The 'ending' trigger is set to release main channel.

While the main channel circuits were fetching the CCW, the SSC began to reselect the I/O device. The device reselection sequence is the same as a start I/O initial selection, except that the SSC already has the unit address of the device it wishes to select. As in start I/O, the SSC must wait for the completion of the CCW fetch before it can send the I/O command to the device and complete the reselection. 'CCW gate' signals the SSC to ingate the new command, flags, byte count, and end count from main channel. The SSC then issues the I/O command to the device and waits for the device to present status. When the device presents status information, the status byte is examined. Status equal zero allows the new I/O operation to proceed (for a write operation, data is now fetched). Non-zero status causes an I/O disconnect, and the new command is not initiated. The new I/O operation now proceeds as outlined in the read or write sections.

Chain Command Operations

When a control unit wishes to present status information to the SSC, it raises the 'status in' interface line and places its status byte on the I/O bus in. (See COD-22.) 'Status in' turns on the SSC clock. At time A3, the I/O disconnect latch is set, which turns off the SSC clock. The off condition of the SSC clock turns on the I/O disconnect condition latch, which turns the SSC clock back on. In addition, the data cycle latch is reset (if on), and the status byte is gated from the I/O bus into byte 4 of the A register.

At A1 time, the control unit status and any channel status in the SSC are gated unchanged through the A register to the B register. Then the SSC flag register is checked to determine whether the chain command flag is on. If it is and the status byte only contains device end, and channel end or the status modifier (any other bits cause a CSW cycle) the CC sync latch is set at time A1. If this is an output operation, the byte count backup register is also reset at the same time. At A3 time, the I/O disconnect and A3 latch is set and 'service out' is then raised to disconnect the control unit from the I/O interface (its status byte has been accepted) (FC919).

Because the CC sync latch is on, 'suppress out' is raised to the control units, and the CC control and CCW request latches are set to initiate a CCW cycle in main channel. The SSC now raises its secondary priority request line to vie for priority in main channel to perform the CCW fetch sequence. In addition, the SSC selected latch is set (FC901) and 'select out' is dropped.

The SSC selected latch causes the SSC to begin to reselect the I/O device in parallel with the CCW fetch. This device selection is identical to the SSC start I/O selection sequence shown in Figure IOP 20 sheets 4 and 5, except that the CC control trigger blocks the ingating of the SSC UAR (Figure IOP 20, A15). As in start I/O, the device selection sequence continues until 'address in' and 'operational in' are active. The SSC now waits for the CCW fetch to complete before it completes the device selection. Details of the device selection sequence can be found in the Selector Subchannel Initial Selection section.

When the SSC is granted priority, main channel checks for the status modifier bit in the status byte (FC305). If the status modifier bit is on, the trigger 8 sequence is performed before the CCW fetch. Trigger 8 reads out UCW 2, increments the command address field by 8, and turns on the SSC pseudo start I/O and SSC-CCW-CC-required latches in main channel. In this case, the command address is incremented on command of the control unit, and thus a CCW is "skipped." If the status modifier bit is not on, the SSC pseudo start I/O and SSC-CCW-CC-required latches are set when priority is granted. The SSC-CCW-CC-required latch causes the start I/O CCW fetch sequence to begin as though the CCW required latch had been set (Figure IOP 20, D5) (FC105).

Main channel now reads out UCWs 0 and 2, turns on the main channel clock, and begins a CCW fetch using the command address from UCW 2. While the CCW is being fetched from main storage (FC551), UCW 2 is updated and stored in local storage. When the new CCW arrives from main storage, a new UCW 0 is formed from it. At the completion of the UCW 0 formation, the 'CCW gate' signal is raised to the SSC. The 'CCW gate' signal causes the SSC to ingate the new flags, end count, and command byte; UCW 0 is stored (FC107). The ending latch is set to release main channel. Details of the CCW fetch and UCW 0 and 2 operations are found in the Selector Subchannel Start I/O section. The only difference in this operation is that 'initial selection' is not sent to the SSC, and the 'SSC-CCW-CC-required' latch is reset when the CCW in channel latch is set.

The CCW gate signal causes the SSC to gate in the new CCW information (FC903). The SSC now completes the reselection of the I/O device. When the control unit returns status information, the status is examined for 'status equal zero' condition.

'Status equal zero' tells the SSC that the I/O device has accepted reselection and the new I/O command (FC907). The new data transfer operation is now performed. If the status returned is not equal to zero, an I/O disconnect is performed and the new command is not executed.

SELECTOR SUBCHANNEL HALT I/O

- CPU sends 'select' and 'halt I/O' with a unit address for a device.
- An invalid unit address causes the main channel to release the CPU with condition code 11.
- If the SSC is busy, halt I/O and SSC select cause an interface disconnect sequence to be performed, regardless of the device that is operating on the subchannel.
- If the SSC is busy and has an interrupt pending, the CPU is released with condition code 00.
- If SSC is idle, the device is selected, an interface disconnect sequence is performed to halt the device, and the CPU is released with condition code 01.
- If 'select in' returns during the device selection sequence, the CPU is released with condition code 11.

All references in this section are to Figure IOP 21 in the diagram manual.

CPU initiates a halt I/O instruction by activating the halt I/O and select channel lines to the 2870 and sending the unit address of the device on the unit address bus out (FC131). 'CPU select' and 'halt I/O' cause a main channel priority request. When priority is granted, the unit address is gated into the initial unit address register and from the initial unit address register to the unit address OR. The output of the unit address OR is fed into the address decoder. The address decoder determines which SSC is being addressed and whether the addressed SSC is installed or busy.

If the addressed SSC is not installed, CPU is immediately released with condition code 11 (FC131). If the SSC is installed, three conditions may exist in the SSC: the SSC may be busy, the SSC may be busy with a pending interrupt, or the SSC may be idle.

If the halt I/O is issued to an SSC with a pending interrupt, CPU is released with condition code 00. The interrupt remains pending in the SSC.

When the halt I/O is issued to a working (busy) SSC, the SSC raises 'address out' and 'select out' and then drops 'select out' (FC911). The control unit operating on the I/O interface (regardless of its address), immediately disconnects itself from the interface and CPU is released with condition code 10. The SSC will have an interrupt request pending.

When the SSC is idle, halt I/O causes an initial selection sequence for the addressed device. If the device responds with its operational in line, an interface disconnect is signaled, bytes 4 and 5 of the CSW formed contain zeros, and the CPU is released with condition code 01. If the device presents status, the device status is placed in the CSW with zeros in the channel status byte. Should 'select in' be returned for 'select out' during the initial selection sequence, CPU is released with condition code 11.

Halt I/O and CPU select channel (A1) are ANDed to cause a main channel priority request (A4). 'Priority response' and 'response delayed' turn on the main channel clock (B2), halt I/O latch (B1), and the gate latch (B3). 'Gate' causes the unit address to be gated into the initial unit address register (B3), and from the initial unit address register to the unit address OR (B4). The output of the unit address OR is fed to the unit address decoder (B4).

If the SSC address is invalid, the CPU is released with condition code 11 (C4). 'SSC decoded' and 'halt I/O' turn on the SSC select latch (C3), and SSC select is raised to the addressed SSC (B4). If 'SSC busy' is not on in the addressed subchannel, the halt I/O channel free latch is set (C3) in the main channel. 'Halt I/O channel free' blocks the trigger 5 sequence and allows trigger 7 to be used for the subsequent CSW cycle. 'Ending' is set (D4) to free the main channel for other operations or possible status from a halted device.

Halt I/O to an SSC with Interrupt Pending: If an interrupt remains pending from any previous operation, 'SSC busy,' 'interrupt pending,' and 'SSC working' are active. SSC working holds 'tie break' active (A6) to hold 'SSC selected' reset (A7). 'Halt I/O' and 'SSC select' are ANDed with 'not SSC selected,' 'interrupt pending,' and 'SSC busy' to send 'accept' to the main channel (B8). Accept causes the main channel to release the CPU with condition code 00 (FC911). The interrupt remains pending.

Halt I/O to an Idle SSC: Two conditions are possible if the unit address is valid and no interrupt is pending in the SSC: the subchannel can be idle or busy. Assume that the subchannel is idle. 'SSC select' and 'halt I/O' set the SSC selected latch (A6). 'SSC selected' turns on the SSC clock (A8) and gates the unit address into the SSC UAR (A8) (FC901). A3 gate from the SSC clock turns on 'SSC busy' (B6) and

'SSC initial select' (C6). 'Busy' turns off the SSC clock (A8).

With 'SSC initial select' on and the clock off, the SSC initial select B latch (C6) is reset. With 'SSC initial select B' off, the SSC clock is turned on to test for a possible unit address check at A2 (D7) and 'address out' is raised at A3 (D7). 'Address out' turns on the SSC initial select B latch, which turns off the clock. With 'address out' up and the clock off, a latch (E6) is set to raise the 'SCIS and address out' line, which turns the clock on again (E8). 'A3 gate' turns on the select out latch (E7) (FC903), and 'select out' is sent to the control unit. The addressed I/O control unit captures 'select out' and returns 'operational in.' If none of the control units recognize the address on bus out, 'select out' returns as 'select in,' 'no selection' is activated to the main channel, and the CPU is released with condition code 11.

'Operational in' removes the address from bus out and resets the address out latch (D7). The fall of 'address out' causes the control unit to respond with its address on bus in and the 'address in' tag. 'Address in' and 'operational in' turn on the SSC clock (A12). If the address sent by the control unit matches the address in the SSC UAR, an address match condition exists.

Because the operation is not a start I/O, address match condition turns on the 'address match and A3' latch without the command loaded condition. With 'address match and A3' on, the SSC clock is turned off and the reset line to the address match latch is removed. At this time, the SSC should raise 'command out' to the control unit. However, because this is a halt I/O operation, the address out halt I/O latch is set to raise 'address out' and block 'command out' (FC907). The I/O disconnect latch is also set to cause an I/O interface ending sequence (FC919).

To send 'halt I/O' to the control unit, the interface disconnect sequence (raise 'address out' and 'select out' and then drop 'select out') is now performed. With the I/O disconnect latch on, the clock is turned off and the I/O disconnect condition latch is set by 'not A3 gate turn-off delayed' (D10). The I/O disconnect condition turns on the SSC clock (D11). A3 gate sets the I/O disconnect and A3 latch (D10). I/O disconnect and A3 activate CSW condition to reset the select out latch (E7) and cause 'select out' to the control unit to fall.

When the control unit recognizes 'address out' and 'not select out,' it immediately drops all in-tags and presents ending status. The fall of the in-tags causes the SSC to turn off the I/O disconnect latches and turn on 'priority request' to the main channel to initiate a CSW cycle. The trigger 7 sequence assembles the CSW (0s in bytes 4 and 5), stores it in main storage location 64, and releases the CPU with condition code 01.

Halt I/O to a Busy SSC: If the SSC is operating with a device, SSC select and halt I/O cause the interface disconnect sequence to be performed, regardless of the device on the interface. Because the device has already been selected, a selection sequence is not performed. With a device on the interface, the SSC sets the select out and SSC busy latches, and 'SSC selected' is reset. Therefore, 'halt I/O' and 'SSC select' from the main channel set the halt I/O busy latch and the not SSC selected latch (F8).

'Halt I/O busy' is set by 'halt I/O', which conditions the AND side of the halt I/O tie break latch (FC911) (F7). With the halt I/O tie break latch set, the halt I/O busy latch is set. 'Halt I/O busy' turns on the SSC clock. A2 and 'halt I/O busy' set the address out halt I/O latch (B11) to raise 'address out' to the control unit. 'A3 gate' and 'halt I/O busy' turn off the select out latch and 'select out' to the control unit falls. When the control unit recognizes 'address out' up and 'select out' down, it immediately drops all in-tags to the SSC.

When 'operational in' falls, I/O disconnect is turned on and incorrect length is indicated if a data transfer operation is terminated. With the I/O disconnect latch on, the clock is turned off to allow the I/O disconnect condition latch to be turned on. 'I/O disconnect condition' turns on the clock (FC919), gates the status on bus in to the A register, and turns on the I/O disconnect and A3 latch.

'I/O disconnect and A3' turns on the CSW cycle latch. 'CSW cycle request' causes the SSC to request priority. 'SSC priority response' turns on the interrupt pending latch and CSW cycle to the main channel. SSC busy causes the trigger 5-6 sequence to be used for the CSW cycle (FC301). The trigger 5-6 sequence assembles the CSW and stores it in UCW 2 (of the device involved). The CPU is released with condition code 10, and an interrupt from the SSC to CPU remains active.

SELECTOR SUBCHANNEL TEST I/O

- CPU sends 'select' and 'test I/O' with a unit address for a device.
- An invalid unit address releases the CPU with condition code 11.
- If SSC is busy with a device other than the one addressed, the CPU is released with condition code 10.
- If an interrupt is pending for the device addressed, the trigger 11 sequence is used to handle the CSW cycle.
- A test I/O to an idle SSC causes the device to be selected and status information to be requested.

- Zero status returned causes a CPU release with condition code 00.
- Nonzero status causes a CSW cycle and the CPU is released with condition code 01.
- If no selection occurs, the CPU is released with condition code 11.

All references in this section are to Figure IOP 22 in the diagram manual.

CPU initiates a test I/O instruction by raising 'select channel' and 'test I/O' and placing the unit address of the device on the unit address bus out (FC351). Test I/O and CPU select channel cause a main channel priority request. When priority is granted, the unit address is gated into the initial unit address register and from the unit address OR to the address decoder. The address decoder determines whether the addressed SSC is installed, and, if installed, whether the SSC is busy or idle. If the SSC is not installed, the address is considered invalid and CPU is released with condition code 11.

If the addressed SSC is busy, these conditions may exist in the SSC: the SSC may be operating with the addressed device, the SSC may be operating with another device, an interrupt may be outstanding for the addressed device, or an interrupt may be pending for another device. To determine which condition exists in the SSC, the unit address supplied by the CPU is compared with the address in the SSC unit address register and the interrupt pending line is tested.

If the SSC is busy and the addresses do not match, CPU is released with condition code 10, regardless of the condition of the interrupt pending line. Condition code 10 indicates to the CPU that the test I/O operation cannot be performed (FC121). Any interrupt conditions remain pending.

Address match and an interrupt pending condition (FC353) indicates that a CSW has been formed and is temporarily stored in UCW 2 of the addressed device. The trigger 11 sequence (FC351) is used to transfer the CSW from local storage to main storage and CPU is released with condition code 01.

If the SSC is not busy (idle) the SSC performs an initial selection sequence (as in start I/O) for the addressed device (FC121). However, the command placed on I/O bus out is a P bit only (0 command). A command code of zero is interpreted by the control unit as a test I/O command (FC907). When a control unit receives a test I/O command, the control unit immediately raises 'status in' and places its status byte on the I/O bus in. The SSC examines the status byte for a bit in any position. If the status byte is zero (P bit only) (FC907), CPU is released with condition code 00, which means that the device is free to accept a start I/O instruction. Non-zero status causes a trigger 7 CSW sequence to be performed. Under trigger 7, a CSW is assembled, stored in main storage, and CPU is released with condition code 01.

'CPU test I/O' and 'select channel' activate main channel priority request. 'Main channel priority response' and 'response delayed' turn on the test I/O latch (B1), turn on the clock (B2), and gate the unit address into the main channel (A4) (FC121). Test I/O blocks log interruptions (B3), and log sequences (B2). The unit address is decoded and used to test the condition of the SSC. If an uninstalled SSC is addressed (invalid address), the CPU is released with condition code 11 (C2).

Test I/O to a Busy SSC: 'SSC valid and busy' and 'not address match' indicate that the SSC is performing an operation with some device other than the one specified (FC121). To indicate to the CPU that the test I/O operation cannot be performed, the CPU is released with condition code 10 (C2).

Test I/O to an SSC with a Pending Interrupt (FC351): 'Address match' and 'interrupt pending' activate 'test I/O and address compare' to indicate that a CSW for the addressed device has previously been formed and is stored in UCW 2. 'Test I/O and address compare' fetches UCW 2 (D2), forces a priority response to the SSC (E2) (FC121), turns off the main channel clock, and turns on trigger 11 (E3). The trigger 11 sequence stores the CSW in main storage and releases the CPU with condition code 01.

Test I/O to an Idle SSC: If the SSC is not busy and does not have an interrupt pending, the SSC selects the device and issues a command byte of all 0s (test I/O command). When the unit address is decoded, the SSC select latch is set (C3) (FC901) and 'SSC select' is sent to the SSC (C4). SSC select and test I/O set the test I/O latch (B6), remove the set to 'tie break' (A6), and remove the reset to 'SSC selected' (A7). With the tie break latch off, the SSC selected latch (A7) is set.

'SSC selected' causes the I/O initial selection sequence to be performed with a 0 command code (test I/O) (FC907). When the control unit receives an I/O command of 0 (P bit only), it raises status in and places its status on bus in. The SSC examines the status byte for a bit in any position. If the status byte is 0 (P bit only), accept is sent to the main channel (B6). Accept causes a CPU release with condition code 00 (B4).

Non-zero status indicates that a trigger 7 sequence is necessary to form a CSW and store it in main storage. The trigger 7 sequence assembles an eight-byte CSW, stores it in main storage location 64, and releases the CPU with condition code 01.

TEST CHANNEL

- CPU raises the test channel and select channel lines.
- The test channel instruction does not interrupt channel operations.
- A test channel instruction results in a CPU release with a condition code that indicates the condition of the channel interfaces.
- CPU release code 00 means that at least one of the interfaces is not in burst mode and no interrupt is pending in the channel.
- CPU release code 01 means that an interrupt is pending in the channel and at least one of the available interfaces is not in burst mode.
- CPU release code 10 indicates that all interfaces are in burst mode.
- CPU release code 10 does not test for the interrupt pending condition.

All references in this section are to Figure IOP 60 in the diagram manual.

The test channel instruction is initiated when the CPU raises the test channel multiplex line and signals the proper channel (2870) with the channel's select channel line. No unit address is sent with the test channel instruction. Because test channel only samples the status of the channel, no priority request is made and the 2870's operations are not disturbed. Test channel's only function is to send the CPU a condition code that describes the present state of the channel.

'CPU test channel' and 'select channel' turn on the test channel 1 or test channel 2 latches (A2) (FC141). Test channel 1 latch indicates that an interruption is pending in the channel. Test channel 2 is turned on if no interrupts are pending.

The CPU is released with a condition code determined by: test channel 1, test channel 2, SSC 1-4 busy conditions, and multiplex subchannels in byte or burst mode (C3). Test channel 2 and either one SSC not busy or the multiplex subchannels in byte mode, cause CPU to be released with condition code 00 (A4). Test channel 1 (interrupt pending condition) and either one SSC not busy or the multiplex subchannels in byte mode, causes the CPU to be released with condition code 01 (A4). If a multiplex subchannel is in burst mode and all SSCs are busy, any pending interrupt conditions are ignored and either test channel 1 or test channel 2 cause the CPU to be released with condition code 10 (B4).

ADDRESS PREFIXING FEATURE

- Used with multiprocessor system.
- Identifies all data transferred to or from the system with the CPU that initiated the operation.
- Feature logic de: ıl is in the 2870 ALDs.

The 2870 address prefixing feature allows a system to communicate with a channel when the channel can be controlled by more than one CPU. In a multiple CPU system, the 2870 can perform operations with more than one CPU simultaneously. Therefore, the identity of the CPU that initiates an operation must be preserved.

Actual communication between the channel and the system is performed via a channel control unit (CCU). The 2870 recognizes the CCU as a processor and the operation of the 2870 is not changed. Address prefixing is not under program control. The data transfer rates of the 2870 are not affected by address prefixing. There are no facilities for off-line testing of the 2870 prefix feature. No alteration of the CE or manual controls of the 2870 occurs when this feature is installed.

System Interface

Address prefixing adds new lines to the 2870 CPU and BCU interfaces. These lines connect the 2870 to a CCU (Figure 4-1). No existing lines on the CPU and BCU interfaces are modified by this feature.

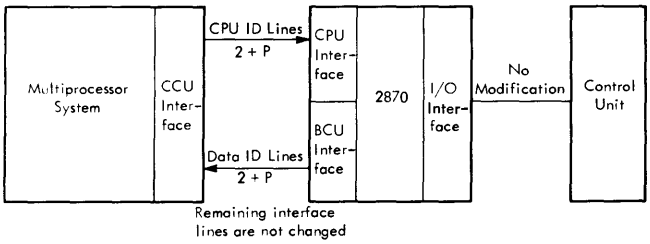


Figure 4-1. Address Prefixing Interface Lines

Three incoming multiplex lines are added to the channel/CPU interface: CPU identity (ID) line 1, CPU ID line 2, and CPU ID line parity. These lines are valid for either of two conditions:

1. The duration of the CPU select channel line.
2. The duration of the CPU interrupt response line.

The CPU ID lines identify which CPU in the system is selecting the channel, or which CPU is accepting the channel interrupt.

Three outgoing simplex lines are added to the BCU interface: data ID line 1, data ID line 2, and data ID line parity. The data ID lines are active when the 2870 sends a storage request to the CCU. These lines are valid for the duration of the address valid line from the 2870.

The data ID lines identify a storage operation as belonging to a specific CPU. No existing BCU interface lines are changed by the feature.

I/O Interface

The 2870 channel-to-control unit I/O interface is not modified in any way by the address prefixing feature. Channel operations over the I/O interface are not affected and the attached control units are not aware of the existence of this feature.

Functional Units

CPU Identity Register

The CPU identity register is a storage unit made up of three latches (bit 1, bit 2, and parity). Each time the main channel receives an instruction from the CPU, the accompanying ID bits are placed in the ID register. From the ID register, the ID bits can be stored in UCW 0 and 2 (via the control register) or gated to the data ID lines.

The identity register can be loaded from either the CPU or bits 37 and 38 of the control register. To load the ID bits supplied by the CPU, the 'gate CPU ID bits to ID register' line is activated (Figure 4-2). This line is active each time start I/O, IPL, interrupt response, or FLT is active to the

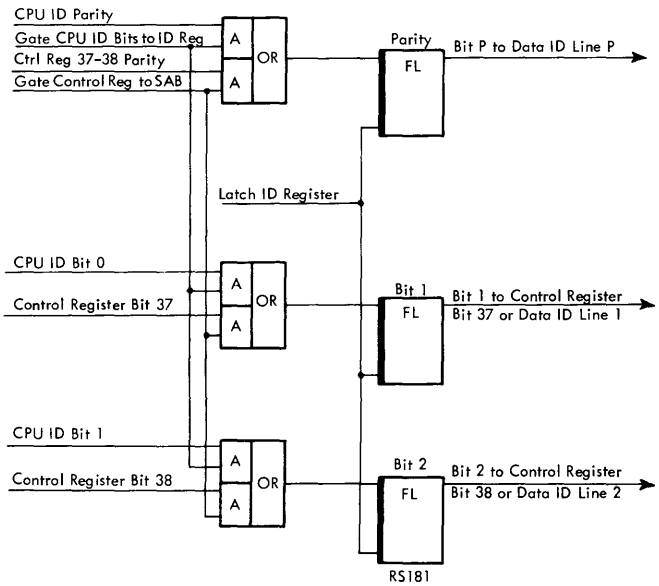


Figure 4-2. CPU Identity Register

main channel. Bits 37 and 38 of the control register are gated into the ID register by the 'gate control register to SAB' line. This line is active when UCW 2 is used to fetch a CCW, or when UCW 0 is used for data transfers (read or write).

The output of the identity register is gated to either the control register or to the BCU data ID lines. ID bits are transferred from the ID register to the control register when:

1. The CAW is gated from the data register to the control register. This stores the ID bits in UCW 2 bits 37 and 38

2. The CCW is gated from the data register to the control register. This stores the ID bits in UCW 0 bits 37 and 38.

ID bits are placed on the BCU data ID lines for all channel-to-main-storage operations. For CCW fetch or data operations, the ID bits from a UCW are placed in the ID register and then gated onto the data ID lines. If a start I/O CAW fetch, CSW cycle, FLT operation, or IPL is performed, the ID bits supplied by the CPU are used.

The channel does not check the parity of the ID bits from the CPU. However, on each storage cycle that the channel uses the ID bits from local storage, the parity of byte 4 of the control register is checked. If byte 4 has bad parity, bad parity is placed in the ID register. Because the CCU checks the parity of the data ID lines, bad parity in byte 4 prevents the CCU from completing the operation. If byte 4 has good parity, the channel generates parity on the ID bits.

UCW Modifications

Because each operation on the 2870 must now be identified with a CPU, the identity of the CPU is retained in UCW 0 and 2 for each device. This is done by placing the two-bit ID code in bits 37 and 38 of UCW 0 and 2. The CPU code is:

Bit 37	Bit 38	Processor
0	0	1
0	1	2
1	0	3
1	1	4

UCW 0 and 2 always contain the CPU ID bits of the last CPU to successfully use the device (Figure 4-3). The ID bits are changed only when a start I/O instruction is issued to an idle subchannel or IPL is issued to the channel.

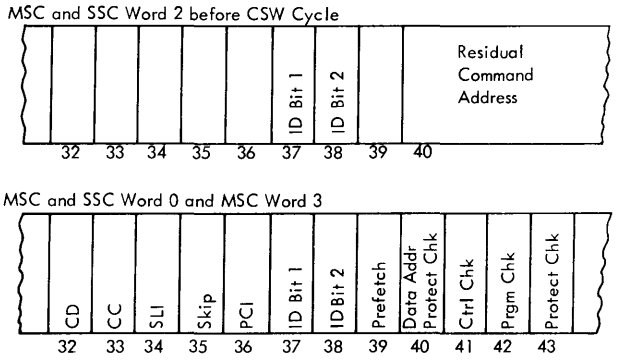


Figure 4-3. Unit Control Words with CPU ID Bits

Principles of Operation

The address prefixing feature keeps the system aware of which CPU in the system is now communicating with or last communicated with any device on the 2870. Address prefixing supplies ID bits with the storage address each time the channel requests a storage operation.

Start I/O

When a start I/O instruction is executed, the ID bits from the CPU are gated into the channel ID register. To fetch the CAW, address 72 is placed on the SAB, the contents of the ID register are placed on the data ID lines, and storage request is raised. The CAW arrives at the channel and is gated into the data register.

When the CAW is gated from the data register to the control register, the ID bits are placed in bits 37 and 38 (the parity bit is dropped) to cause the CCW ID to be stored in UCW 2. The channel fetches the first CCW by using the command address from the CAW and the contents of the control register. As the CCW is gated from the data register to the control register (to form UCW 0), the ID bits are placed in bits 37 and 38 to identify all data transfers for this CCW.

Data Transfer

For each main storage data fetch or store operation, UCW 0 provides the data address. The CCU requires

that the ID bits of the CPU that initiated the operation be sent with the data address for a storage operation (fetch or store). To load the ID register, bits 37 and 38 are gated from UCW 0 in the control register to the ID register.

As bits 37 and 38 are transferred, the parity of byte 4 of the control register is checked. If byte 4 has bad parity, bad parity is forced in the ID register to prevent the CCU from completing the storage cycle. If byte 4 has good parity, the ID register parity bit is adjusted so that odd parity results in the ID register. All parity checking on the ID bits is performed by the CCU.

Chaining

When chaining is indicated, a new CCW is fetched when the old count is exhausted. CCU requires that the CPU ID bits be sent to the CCU with the new command address. To load the ID register, bits 37 and 38 of UCW 2 are gated from the control register to the ID register. Parity is adjusted (odd) if byte 4 has good parity. As in data fetch operations, bad parity in byte 4 causes bad parity in the ID register, and the CCU does not complete the CCW fetch.

IPL, CSW, FLT, or Logout

For IPL, CSW, FLT, or logout operations, the subchannel ID bits are not used. The CPU ID bits supplied by the CPU that accepts the interrupt are gated into the ID register at the beginning of the operation. Each time the channel makes a storage request, the ID register contents are gated to the ID lines. The ID bits held in UCW 0 or 2 are not changed during these operations.

MODEL 75 ATTACHMENT FEATURE

- Allows the 2870 to be attached to the processor of an IBM System/360 Model 75.
- Does not alter the operation of the 2870.
- Feature logic detail is found in the 2870 version 001 ALD.

To allow the 2870 to operate with the processor of an IBM System/360 Model 75, the Model 75 attachment feature must be installed in the 2870. This feature changes the CPU and BCU interface circuits of the 2870 so they are compatible with the minus signal levels used by the Model 75. Without this feature, the 2870 is designed to operate with the processor of a System/360 Model 65, which uses a positive level as the active state of its interface lines. The Model 75 attachment feature consists of inverter circuits, for both input and output lines, which allow the 2870 to operate with a Model 75.

Operation of the 2870 is not changed by this feature. There are no facilities for off-line testing of the Model 75 attachment feature. No alteration of the CE or manual controls of the 2870 occurs when this feature is installed.

Note: If CPU power goes down with this feature installed, the processor/channel interface lines "float" to an active level. The 2870 can be operated in test mode, for off-line testing, with CPU power down.

MODEL 90 SERIES INTERFACE FEATURE

- Allows the 2870 to operate with IBM System/360 processors of the Model 90 series.
- The 2870 BCU interface is modified and becomes the PSCE interface.
- The I/O interface is not changed by this feature.
- Feature logic detail is in the 2870 version 004 ALD pages.

The 2870 Model 90 series interface feature allows a processor of the IBM System/360 Model 90 series to communicate with the 2870. The 2870 is cabled to the Peripheral Storage Control Element (PSCE) of the processor (Figure 4-4). Because the BCU of the Models 65 and 75 is replaced by the PSCE in the Model 90 series, the 2870 BCU interface becomes the PSCE interface.

The 2870 communicates with the system via the PSCE. The 2870 recognizes the PSCE as a processor, but the timing of 2870 main storage

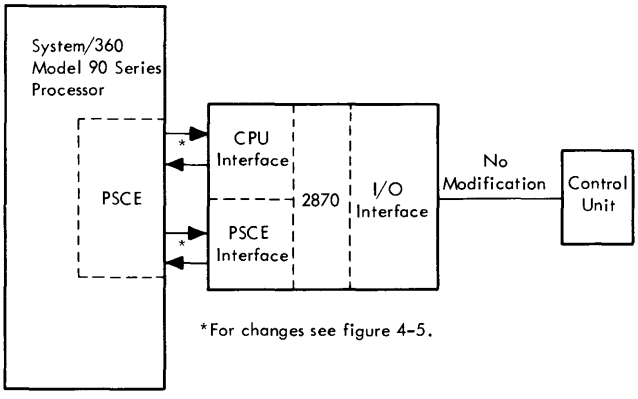


Figure 4-4. Model 90 Interface Features

operations is changed. There are no facilities for off-line testing of the 2870 Model 90 series interface feature. No alteration of the CE or manual controls occurs when this feature is installed.

System Interface

The system interface consists of the CPU and PSCE interfaces. When the 2870 operates with a processor of the Model 90 series, neither the FLT or LCS operations are performed. The FLT and LCS control lines, therefore, are deleted from the CPU interface. Also, the operational in and test light lines are not used. On the PSCE interface, CDA priority is not used, and the function and timing of some of the main storage communication lines is changed. Details of these changes can be found in the Functional Units section.

I/O Interface

The 2870 channel-to-control unit I/O interface is not modified in any way by the Model 90 series interface feature. Channel operations over the I/O interface are not affected and the attached control units are not aware of the existence of this feature.

Functional Units

The CPU and PSCE interfaces are the functional units of this feature (Figure 4-5). Descriptions of lines not mentioned in this section are in Chapter 2 of this manual.

CPU Interface

The CPU interface and its associated controls is classified in three groups: operation lines, diagnostic lines, and FLT controls.

Operational Lines: Two operational lines (operational in and test light) are deleted from the CPU interface. The other operational lines are used as defined in Chapter 2 of this manual.

Diagnostic Lines: The diagnostic lines are not changed. The diagnostic lines are defined in Chapter 2 of this manual.

FLT Controls: FLT control lines are not used when the 2870 is attached to a Model 90 series CPU.

PSCE Interface

The PSCE interface replaces the BCU interface when the 2870 is attached to a CPU of the Model 90 series. The following lines are changed:

SSC in Operation: This simplex line from the 2870 to the PSCE is active when one of the SSCs is operating. This line becomes active during the initial selection of an I/O device, and remains active until CPU accepts the terminating interrupt for the device. This line is generated by ORing the SSC busy lines.

BCU Data Request: This signal is not sent by the PSCE. The 2870 uses the BCU response signal (delayed by approximately 150 ns) to generate the BCU data request line. The function of BCU data request is not changed.

Set LCS Priority: This line is deleted from the interface.

LCS Priority: This line is deleted from the interface.

LCS Advance Pulse: This line is deleted from the interface.

Advance Pulse: Advance is a simplex pulse that the PSCE sends to the 2870. The duration and timing of the advance pulse are described in Principles of Operation section.

CDA Priority: This line is deleted from the interface.

Principles of Operation

The 2870 Model 90 interface feature allows the 2870 to communicate with a processor of the Model 90 series via the PSCE unit of the processor. Because the PSCE does not handle main storage operations in the same manner as a Model 75 BCU, 2870s main storage operations are altered.

Storage Operations

When operating with the PSCE, the 2870 main storage operations (store or fetch) has the timings

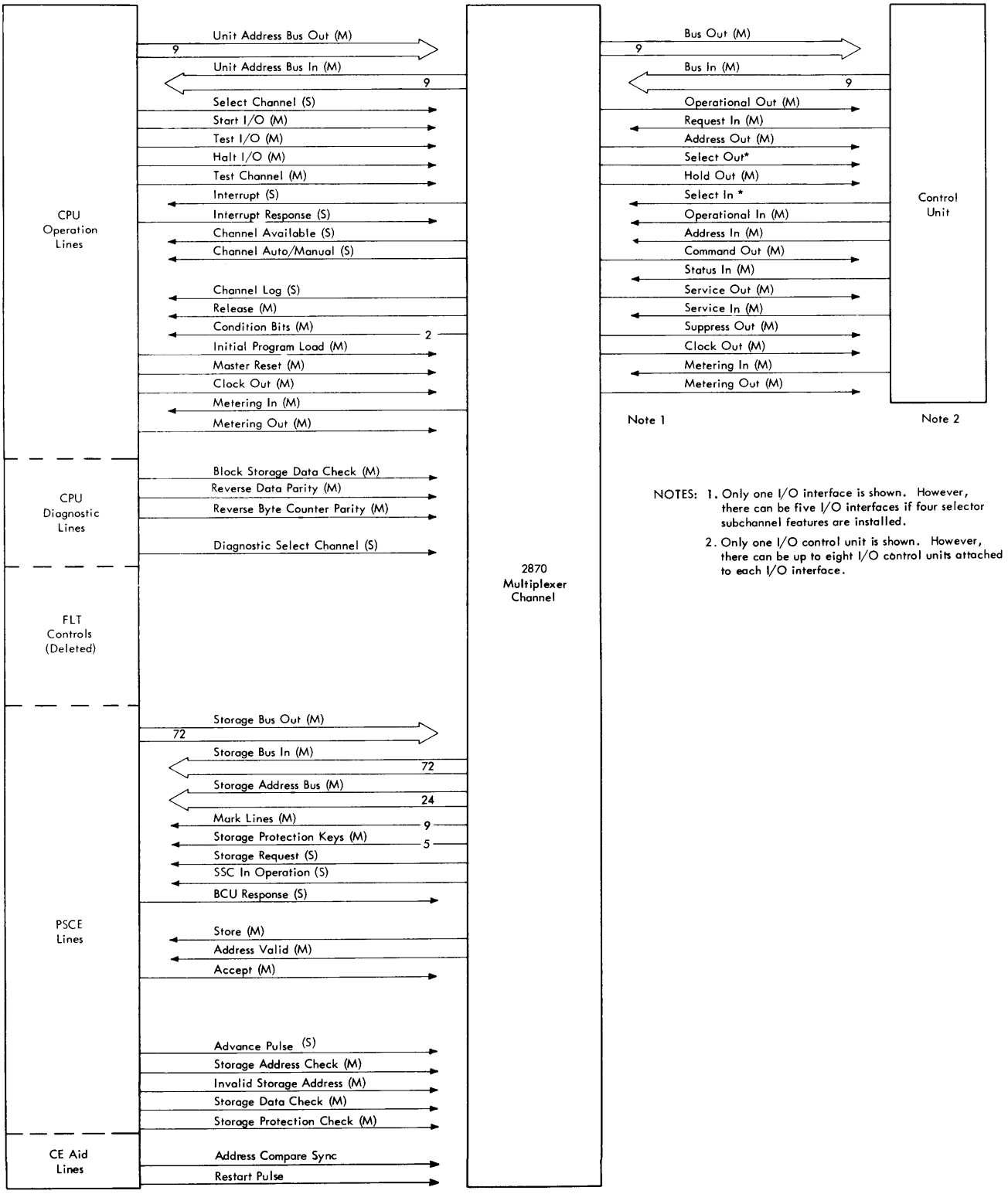
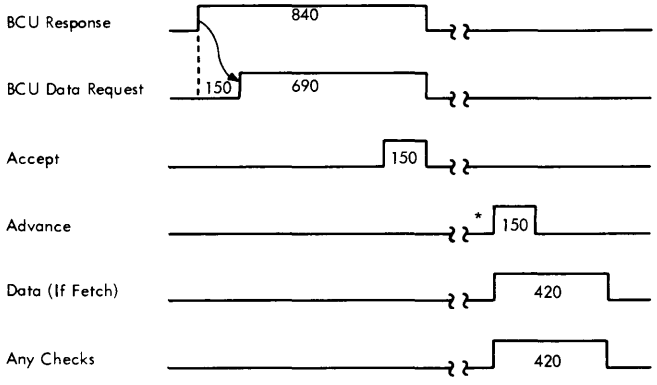


Figure 4-5. 2870-Model 90 Interface Lines

shown in Figure 4-6. These operations differ from Model 65 or 75 operations as follows:

1. BCU response, the data (for a data fetch), and any check indications are all active for a longer time.
2. BCU response is delayed (by the 2870) and used to generate BCU data request.
3. 'Accept' rises earlier in the cycle and falls with BCU response.
4. Data and any check indications rise with the advance pulse.

These timing differences require changes in the adjustment of several singleshots in the 2870. For these adjustments, see the 2870 maintenance manual.



* Variable - dependent upon storage conflicts in the PSCE.

NOTE: The values given are approximate, in nanoseconds, and may change due to engineering changes. For accurate timings see the latest maintenance manual.

Figure 4-6. 2870-Model 90 Storage Cycle Timing

FLT Operation

FLT operations are not performed when the 2870 is attached to the PSCE.

LCS Operations

Because the PSCE does not identify which main storage area from which the channel is storing or fetching data, the LCS control lines are not used.

MODEL 85 ATTACHMENT FEATURE (VERSION 008)

- Allows the 2870 to communicate with the Channel Adapter (CAD).
- Allows 2870 to operate with IBM System/360 processor of Model 85 series.
- Enables a second 2870 Multiplexer Channel (not exceeding seven channels) to be attached.
- Does not alter operation of 2870.
- Feature logic detail is found in version 008 ALD.

Description

The 2870/Model 85 Attachment Feature allows communication with the Channel Adapter. The CAD interfaces the System/360 Model 85 CPU/SCU to the 2870 Multiplexer Channel, thus allowing use of the 2870 with System/360 Model 85. Operation of the 2870 is not affected by this feature. Installation of this feature allows a second 2870 Multiplexer Channel (not to exceed seven channels) to be attached to interface. However, the priority assigned to this additional channel must be third or fourth in the priority sequence.

There are no facilities for off-line testing of the Model 85 Attachment Feature. No alteration of the CE or manual controls occurs when this feature is installed.

General Characteristics

The 2870 basic CPU and BCU interface lines remain essentially the same except that three new functional lines are added; they are 'force instruction sequence', 'hang detect', and 'selective channel reset'. The timing of some signals is changed, and certain interface lines, such as the FLT and LCS control lines, are not used. Except for the minor modifications mentioned, the operating characteristics and capabilities of the basic channel are not changed and the basic date rate of the 2870 remains the same. The active-state polarity of signals in the channel's BCU-CPU interface is positive. Channel logic for the Model 85 modification is shown on the 2870 Version 008 ALD's. In addition, the modifications required for the Model 85 version are described in the following paragraphs.

CPU Interface Lines

Modification of the Model 85 CPU to 2870 interface is as follows: The unused CPU function lines are 'channel auto/manual', 'channel log', 'test light', and 'FLT controls'.

New CPU Lines are as follows:

'Force instruction sequence' is a multiplex line added to the basic 2870 CPU interface from the channel adapter. The 'force instruction sequence' signal is a 200-ns pulse which is raised approximately 3 ms after the 'select channel' or 'interrupt response' lines rise. When activated, the signal line blocks the 'request in' signals that may be present on the multiplex interface, thus enabling CPU instructions or I/O interrupts to have priority over any data requests.

'Hang detect' is a multiplex line that becomes activated 6 ms after a 'CPU select channel' or 'interrupt response' signal has been issued and no release function occurs. Upon receipt of the 'hang detect' signal from CAD, the 2870 determines the particular time that an operation will be terminated, as follows:

1. If an operation or instruction has not reached the I/O interface, a logout, a CSW store, and a machine reset operation will be attempted.

2. If an operation or instruction has reached the I/O interface, a selective reset, a logout, and a CSW store will be attempted.

'Selective channel reset' is a simplex line from the CAD to the 2870; it carries a pulse of 200-ns duration. When the 2870 receives the signal, the channel performs a machine-reset operation to reset the channel registers, triggers, and latches. In addition, the channel performs a selective reset operation if operating with an attached I/O device. The selective-reset operation causes the control line to disconnect from the I/O interface and perform a reset operation.

BCU Interface Lines

Modification of the Model 85 BCU to 2870 interface is as follows:

Unused BCU storage function lines include LCS controls and CDA priority.

Storage Bus Out consists of 72 multiplex lines (64 data, 8 parity) from the channel adapter to the channel's BCU interface. The SBO signals rise 100 ns after the rise of the 'BCU advance' signal and after the 'BCU response' and 'accept' signals have dropped. The SBO signals will remain valid until 450 ± 25 ns after the rise of the 'BCU advance pulse' signal (timing change in basic 2870 interface signals).

'BCU advance pulse' is a simplex line from the channel adapter to the channel. The signal rises coincident with the data signals on the SBO lines or coincident with a check signal ('storage address check', 'invalid address check', 'storage data check', or 'storage protection check'). The 'BCU advance pulse' signal duration is 200 ± 20 ns. (The basic 2870 line is changed from multiplex to simplex, and the signal timing is changed.)

'Storage address check' is a multiplex line to the channel's BCU interface; it indicates a parity error was detected in the SAB bits, storage protect key bits, or mark bits. The 'storage address check' signal rises coincident with the rise of the 'BCU advance pulse'. The signal remains active until 450 ± 25 ns after the rise of the 'BCU advance pulse' signal (timing change in basic 2870 BCU interface signal).

'Invalid storage address' is a multiplex line to the channel's BCU; it is activated when the address on the SAB refers to a nonexistent storage location. The signal rises coincident with the rise of the 'BCU advance pulse' signal. The signal remains active until 450 ± 25 ns after the rise of the 'BCU advance pulse' signal (timing change in the basic 2870 BCU interface signal).

'Storage data check' is a multiplex line to the channel's BCU interface. The 'storage data check' signal is activated when a data parity error is detected in information sent to main storage on a store operation or in information coming from main storage on a fetch operation. The signal rises coincident with the rise of the 'BCU advance pulse' signal. The signal remains active until 450 ± 25 ns after the rise of the 'BCU advance pulse' signal (timing change in the basic 2870 BCU interface signal).

'Storage protection check' is a multiplex line to the channel's BCU interface. The signal indicates that an attempt was made by the channel to access a protected storage area with an improper storage protect key. The signal rises coincident with the rise of the 'BCU advance pulse' signal. The signal remains active until 450 ± 25 ns after the rise of the 'BCU advance pulse' signal (timing change in the basic 2870 BCU interface signal).

Physical Characteristics

The Model 85 feature is an integral part of the 2870 Multiplexer Channel logic, hardware, and cabling. The feature is physically located on a logic gate of the 2870 and conforms to the power requirements, environmental limits, installation planning, and other criteria required by the 2870 Multiplexer Channel.

MODEL 165 ATTACHMENT FEATURE

- Allows 2870 to communicate with Model 165 Storage Control Unit (SCU).
- Does not alter operation of the 2870.
- Feature is only added to 2870's having serial numbers 70, 000 and above.
- Feature logic detail is found in version - ALD.

Description

The 2870/Model 165 Attachment Feature allows communication with the Model 165 Storage Control

Unit (SCU), thus allowing use of the 2870 Multiplexer Channel with the 165. The hardware associated with this feature is physically an indistinguishable part of the 2870 and does not affect its operation. There are no off-line facilities for testing the Model 165 Attachment Feature. No alterations of the CE or manual controls occur when this feature is installed.

General Characteristics

The 2870 Multiplexer Channel's I/O interface remains unchanged by this feature. The SCU/CPU interface performs the same function as the BCU/CPU interface except for the differences listed below:

1. FLT circuits are not used when attached to the Model 165.

2. Twenty-two new functional lines have been added.

3. The following lines are no longer applicable to the 2870 when the Model 165 attachment feature is installed: 'LCS priority,' BCU, data request', 'TIC pulse', 'interrupt response' (simplex), 'FLT data check', 'stop FLT', 'Start FLT', 'LCS advance pulse', 'LCS priority set', 'advance pulse' (multiplex), 'accept', 'CPU start I/O', 'CPU test I/O', 'CPU halt I/O', 'CPU test channel', 'IPL channel', 'CDA priority', 'GAP pulse', 'FLT control check', and 'FLT mode'.

The active-state polarity of signals between the 2870, Model 165 SCU, and CPU is positive. A description of the new CPU interface lines is presented in the following paragraphs.

New CPU Interface Lines

'Interrupt response multiplex': A single multiplex line routed from the CPU to all channels; when activated, allows a channel to store its channel status word (CSW). The signal is generated at least 150 ns before the 'select channel' signal is issued.

'CPU control transmit': A single multiplex line routed from the CPU to all channels; when activated, signals the 2870 that a control function exists in the CPU control bus in encoded form. The line becomes active coincident with the use of the 'select channel' signal and remains in this state (minimum of 100 ns) until the fall of the 'select channel' signal. The 'CPU control transmit' signal is recognized only by the channel being selected by the CPU.

'Channel instruction bus': Consists of five multiplex lines (four data, one parity); when activated, determine the type of CPU instruction to be performed. The lines are labeled as follows: CHIB bit 0 - CHIB bit 1, CHIB bit 2, CHIB bit 3, and CHIB bit parity. These lines are activated by the CPU and are sent concurrently to all channels. The lines are made active at least 150 ns before the 'select channel' signal is issued and remain in this state for no less than 50 ns after the 'select channel' signal has dropped.

The I/O instructions that are determined by the channel instruction bus are presented in Table 4-1.

Table 4-1. Channel Bus Instructions

Bit P	Bit 0	Bit 1	Bit 2	Bit 3	I/O Instruction
0	0	0	1	0	IPL
0	0	1	0	0	Start I/O
1	0	1	0	1	Test I/O
1	0	1	1	0	Halt I/O
0	0	1	1	1	Test Channel
0	1	1	1	0	*Halt Device
1	1	1	0	0	*Fast Start I/O
1	1	1	1	1	*Store Channel ID

*Indicates new CPU instructions

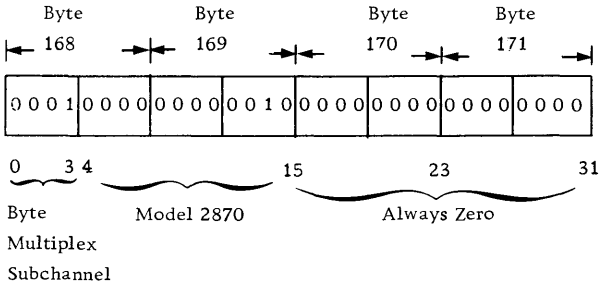
The three new I/O instructions cited in Table 4-1 are decoded by the 2870 Multiplexer Channel as follows:

Halt Device is decoded as a Halt I/O instruction. Fast Start I/O is decoded as a Start I/O instruction. The Store Channel ID instruction is initiated by the CPU by placing the proper code on the CHIB bus and signaling the channel on the 'select channel' line. This particular instruction does not require the eight-bit unit address. Its function is to cause the channel type and model-dependent information to be stored in byte locations 168 and 169 respectively, storing 0's in byte locations 170 and 171. Listed below are designations, in hex, of the fields to be stored in byte locations 168 and 169.

Bits 0-3	Type
0 (hex)	Selector Channel
1 (hex)	Byte Multiplex
2 (hex)	Block Multiplex

Bits 4-15	Channel Model
000 (hex)	Determined by CPU Model
001 (hex)	2860
002 (hex)	2870
003 (hex)	2880

Assume a query being made by the CPU to determine what type of channel and model it is communicating with. The CPU initiates a Store Channel ID instruction; the channel responds, identifying itself by storing its ID in byte locations 168-171 as follows:



Condition Codes

The condition codes relating to the Store Channel ID instruction are listed below.

CC	Function
00	Channel ID has been stored successfully.
01	Channel detected an error condition during execution instruction. A two-byte CSW will be stored, and a channel control check will be indicated.
02	Current actively on the 2870 I/O interface prevents instruction from being executed.
03	Channel not available.

CPU Control Bus

The CPU control bus consists of three multiplex lines: 'control bus bit 0', 'control bus bit 1', and 'control bus bit 2'. When activated, they represent (in encoded form) the control functions that can be performed by the 2870. The control function lines are activated by the CPU and are routed concurrently to all channels. The lines are made active at least 80 ns before issuance of the 'CPU control transmit' signal and remain in this state for 80 ns after its fall. The CPU control bus control functions are encoded as follows:

Control Bus			
Bit 0	Bit 1	Bit 2	Control Function
0	0	0	Reserved
0	0	1	Spare
0	1	0	Time Out 1
0	1	1	Time Out 2
1	0	0	Selective Reset
1	0	1	Spare
1	1	0	Unit Address Invalid
1	1	1	Spare

The 2870 executes the following sequences when the aforementioned control functions, issued by the CPU, are decoded in the CPU Control Bus.

1. Time Out 1: Blocks the 2870 from honoring another 'request in' signal on the MPLX interface, giving the CPU instruction higher priority.

2. Time Out 2: If the operation has not reached the I/O interface, a logout, CSW store, and machine reset will be attempted.

3. Selective Reset: A machine reset including all the control units attached to the 2870 interface.

4. Unit Address Invalid: Not used by 2870.

SCU Storage Functional Lines

Modifications of the Model 165 SCU to 2870 lines are presented in the following paragraphs.

Storage Bus Out: Consists of 72 multiplex lines (64 data, 8 parity) from the SCU to the channel. The SBO signals rise 80 ± 20 ns after the rise of the 'advance' signal and after the 'SCU response' signal has fallen. These signals remain valid for a minimum period of 320 ns (measured at the CPU drivers).

SCU Advance Pulse: A simplex line from the SCU to the channel. The line carries a 240 ± 20-ns pulse that precedes the data to the proper channel by 80 ± 20 ns.

Storage Bus In: Consists of 72 multiplex lines (64 data, 8 parity) that transmit data from the channel to the SCU. The signals rise coincident with the rise of the 'address valid' signal and remain in this active state for 260 ± 25 ns (measured at the channel drivers).

Storage Address Bus: Consists of 24 multiplex lines (21 data and 3 parity) that transmit addresses from the channel to the SCU. These lines have the same timing as that specified for the SBI lines.

Mark Lines: Nine multiplex lines (eight data, one parity) from the channel to the SCU that have the same timing response as the SAB lines. These lines, when active, indicate which of the eight data bytes are to be stored when the channel is performing a store operation.

Protection Key Lines: Five multiplex lines (four data, one parity) from the channel to the SCU that remain active with the SAB lines. These lines carry the storage protection information.

Storage Request: A single line from the channel to the SCU that requests priority for a storage cycle. It falls when the channel receives the 'SCU response' signal.

SCU Response: A single simplex line from the SCU to the channel. It rises when the SCU grants priority to a particular channel and is requesting the address, data, marks, and keys to be gated to their respective buses.

Address Valid: A multiplex line from the channel to the SCU; indicates that the data, protection keys, marks, and address are valid on their respective buses. The signal is formed from the 'SCU response' signal, whereupon it undergoes a deskewing delay before it is sent to the SCU. The signal falls 260 ± 25 ns after the channel receives the 'SCU response' signal.

Store: A multiplex line from the channel to the SCU: indicates that the channel is performing a store operation. The signal timing is the same as that described for the SIB lines.

Storage Address Summary Check: A multiplex line from the SCU to the channel; indicates that the SCU or storage has detected a parity on the address marks or key received. The line signal has the same timing as that described for the SBO lines.

Invalid Address Check: A multiplex line from the SCU to the channel; indicates the SCU has detected a nonexistent address on the SAB lines from the channel. The line signal has the same timing as that described for the SBO lines.

Protection Check: A multiplex line from the SCU to the channel, indicating that the channel attempted to store information in a protected storage area. The pulse timing is the same as that described for the SBO lines.

Data Check: A multiplex line from the SCU to the channel; indicates a data parity error has been detected in the information sent to storage during a store operation or in information coming from storage during a fetch operation. This pulse can rise in a maximum period of 30 ns after data is present on the SBO lines.

New Control Unit Interface Line

A new line, disconnect in, provides control units with the ability to alert the system of a malfunction that is preventing the control unit from signaling properly over the I/O interface. An example of this condition may be a microcoded control unit communicating with the channel at the time a read-only storage (ROS) error is detected. Such a control unit may be unable to complete an interface sequence properly.

'Disconnect in' can be raised by a control unit only when it is connected to the channel (that is, it has 'operational in' up). When 'disconnect in' is used during a polling sequence, the control unit must ensure that the sequence has progressed at least to the point where 'address in' has been raised with the unit address on 'bus in' before raising 'disconnect in'.

The channel, in response to 'disconnect in', performs a selective reset. 'Disconnect in' must not fall before the reset nor remain up longer than 100 nanoseconds after the fall of 'operational in'.

Physical Characteristics

The Model 165 feature is an integral part of the 2870 Multiplexer Channel logic, hardware, and cabling. The feature is physically located on a logic gate of the 2870 and conforms to the power requirements, environmental limits, installation planning, and other criteria required by the 2870 Multiplexer Channel.

MODEL 195 ATTACHMENT FEATURE

- Allows the 2870 to communicate with the System/360 Model 195 Storage Control Unit (SCU).
- Does not alter the operation of the 2870.
- Feature is added only to 2870's having serial numbers 70,000 and above.
- Feature logic detail is found in version 14 ALD's.

Description

The 2870/Model 195 Attachment Feature allows communication between the storage control unit (SCU) and the central processing unit (CPU) of a System/360 Model 195 computer and the 2870 Multiplexer Channel. The hardware associated with this feature is physically an indistinguishable part of the 2870 and does not affect its operation. There are no off-line facilities for testing the Model 195 Feature. No alteration of the CE or manual controls occurs when this feature is installed.

General Characteristics

The 2870 Multiplexer Channel's I/O interface remains unchanged by this feature. The SCU/CPU interface performs the same function as the BCU/CPU interface with the exception of the differences cited below:

1. FLT circuits are not used when attached to the Model 195.

2. New functional lines have been added.

3. The following lines are no longer applicable to the 2870 when the Model 195 attachment feature is installed: 'LCS priority', 'BCU data request', 'TIC pulse', 'interrupt response' (simplex), 'FLT data check', 'stop FLT', 'start FLT', 'LCS advance pulse', 'LCS priority set', 'advance pulse' (multiplex), 'accept', 'CPU start I/O', 'CPU test I/O', 'CPU halt I/O', 'CPU test channel', 'IPL channel', 'CDA priority', 'GAP pulse', 'FLT control check', and 'FLT mode'.

The active-state polarity of signals between the 2870, Model 195 SCU, and CPU is positive. Descriptions of the new CPU interface lines are presented in the following paragraphs.

Table 4-2. Channel Bus Instructions

Bit P	Bit 0	Bit 1	Bit 2	Bit 3	I/O Instruction
0	0	0	1	0	IPL
0	0	1	0	0	Start I/O
1	0	1	0	1	Test I/O
1	0	1	1	0	Halt I/O
0	0	1	1	1	Test Channel
0	1	1	1	0	*Halt Device
1	1	1	0	0	*Fast Start I/O
1	1	1	1	1	**Store Channel ID

*Indicates new CPU instructions
**Not used in Model 195 Feature

New CPU Interface Lines

'Interrupt response multiplex' is a single multiplex line routed from the CPU to all channels; when activated, it allows a channel to store its channel status word (CSW). The signal is generated at least 130 ns before the 'select channel' signal is issued.

'Channel instruction bus' consists of five multiplex lines (four data, one parity) that when activated determine the type of CPU instruction to be performed. The lines are labeled as follows: CHIB bit 0, CHIB bit 1, CHIB bit 2, CHIB bit 3, and CHIB bit parity. These lines are activated by the CPU and are sent concurrently to all channels. The lines are made active at least 150 ns before the 'select channel' signal is issued and remain in this state for no less than 50 ns after the 'select channel' signal drops.

The I/O instructions that are determined by the Channel Instruction Bus are presented in Table 4-2.

The Halt Device instruction is decoded by the 2870 as a Halt I/O instruction; the Fast Start I/O instruction is decoded as Start I/O instruction.

SCU Storage Functional Lines

Modification of the Model 165 SCU to 2870 lines is presented in the following paragraphs.

'Storage bus out' consists of 72 multiplex lines (64 data, 8 parity) from the SCU to the channel. The SBO signals rise 54 ± 20 ns after the rise of the 'advance' signal and after the 'SCU response' signal has fallen. These signals remain vital for a minimum of 378 ns measured at the CPU drivers.

'SCU advance pulse' is a simplex line from the SCU to the channel. The line carries a 270 ± 20-ns pulse that precedes the data to the proper channel by 54 ± 20 ns.

'Storage bus in' consists of 72 multiplex lines (64 data, 8 parity) that transmit data from the channel to the SCU. The signals rise coincident with the rise of the 'address valid' signal and remain in this active state for 260 ± 25 ns, measured at the channel drivers.

'Storage address bus' consists of 24 multiplex lines (21 data and 3 parity) that transmit addresses from the channel to the SCU. These lines have the same timing as that specified for the SBI lines.

'Mark lines' are nine multiplex lines (eight data, one parity) from the channel to the SCU, having the same timing response as the SAB lines. These lines, when active, indicate which of the eight data bytes are to be stored when the channel is performing a store operation.

'Protection key lines' are five multiplex lines (four data, one parity) from the channel to the SCU; they remain active with the SAB lines. These lines carry the storage protection information.

'Storage request' is a single line from the channel to the SCU; it requests priority for a storage cycle. It falls when the channel receives the 'SCU response' signal.

'SCU response' is a single simplex line from the SCU to the channel. It rises when the SCU grants priority to a particular channel and is requesting the address, data, marks, and keys to be gated to their respective busses.

'Address valid' is a multiplex line from the channel to the SCU; it indicates that the data, protection keys, marks, and address are valid on their respective buses. The signal is formed from the 'SCU response' signal, whereupon it undergoes a deskewing delay before it is sent to the SCU. The signal falls 260 ± 25 ns after the channel receives the 'SCU response' signal.

'Store' is a multiplex line from the channel to the SCU; it indicates that the channel is performing a store operation. The signal timing is the same as that described for the SIB lines.

'Storage address summary check' is a multiplex line from the SCU to the channel; it indicates that the SCU or storage has detected a parity on the address marks or key received. The line signal has the same timing as that described for the SBO lines.

'Invalid address check' is a multiplex line from the SCU to the channel; it indicates the SCU has detected a nonexistent address on the SAB lines from the channel. The line signal has the same timing as that described for the SBO lines.

'Protection check' is a multiplex line from the SCU to the channel, indicating that the channel attempted to store information in a protected storage area. The pulse timing is the same as that described for the SBO lines.

'Data check' is a multiplex line from the SCU to the channel; it indicates that a data parity error has been detected in the information sent to storage during a store operation or in information coming from storage during a fetch operation. This pulse can be used within a maximum period of 30 ns after data is present on the SBO lines.

New Control Unit Interface Line

A new line, disconnect in, provides control units with the ability to alert the system of a malfunction that is preventing the control unit from signaling properly over the I/O interface. An example of this condition may be a microcoded control unit communicating with the channel at the time a read-only storage (ROS) error is detected. Such a control unit may be unable to complete an interface sequence properly.

'Disconnect in' can be raised by a control unit only when it is connected to the channel (that is, it has 'operational in' up). When 'disconnect in' is used during a polling sequence, the control unit must ensure that the sequence has progressed at least to the point where 'address in' has been raised with the unit address on 'bus in' before raising 'disconnect in'.

The channel, in response to 'disconnect in', performs a selective reset. 'Disconnect in' must not fall before the reset nor remain up longer than 100 nanoseconds after the fall of 'operational in'.

Physical Characteristics

The Model 195 feature is an integral part of the 2870 Multiplexer Channel logic, hardware, and cabling. The feature is physically located on a logic gate of the 2870 and conforms to the power requirements, environmental limits, installation planning, and other criteria required by the 2870 Multiplexer Channel.

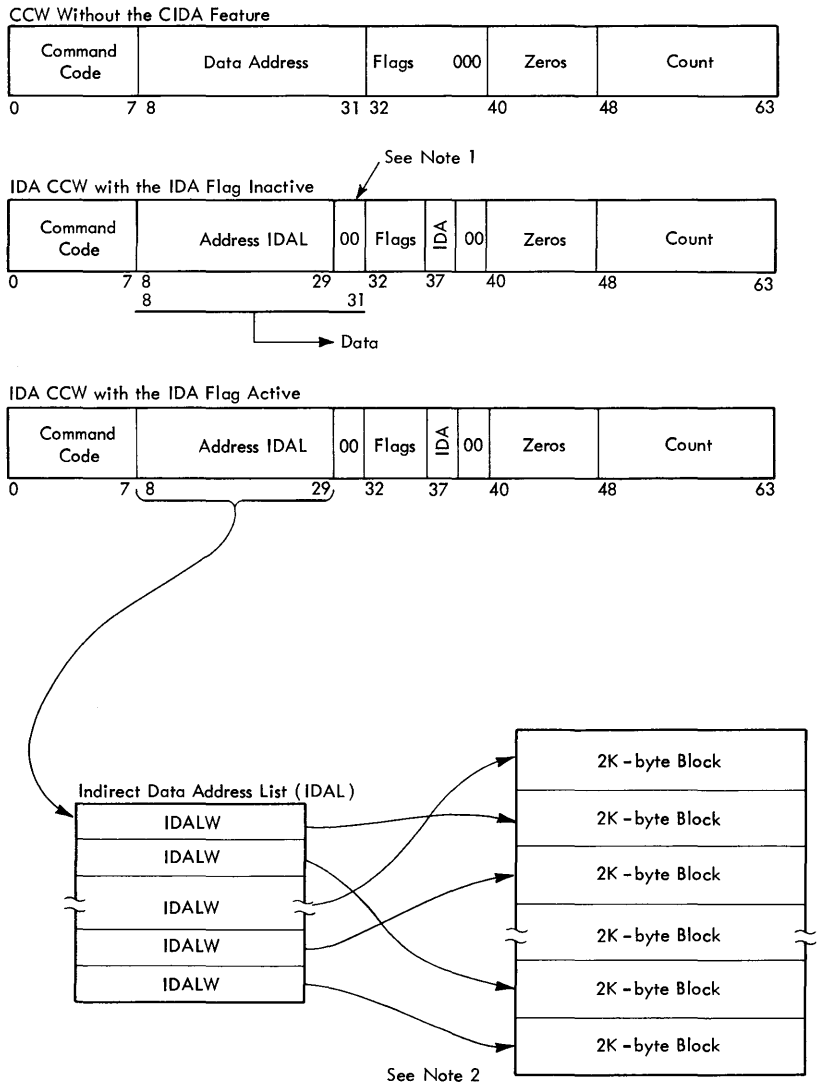
CHANNEL INDIRECT DATA ADDRESS FEATURE (CIDA)

- The CIDA feature allows the 2870B to indirectly address 2,048 (2K) byte blocks of storage.
- Channel operation is altered in both CIDA and normal mode.
- The CIDA feature can be installed on any 2870B.

Description

The CIDA feature makes the 2870B compatible with the relocate feature of the System/370 Models 165 II and 168. This is accomplished by changing the function of the data address field of the CCW.

Normally the data address field of the CCW is used to access storage for data. But with the CIDA feature installed, the channel is capable of using the data address field as a pointer (Figure 4-7) to a list of words called the IDAL (Indirect Data Address List).



Notes:
1. Bits 30 and 31 need not equal zero if the IDA flag is inactive.
2. The first IDALW of an IDAL can point to any byte of any 2K-byte block of storage. Succeeding IDALWs must point to the first or last byte (rd bkwd) of any 2K-byte storage block.

Figure 4-7. Indirect Addressing

Each word of the list contains the address of a 2K-byte block of storage. This allows the channel to indirectly address 2K-byte data blocks of storage.

The hardware associated with this feature is a physically indistinguishable part of the channel. This feature may be installed on any 2870B Multiplexer Channel.

Functional Characteristics

The functional characteristics for the System/370 2870 (2870B) Multiplexer Channel remain unchanged by the addition of the CIDA feature, with the following exceptions:

1. The CCW is modified by adding the IDA flag (bit 37).
2. The use of UCW 3 is changed.
3. A new SBO gate has been added.
4. Two bits are added to log word 3.
5. Four CE panel indicators are modified.

Indirect Data Address (IDA) Flag

Bit 37 of the CCW is the IDA flag; it previously was required to be zero (CCWs with and without the CIDA feature are shown on Figure 4-7). When the IDA flag is equal to one, bits 8-31 of the CCW specifies the address of the Indirect Data Address List (IDAL). If the IDA flag is equal to zero or the feature is not installed, bits 8-31 specify the data address.

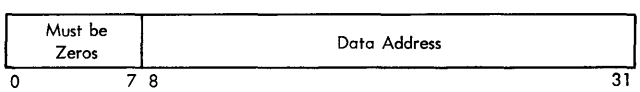
Conditions for program checks remain the same with the following exceptions.

1. Bit 37 equal to a one does not cause a program check.
2. Bits 30 and 31 of the IDAL address must equal zero or a program check occurs.

Indirect Data Address List (IDAL)

The IDAL (Figure 4-7) is a series of words (addresses) called Indirect Data Address List Words (IDALW); each word must be on a word boundary. A program check occurs and the operation is terminated if the channel attempts to fetch an IDALW that is not on a word boundary. Each IDALW addresses a 2K-byte block of data in main storage. The first word of the list is addressed by bits 8-31 of an IDA CCW; each succeeding IDALW is addressed by using the current IDALW address plus 4.

Indirect Data Address List Word (IDALW)



The IDALW is 32 bits; bits 8-31, the data address, point to a 2K-byte block of storage; bits 0-7 must equal zero or a program check occurs and the operation is terminated.

IDA Cross-gate Latch

Because the IDALWs are on word boundaries and because the 2870 Multiplexer Channel can only make doubleword fetches. a new gating line is added; this line allows SBO bits 32-63 to be cross-gated to bits 0-31 of the channel input OR. The cross-gate latch is active only for IDALW fetches with addresses on word boundaries.

Log Word 3 Additions

Two additional bits are added to log word 3; bit 36 to indicate a word 3 check, and bit 47 to indicate an IDAL word fetch was in process when an error was detected.

UCW Word 3

With the CIDA feature installed. UCW word 3 holds the address of the next IDALW (the current IDALW+4). The IDAL address (Figure 4-7) is used to fetch the first IDALW; it is updated by 4 and stored in UCW word 3 for any subsequent IDALW fetches. Subsequent IDALW fetches are necessary whenever a 2K-byte data boundary is crossed and the current CCW still has data to transfer ($Ct \neq 0$).

Previously UCW word 3 held prefetched CCWs during Multiplex Subchannel Write CDA operations. However, with the CIDA feature installed. CCWs cannot be prefetched; this is true whether or not the IDA flag is active. UCW word 3 has only one function--to hold the address of the next IDALW fetch if a fetch is required.

Parity is checked for bytes 1-3 whenever UCW word 3 is stored into local storage. Incorrect parity causes a channel-control check.

CE Panel Modification

Four CE panel indicators have been modified with the addition of the IDA feature, lamps B7. G14. F25, and F26 (see Figure 6-1A). Lamp B7 indicates the condition of the IDA flag (CCW bit 37). F25, the initial IDA lamp (IDA CCW fetch latch), indicates that the channel is fetching the first IDALW. F26, the 2K-IDA lamp, indicates that data has crossed a 2K-byte boundary and the channel is fetching the next IDALW. Lamp G14, the WD2/WD3 check, indicates that UCW WD2 or UCW WD3 has bad parity. UCW WD 3 has bad parity if lamp G14 and either F25 or F26 is on. G14 indicates UCW WD2 has bad parity if neither F25 or F26 is on.

Operational Characteristics

Functionally, channel operations remain unchanged by the addition of the CIDA feature. With or without the CIDA feature the 2870 performs I/O operations identically; the only difference is how the channel determines its data address. For channels with the CIDA feature, bit 37 of the CCW (the IDA flag) is sampled; if the IDA flag is active, an IDALW fetch is made. The IDALW supplies the data address for the I/O operation. For channels without the CIDA feature or channels with the CIDA feature and the IDA flag inactive, the data address in the CCW is used to access storage for data during I/O operations.

Data processing is the same for either channel unless a 2K-byte data boundary is crossed. If a 2K-byte boundary is crossed and the Ct≠0, an IDALW fetch is necessary to obtain the address of the next 2K block of data. If a 2K-byte boundary is reached and the Ct=0 or if the CIDA feature is not installed and the Ct=0, the channel stops data transfer and terminates normally.

Write, Read, Control, and Sense Operations

In write, read, control, and sense operations (Figure 4-8), the storage addresses used for data transfers are in ascending order. As data transfer operations proceed, the data may cross a 2K-byte block boundary (that is, bits 21-31 of the data address register change from ones to zeros). When this occurs, the next IDALW points to the first byte of the next 2K-byte block with which data transfer is to occur. The second and all subsequent IDALW data addresses must have bits 21-31 equal to zeros to be on a 2K-byte block boundary; if not, a program check occurs and the operation is terminated.

A data address program check condition causes the turn-on of UCW 0 bit 40. Because a write operation prefetches data and because a write operation can be terminated before the data is used, UCW 0 bit 38 is set for data address program checks. If the channel attempts to use the data, UCW 0 bit 38 is reset and bit 40 is set.

Read-backward Operations

Storage addressing for read-backward operations is in descending order. As data transfer operations proceed, the data may cross a 2K-byte boundary (that is, bits 21-31 of the data address register change from zeros to ones). When this occurs, the next IDALW points to the end of the next 2K-byte block with which data transfer is to occur. The second and all subsequent IDALWs must have bits 21-31 equal to ones in order to be at the end of a 2K-byte block boundary; if not, a program check occurs and the operation is terminated.

Performance Characteristics

Use of the CIDA feature will cause additional delay in the data path to the I/O device. This is due to the channel time required to perform the CIDA function and the additional storage reference required. This is true on any CCW fetch when bit 37 of the new CCW is a one or where a 2K-byte block crossing is detected in the data field. This will increase the probability of overrun (both service and command) and chaining checks.

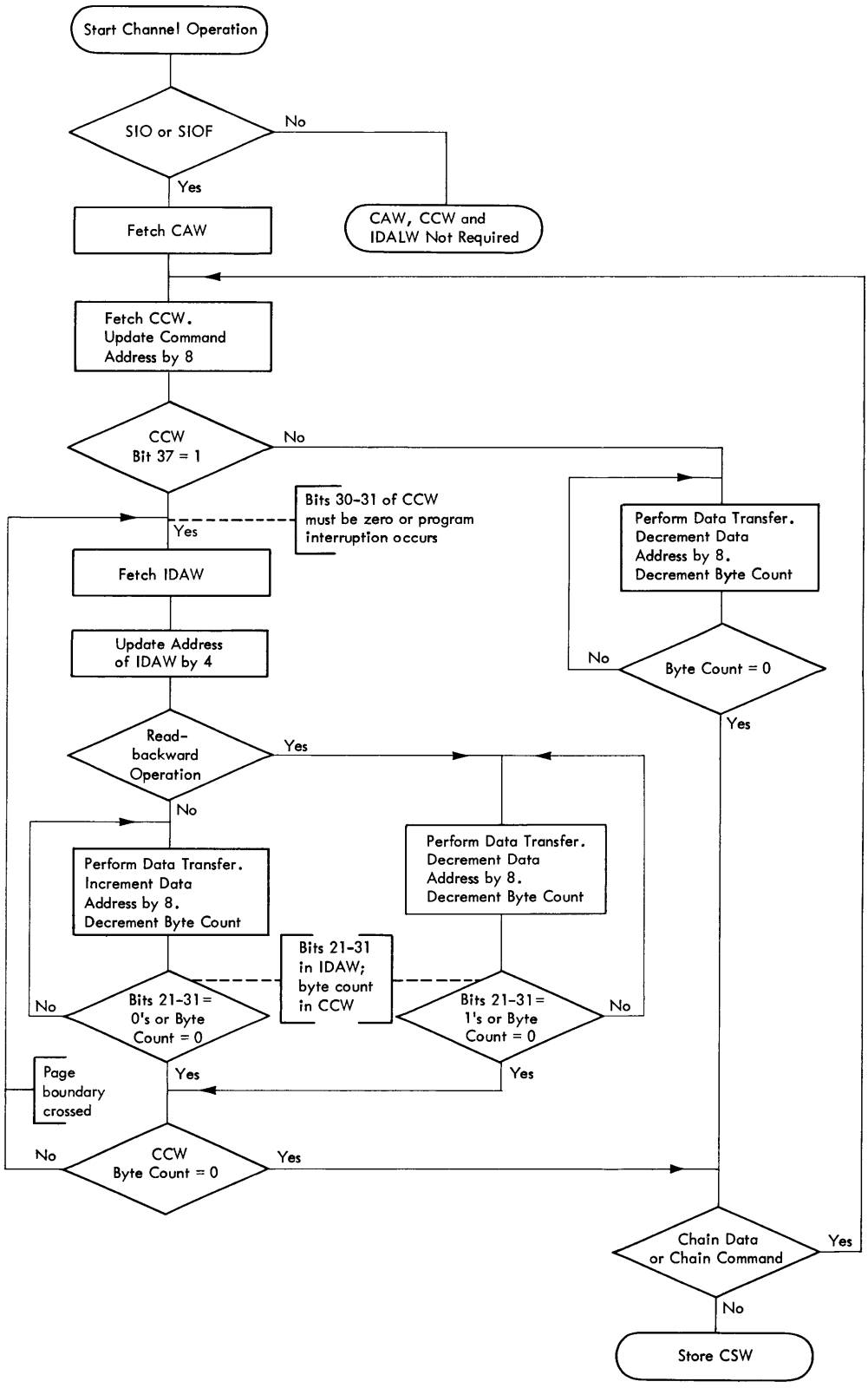


Figure 4-8. CIDA Flowchart

This chapter discusses the 2870 power supply and control, including control, power fault detection, and manual control.

POWER SUPPLY

- Requires a 208/230-v, 3-phase, 60-cycle power source.
- IBM World Trade requires 195/220/235 "delta" or 380/408 "wye", 50-cycle voltage source.
- Two duplex convenience outlets, 115 volts, for each channel frame.
- Six mid-pac regulators used to power the machine.
- A seventh regulator added for selector subchannel feature.

AC Voltage

Line voltage is connected to the 2870 via the feedthrough capacitor box and main supply disconnect circuit breaker. The input voltage is 208/230v +10%-8% (2% allowed for distribution losses within the system), 3 phase, 4 wire; the fourth wire is equipment ground.

For IBM World Trade application, the required input voltage is 195/220/235 "delta" or 380/480 "wye" +10% -8% (2% allowed for distribution losses within the system). Changing the input configuration from "delta" to "wye" and vice versa is possible in the field. In 3-phase, 5-wire "wye," the fourth wire is neutral and the fifth wire is equipment ground; ground and neutral can be jumpered where required by local regulations. A 4-wire, 3-phase "delta" source is used where required; the fourth wire is equipment ground.

Convenience Outlet

Two 115v ac duplex convenience outlets are provided. This power is available as long as the main circuit breaker of the channel is on. Maximum current per outlet is 20 amp, and the maximum total current for all outlets is 20 amp. The outlets are protected by a 10 amp fuse, for 60 cycles, in the primary of the convenience outlet transformer.

DC Voltage

The 2870 has six mid-pac regulator power supplies, to develop +6v @ 16 amp, -8.5/-10.5v @ 14 amp, +6vM @ 40 amp, +3v @ 45 amp, -3v @ 20 amp, -15v @ 1.5 amp, or +3v @ 30 amp. The seventh regulator, +3v @ 30 amp, is added with the installation of the first selector subchannel feature.

Blowers

Two single-phase blowers are located below the regulators in the power supply compartment, and in each of the three channel gates. These blowers are on only when power is up on the channel. The channel gate blowers are individually protected by 0.65 amp, two-pole breakers.

Overvoltage Protection

Overvoltage protection is provided in the mid-pac regulators by individual overvoltage cards. These overvoltage cards shut off the regulators if the output voltage exceeds a predetermined value. The protection is accomplished by gating on a silicon rectifier that provides a short across the output of the regulator, causing the regulator circuit breaker to trip. This interruption of the regulator output causes remaining power on the channel to be sequenced down.

Voltage Sequence Controller

When the 8.5/10.5v level gets to approximately 7.0v on powering up, TR10 is turned on. This causes SCR 5 to be gated on, resulting in K17 being energized. The normally open points of K17 now close, and K27 is held through normally open points instead of normally closed points of K17. Normally open points of K17 connected to K29 are also closed. When 8.5/10.5v level drops to 6.0 to 7.0v, TR3 is turned on. With TR3 on, SCR 2 is gated on, resulting in K21 being energized. Then a normally closed point of K21 that is in series with K28 opens; this controls the -15v level.

TR5 is turned on when the 8.5/10.5v level drops to 0-25% of 9v. With TR5 on, SCR 3 is gated on, resulting in K22 being energized. A normally closed point of K22, in series with K27, then opens. Also a normally closed point of K22, in series with

the -20v source opens, providing an automatic reset. When the -15v level gets to 75-100%, TR8 is turned on. With TR8 on, the SCR 4 is gated on, resulting in K19 being energized. Normally open points of K19 then transfer. The normally closed points of K19 in the K29 circuit are open. If the -15v level drops to 0-25%, TR1 turns on. When TR1 is turned on, then SCR1 is gated on, resulting in K20 being energized.

Sequencing Power Up

1. With power connected, the 24v dc power supply is energized through F1 and F2.
2. With the emergency power off (EPO) contactor K26 pick circuit completed between A and B, EPO control contactor K26 is picked. The thermal sense control relay is picked through the normally closed points of K8. After picking, K9 is then held through its own points.
3. The sense power source, +20v, common, and -20v, is brought up when 28v ac relay K30 is energized.
4. The convenience outlet transformer T3 is now energized.
5. The dc power may now be brought up either locally at the 2870 or remotely from the CPU. To bring the power up locally, position the local/remote switch to LOCAL and depress the power-on switch on the CE console. Power is brought up remotely by positioning the local/remote switch to REMOTE. Then power can be shunted through J44 pin D from the CPU.
6. When dc power is brought up, K27, which controls the logic levels, is energized through the normally closed points of K17 and K22. Once the logic levels are all up to 75-100% of their nominal values, K1 and K2 in the voltage sense unit transfers, allowing K29, which controls the 8.5/10.5v level, to be energized through normally closed points of K19 and K20.
7. The sequencing control unit picks K17, which in turn energizes K28, when the 8.5/10.5v level is up to 75-100% of 9v. K28, which controls the -15v levels, was energized through normally closed points of K21 and K20.
8. K27 is now held energized through the normally open points of K17 and the normally closed points of K22.
9. K29 is now held energized through the normally open points of K17 and the normally closed points of K20.
10. When the -15v supply is up to 75% or more of its nominal value, the voltage sequencing unit picks K19, which holds power on.
11. K19 transfers, allowing the stepping switch to move off start position and advance through the points of the I/O adapter relays.
12. K10-K16, which control the power on/off of the I/O equipment, are energized when K19 is transferred. Also, when K19 is picked, power-on reset is shifted from ground to +3v. Sequencing power up is completed.

Voltage Sequencing Down

1. Power can be sequenced down from either the CPU or the 2870 CE console by positioning the local/remote switch. In the local position, power may be sequenced down only by the power-off switch on the multiplexer control panel. If, however, the local/remote switch is in the remote position, power can be sequenced down from either the CPU or the 2870 control panel.
2. When power down is initiated, voltage to K28, which controls the -15v level, is interrupted. Once the -15v level drops to 0-25% of 15v, K20 is energized in the sequencing control unit. The normally open points of K20 close, shifting power levels to ground. The K20 normally closed points that control K28 (-15) and K29 (8.5/10.5) are now opened. The -15v level is already down, so the 8.5/10.5v level starts down. When it drops to 6v, K21 in the sequence control unit is energized.
3. The normally closed point in the control circuit of K28 is then opened. This is to ensure that the -15v level is down. Then, when the 8.5/10.5v level drops to 0-25% of 9v, K22 of the sequence control unit is energized. The K22 normally closed points then open, interrupting the voltage to K27, which controls the logic levels.
4. The K22 normally closed points interrupt the 20v supply, which, in turn, resets K17-K19. However, K22 is delayed on dropout to ensure the resetting of the other control relays. When K19 is reset, 24v are applied to the stepping switch through K19 normally closed points; this returns the stepping switch to the start position. The dc power is now completely down.

Remote Voltage Sensing

All mid-pac regulators used in the 2870 are equipped for either remote or local voltage sensing. Voltage levels that will experience appreciable distribution losses are remotely sensed to compensate for these losses.

SECTION 1. CE CONSOLE (SERIAL NO. 60,001 AND 70,000 AND ABOVE)

MANUAL CONTROLS AND INDICATORS

- The channel has a CE console with manual controls and indicators for channel test or control.
- The channel has a power control panel for controlling and regulating power.

The CE console indicators and switches are arranged in horizontal rows. These rows of indicators or switches are labeled A-M from top to bottom. Rows A-J are indicators and rows K-M are switches. The indicators and switches are numbered vertically 1-36 from left to right. Indicators and switches are referenced by alphameric grid coordinates on the CE console (Figure 6-1).

The power control panel contains switches and jacks for controlling and regulating power, and a meter for recording channel running time.

CE Console Indicators

Registers, error conditions, important triggers, and most of the I/O interface lines are indicated on the CE console. The indicators in rows A and B represent the control register fields and are arranged as the fields occur in the control register. Rows C-G are main channel and multiplex subchannel indicators. Rows H and J are selector subchannel indicators for a particular subchannel, as selected by the SSC display switches (unit address switches 2 and 3) except when a SSC log-on-machine check is in process at which time rows H and J display the SSC being logged.

Control Register (A-B): The control register (64 data bits plus eight parity bits) is divided into fields to represents a CAW, or CSW (UCW 0, UCW 2, or UCW 3). The control register is also used to display UCW 1 on a manual local storage fetch. Unless a reset occurs, the register contains the last operation performed. A master reset clears the register and sets the parity bits.

MPX Simulate I/O Register (C1-9): This is a data register (eight bits plus parity) used in simulate I/O operations for the multiplex interface. The register is loaded by a write operation. Data is obtained from this register during a read operation. Machine reset does not affect the contents of this register.

SSC Simulate I/O Register (C10-18): This is a data register (eight bits plus parity) used in simulate I/O operations for any selector subchannel interface. The register is loaded by a write operation. Data is obtained from this register during a read operation. Machine reset does not affect the contents of this register.

Command Register (C19-27): The command byte (eight bits plus parity) is stored in this register during a multiplex start I/O CCW fetch. A master reset, or a multiplex start I/O CCW fetch changes the contents of this register.

MPX CC Command Register (C28-36): The command byte (eight bits plus parity) is stored in this register during a multiplex chain command CCW fetch. Note: The command register may also contain a command. Master reset, or multiplex chain command CCW fetch changes the contents of this register.

Logout Register (D1-9): The address (eight bits plus parity) for the subchannel that has an outstanding log interrupt request is stored in this register. Master reset, or a log-in-2 sequence changes the contents of this register.

Interrupt Queue Register (D10-18): This eight-bit plus parity register holds the address of the subchannel that has an outstanding interrupt request (interrupt buffer full trigger on). This register is used for multiplex subchannel interrupts and selector subchannel PCI interrupts. Master reset, diagnostic test local store, or the setting of interrupt buffer full changes the contents of this register.

Initial UA Register (D19-27): This register contains the address (eight bits plus parity) of the device for an initial selection. It is loaded from the CPU interface via UABO. It is also loaded from the unit address OR on a pseudo test I/O. Master reset clears this register and sets the parity bit.

MPX UA Register (D28-36): This eight-bit plus parity register is set from the initial unit address register during a multiplex initial selection sequence, or from the address on bus in presented (by a control unit) during a device service request sequence. Master reset clears this register and sets the parity bit.

Unit Address OR (E1-9): This eight-bit plus parity OR displays the device address for which the main

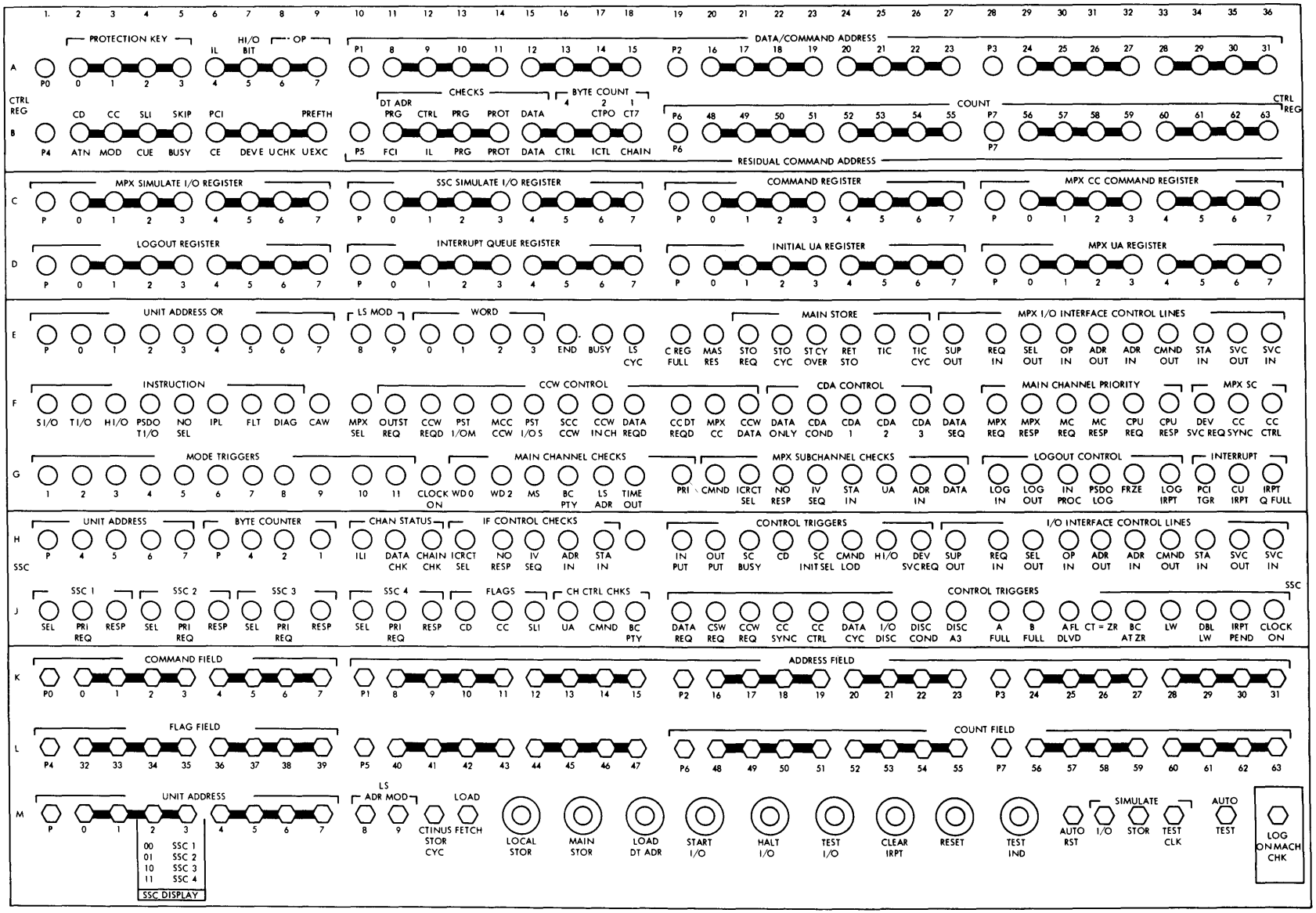


Figure 6-1. CE Console (Serial No. 60,001 and 70,000 and above)

channel sequence is active. The address presented to local storage is obtained from this OR.

LS Mod (E10-11): These two bits represent a decode of one of the four local storage words for the device address indicated by the unit address OR. The contents of this register represent the word fetched or stored on the last local storage operation.

Word 0 (E12): Word 0 is fetched for the device displayed in the unit address OR.

Word 1 (E13): Word 1 is fetched for the device displayed in the unit address OR. Word 1 control is also used during a master reset or test local storage operation.

Word 2 (E14): Word 2 is fetched for the device displayed in the unit address OR.

Word 3 (E15): Word 3 is fetched for the device displayed in the unit address OR.

End (E16): 'End' is turned on to complete a main channel sequence. This turns off 'busy' when main channel operations are completed. The release of the priority circuits resets this trigger.

Busy (E17): 'Busy' is set by priority circuits at beginning of a main channel sequence and remains on until 'end' turns it off.

LS Cycle (E18): A local storage fetch or store cycle is in progress.

C Reg Full (E19): A local store fetch to the control register is completed. It is reset at the end of the main channel sequence.

Mas Res (E20): Master reset trigger is turned on at the completion of a 6 usec master reset. This trigger causes the clearing of local storage data and insertion of correct parity. It is reset by a 2 usec reset pulse after local storage is cleared.

Main Storage Indicators

Sto Req (E21): A storage request is outstanding to the BCU.

Stor Cyc (E22): A storage cycle with the BCU is in progress.

ST Cy Over (E23): A storage cycle is completed. This trigger is reset at the end of the main channel sequence.

Ret Sto (E24): 'Retain storage' causes main channel to perform two main storage fetches.

TIC (E25): A TIC command is decoded on a CCW fetch. It is reset during the TIC cycle sequence.

TIC Cycle (E26): This trigger controls the main channel update of the command address and the fetch of the new CCW. It is reset at completion of the CCW fetch cycle.

Multiplex Subchannel I/O Interface Control Lines

Sup Out (E27): Monitors the suppress out line.

Req In (E28): Monitors the request in line.

Sel Out (E29): Monitors the select out line.

Op In (E30): Monitors the operational in line.

Adr Out (E31): Monitors the address out line.

Adr In (E32): Monitors the address in line.

Cmnd Out (E33): Monitors the command out line.

Sta In (E34): Monitors the status in line.

Svc Out (E35): Monitors the service out line.

Svc In (E36): Monitors the service in line.

Instructions

S I/O (F1): The start I/O latch is set during a CAW fetch. It is reset when CPU drops the select channel line.

T I/O (F2): A main channel test I/O sequence is in progress. Note: The CPU may or may not be released at this time.

H I/O (F3): A main channel halt I/O sequence is in progress. Note: The CPU may or may not be released at this time.

Psdo T I/O (F4): This trigger is turned on to clear a control unit interrupt during CPU priority response, causing a test I/O to be executed to clear the device status. This trigger remains on until the CPU is released.

No Sel (F5): A select-in was received during an initial selection sequence. It is reset with the next main channel priority request or CPU priority request.

IPL (F6): The channel is performing an initial program load sequence. This latch is reset when CPU is released.

FLT (F7): An FLT operation is in progress with a selector subchannel.

Diag (F8): The diagnose line is active from CPU. This causes channel to operate in the simulate I/O mode.

CAW (F9): A CAW is being fetched for a start I/O instruction. This latch is reset at the completion of the CAW fetch.

MPX SEL (F10): A multiplex subchannel initial selection is to be executed. This latch is reset when the CPU is released.

CCW Control

Outst Req (F11): The outstanding request trigger is set to allow a subchannel priority request to interrupt a CCW fetch or a multiplex subchannel write data fetch during the start I/O sequence. This latch is reset at the end of the main channel sequence which interrupted the start I/O.

CCW Reqd (F12): CCW required fetches a CCW for start I/O operation. This latch is reset at the end of the CCW fetch.

PST I/O MPX (F13): The multiplex pseudo start I/O trigger causes a CCW to be fetched for a multiplex subchannel chain command operation. Pseudo start I/O has priority over a start I/O operation. This latch is reset at the end of the main channel response for the CCW fetch.

MPX CC CCW (F14): The multiplex chain command CCW trigger causes a CCW to be fetched during the main channel response sequence for the multiplex pseudo start I/O. This latch is reset at the completion of the CCW fetch.

PST I/O SSC (F15): Pseudo start I/O selector subchannel executes a chain command operation for a selector subchannel. The entire operation is performed under one SSC response. This latch is reset at the completion of the CCW in channel sequence.

SSC CC CCW (F16): Selector subchannel chain command CCW latch causes a CCW to be fetched for a SSC pseudo start I/O sequence. This latch is reset at the completion of the CCW fetch.

CCW In Chan (F17): A CCW fetch is completed for a start I/O or a chain command operation. This latch is reset at the end of the main channel sequence.

Data Reqd (F18): This latch is turned on if a multiplex subchannel write data fetch during a start I/O operation is interrupted by an outstanding request. The write data is fetched when main channel again receives priority. This latch is reset at the completion of the main channel sequence that fetches the write data.

CC DT Reqd (F19): This latch is set if a chain command multiplex write data fetch is interrupted by a subchannel priority request, causing data to be fetched during the next main channel response. This latch is reset at the completion of the data fetch sequence.

MPX CC (F20): Multiplex chain command sequence is set by trigger 9. This latch is reset at the end of the sequence.

CCW Data (F21): This SSC write CDA control latch is set during a trigger 1 sequence. CCW data sets the data only latch at the completion of the CCW fetch during the trigger 3 sequence. This latch is reset by the turn-on of the data only latch.

Data Only (F22): The data only latch is set by the CCW data latch or by SSC write CDA with a prefetched CCW. This latch causes a double word of data to be fetched using the new CCW's data address field. This latch is reset during the CDA sequence.

CDA Cond (F23): Indicates that a CDA sequence is being performed. This latch is reset when the data only latch turns on trigger 1, or at the end of the CDA sequence.

CDA 1 (F24): CDA 1 is set during multiplex CDA operation with count equal to 1, and no CCW prefetched. CDA 1 is reset at the completion of the CDA operation.

CDA 2 (F25): A multiplex CDA operation is in progress for a prefetched CCW (local storage UCW 3). This latch is reset at the completion of the CDA operation.

Init IDA (F25): The channel is fetching the first IDALW of the IDAL. The indicator is called the IDA CCW fetch latch in the ALDs and is reset at the end of the IDALW fetch. Note: This indicator is used only with the CIDA feature. (See Figure 6-1A).

CDA 3 (F26): A multiplex write CDA CCW is being prefetched and stored in UCW 3 of local store. This latch is reset at the completion of the CDA operation.

2K IDA (F26): Data has crossed a 2K-byte boundary and the channel is fetching the next IDALW. The latch is reset at the end of the IDALW fetch. Note: This indicator is used only with the CIDA feature. (See Figure 6-1A).

Data Seq (F27): This latch is turned on during a multiplex status sequence to store data in main storage from UCW 1 of local storage. This latch is reset at the end of the status sequence.

Main Channel Priority

The request latch is reset when response is granted.

MPX Req (F28): The multiplex subchannel is requesting priority for a data or status cycle.

MPX Resp (F29): Multiplex subchannel priority response is active.

MC Req (F30): Main channel is requesting priority for a CPU instruction, multiplex subchannel chain command, a no selection, or a multiplex subchannel burst mode operation.

MC Resp (F31): Main channel response is active.

CPU Req (F32): CPU priority is active for an interrupt register full condition or a log interrupt request.

CPU Resp (F33): CPU response is active.

Multiplex Subchannel

Dev Srv Req (F34): A request-in for a data or status sequence is in progress. This latch is set by 'operational in' and 'address in' and remains set until the fall of 'operational in' and 'status in.'

CC Sync (F35): This control latch is set during a multiplex chain command sequence if device end status is present. This latch is reset prior to reselection of the device for the chain command operation.

CC Ctrl (F36): This latch is set by the fall of 'operational in' and 'status in' if the CC sync latch is on. It causes reselection of the device for the chain command operation. It is reset by the response to the initial selection status during the reselection sequence.

Mode Triggers

Mode triggers are reset at the end of their sequence.

Mode Trg 1 (G1): Controls data sequences for both multiplex and selector subchannels.

Mode Trg 2 (G2): Indicates that a CDA sequence for either the multiplex or selector subchannel is in process. The new CCW is fetched during this sequence.

Mode Trg 3 (G3): Is a CDA sequence which modifies (for use by the 2870) the new CCW obtained during trigger 2.

Mode Trg 4 (G4): Is a multiplex write CDA operation which fetches data using the data address in the new CCW.

Mode Trg 5 (G5): Is a SSC CSW cycle that assembles channel and control unit status.

Mode Trg 6 (G6): Is a SSC CSW cycle. This trigger is turned on at the completion of a trigger 5 sequence. Trigger 6 assembles the CSW and stores it in local storage.

Mode Trigger 7 (G7): Assembles, and stores in main storage, a CSW for a pseudo test I/O or an initial selection status sequence (code 01 response to start I/O, test I/O, or halt I/O).

Mode Trigger 8 (G8): Is a selector subchannel chain command sequence. Trigger 8 is turned on if a control unit returns a status byte with the status modifier bit on. The trigger 8 sequence increments the command address by eight before fetching the next CCW.

Mode Trigger 9 (G9): Is a multiplex subchannel CSW sequence that assembles channel and control unit status, stacks status, or turns on the multiplex chain command trigger if chaining is indicated.

Mode Trigger 10 (G10): Is turned on by trigger 9 if interrupt status is not stacked. Trigger 10 assembles a CSW and stores it in local storage.

Mode Trigger 11 (G11): Stores a CSW (assembled and stored in local storage UCW 2 during a previous operation) into main storage, when the channel receives an interrupt response or test I/O instruction from the CPU.

Clock On (G12): Indicates that the main channel clock is on. The main channel clock is reset at the end of every sequence.

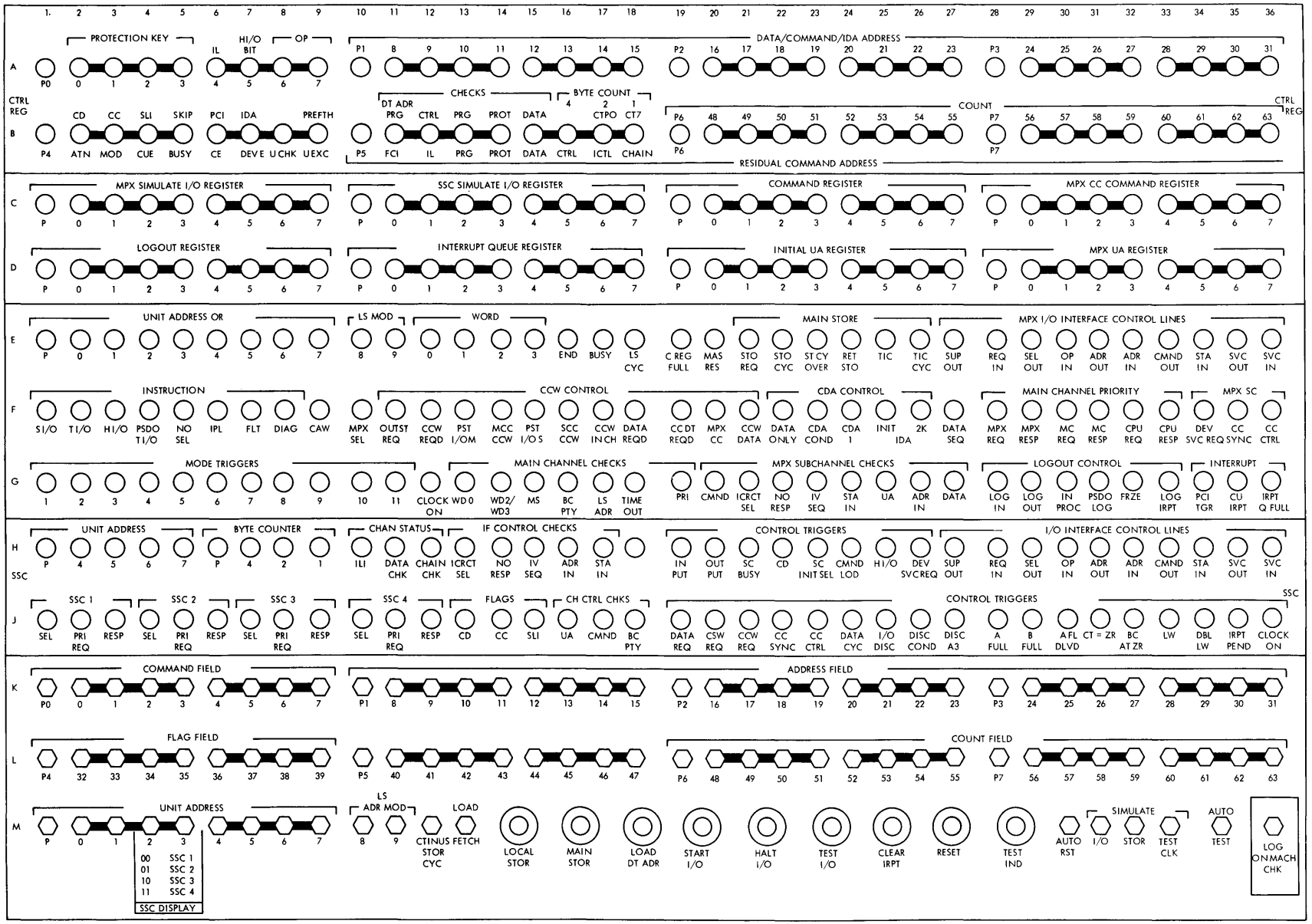


Figure 6-1A. CE Console (2870B with CIDA Feature)

Main Channel Checks

All checks are reset at the end of the sequence.

WD-0 (G13): A parity error was detected while storing UCW 0 from the control register into local storage.

WD-2 (G14): A parity error was detected while storing UCW 2 from the control register into local storage.

WD-2/WD-3 (G14): A parity error was detected while storing UCW 2 from the control register into local storage or a parity error was detected while storing UCW 3 from the control register into local storage if either the initial IDA or the 2K-IDA latch are on. Note: WD-3 check is used only with the CIDA feature. (See Figure 6-1A).

MS (G15): A storage data check occurred on a CCW fetch, or a storage address check occurred during a BCU operation.

BC Pty (G16): A byte count parity error was detected, at the byte count register, when the byte count was gated from the control register during a multiplex trigger 1 sequence.

LS Adr (G17): A parity error was detected at the unit address OR during a local storage cycle.

Time Out (G18): A main channel busy condition (for an initial selection sequence) lasted longer than 16 ms during a CPU instruction.

Pri (G19): Is a priority circuit failure caused by the response not equal to the request, or the request not reset by the response.

Mpx Subchannel Checks

Reset occurs on the next subchannel operation (initial select or device service request).

Cmnd (G20): A parity error was detected on bus out when 'command out' was sent in response to 'address in.'

ICRCT Sel (G21): An address mismatch occurred during an initial selection sequence.

No Resp (G22): A no selection occurred during a chain command reselection sequence.

IV Seq (G23): Invalid interface sequence was caused by the fall of 'operational in' before the fall of 'select out.'

Sta In (G24): A parity error was detected in the status byte on bus in.

UA (G25): A parity error was detected on bus out when the unit address was placed on bus out during an initial selection sequence.

Adr In (G26): A parity error was detected on address in during a device service request sequence.

Data (G27): A parity error occurred on bus out or bus in during a data transfer sequence.

Logout Control

Log In (G28): This indicator is on during a log in 1, log in 2, log CSW cycle, or a long CSW complete sequence. These sequences assemble log words and store them in local storage.

Log Out (G29): This indicator is on during a log first word, log second word, log third word, or a log CSW sequence. These sequences store log words in main storage from local storage.

In Proc (G30): Turned on during log in 2 sequence and remains on until logout is completed.

Psdo Log (G31): This indicator is on during a pseudo log 1, pseudo log 2, or pseudo log 3 sequence. These sequences assemble and store log words and a CSW into main storage, without a log-in to local storage. A machine reset is performed at the completion of this operation.

FRZE (G32): The freeze latch is set during a pseudo log sequence, or by a control check during a log in sequence. This latch causes an immediate logout and a machine reset.

Log Irpt (G33): A log interrupt request is outstanding to BCU. This latch is reset at the beginning of the logout operation.

Interrupt

PCI (G34): A PCI interrupt is outstanding for the multiplex subchannel or a selector subchannel. This trigger is reset when the PCI interrupt is cleared or when the PCI bit is stored in the CSW.

CU Irpt (G35): A control unit interrupt is outstanding for the multiplex subchannel and status is stacked in the device. This latch is reset by multiplex initial selection.

Irpt Q Full (G36): A PCI interrupt, a multiplex subchannel control unit interrupt, or a multiplex subchannel interrupt is outstanding. The device address is in the interrupt register. This latch is reset when the interrupt is cleared.

SSC Indicators

Rows H and J display the SSC determined by the SSC display (unit address switches 2 and 3), except when a SSC log-on machine check is in process. During a log-on machine check, rows H and J display the SSC being logged.

Unit Address (H1-5): This register displays the low order four bits (+P) of the SSC address. The high-order four bits are prewired. Parity is determined by all eight bits. This register represents the address of the last operation performed.

Byte Counter (H6-9): This three-bit plus parity register displays the SSC byte count. A master reset does not change the contents of this register.

Channel Status

ILI (H10): This indicator is turned on, regardless of the SLI flag, if a wrong length record condition occurs. It is reset by the next initial selection sequence.

Data Chk (H11): A parity error occurred on bus-out or bus-in during a data sequence. It is reset by the next SSC operation.

Chain Chk (H12): A loss of data occurred during a read chain data operation. It is reset by the next SSC operation.

IF Control Checks

These checks are reset by the next SSC operation.

ICRCT Sel (H13): An address mismatch occurred during an initial selection sequence.

No Resp (H14): A no selection occurred during a chain command operation.

IV Seq (H15): An invalid tag sequence was caused by the fall of 'operational in' before the fall of 'select out.'

Adr In (H16): A parity error occurred on bus in when the control unit returned its address and address in.

Sta In (H17): A parity error was detected in a status byte.

Control Triggers

Input (H19): An input operation is in progress (read, read backward, sense). It is reset at the end of the operation.

Output (H20): An output operation is in progress (write or control). It is reset at the end of the operation.

SC Busy (H21): This trigger is turned on during an initial selection sequence and remains on until the subchannel is free to accept a new operation (instruction or device service request).

CD (H22): A write or read chain data operation is in progress. It is reset when the subchannel uses the first doubleword of data under the new CCW.

SC Init Sel (H23): This trigger is set at the beginning of an initial selection sequence and remains on until the initial status byte is accepted or a status cycle is requested.

CMND LDD (H24): This trigger is set to indicate that a CCW has been loaded into the SSC from main channel. It is reset when the CCW operation is terminated.

H I/O (H25): This trigger is set when the halt I/O sequence is executed on the subchannel interface. It is reset when the halt I/O instruction is released.

Dev Svc Req (H26): This trigger is set by 'operational in' and 'address in' for an interrupt sequence. It is reset by the fall of 'operational in'and 'status in.'

I/O Interface Control Lines

These indicators display the status of the I/O interface lines.

Sup Out (H27): Monitors the suppress out line.

Req In (H28): Monitors the request in line.

Sel Out (H29): Monitors the select out line.

Op In (H30): Monitors the operational in line.

Adr Out (H31): Monitors the address out line.

Adr In (H32): Monitors the address in line.

Cmnd Out (H33): Monitors the command out line.

Sta In (H34): Monitors the status in line.

Svc Out (H35): Monitors the service out line.

Svc In (H36): Monitors the service in line.

SSC1, SSC2, SSC3, SSC4 (J1-12)

These indicators are not controlled by the SSC display switch settings. Because the four groups of lights are identical, only the SSC1 group is described.

Sel (J1): Turned on when main channel requests an initial selection sequence by this subchannel. Remains on until the CPU is released. Also, turned on during a SSC logout to force an SSC response to reset the interrupt pending trigger.

Pri Req (J2): Indicates that a subchannel priority request to main channel is active for a data transfer, CSW assembly, or an interrupt response. Reset by subchannel response.

Resp (J3): Indicates that selector subchannel 1 priority is active.

Flags

Reset occurs on a master reset.

CD (J13): Indicates that a chain data address operation is to be performed on the SSC. Set by CCW gate to SSC and the CD flag in the CCW.

CC (J14): Indicates that a chain command operation is to be performed on the SSC. Set by CCW gate to SSC and the CC flag in the CCW.

SLI (J15): Inhibits wrong length record indication in the CSW and allows chain command operations to be executed with ILI on. Set by CCW gate to SSC and the SLI flag in the CCW.

Channel Control Checks (Ch Ctrl Chks)

Reset by the next SSC operation.

UA (J16): An address out parity error was detected during an initial selection sequence.

CMND (J17): A parity error occurred on bus out (during an initial selection sequence) when command out was raised in response to address in.

BC PTY (J18): A parity error was detected in the byte count register.

Control Triggers

Data Req (J19): A main channel trigger 1 sequence is being requested. Reset by subchannel response.

CSW Req (J20): A trigger 5 or trigger 7 request is active. Reset by SSC response.

CCW Req (J21): A chain command CCW operation is requesting a main channel SSC pseudo start I/O operation. Reset by the CCW gate for the new CCW.

CC Sync (J22): This control latch is set during a SSC status sequence if the CC flag is on and no interrupt conditions exist. It remains on, from its turn-on by 'channel end status,' until the fall of 'operational in' causes a subchannel reset (to prepare for reselection), or it is reset during the next device end status sequence if an interrupt condition exists.

CC Ctrl (J23): This latch is set if the device end status bit is presented, no interrupt conditions exist, and CC sync is on. CC control causes a device reselection sequence for the chain command operation. It is reset by the response to initial selection status during the reselection sequence.

Data Cyc (J24): This is set by a zero initial selection status byte and remains on until ending status is received.

I/O Disc (J25): This is turned on when interrupt status is received and causes an I/O disconnect sequence when the subchannel is free to generate a status cycle request or perform a chain command operation.

Disc Cond (J26): This sequence is started by the I/O disconnect trigger to handle interrupt status. It controls the turn-on of chain command sync, status cycle request, service out, and the turn-off of select out.

Disc A3 (J27): This is turned on by disconnect condition and SSC clock A3 time and remains on until the fall of disconnect condition (after the fall of operational in and status in).

A Full (J28): This indicates that buffer register A contains a doubleword of data. It is reset when the A register contents are transferred to the B register.

B Full (J29): This indicates that buffer register B contains a doubleword of data. It is reset when the last byte of data is transferred to the control unit during an output operation, or when the doubleword of data is stored in the main channel data register during an input operation.

A Fl Dlyd (J30): This control trigger is set by the last data byte of an input operation. This trigger controls the turn-on of A full when the B register is empty, blocks the turn-on of I/O disconnect condition until the data is transferred to main storage. This trigger is reset by the data cycle request for the last doubleword of data.

CT=ZR (J31): This trigger is set when the last byte of data for the current CCW is transferred for an input or an output operation. Reset during the next initial selection or when the first byte of data is transferred under the new CCW on a CDA operation.

BC at ZR (J32): This trigger is set when the byte count latches are stepped to zero. This latch is reset during the next initial selection sequence or the next data transfer.

LW (J33): Last word is set when the last doubleword of data for the CCW is being transferred by the SSC. This latch is used for main channel count recovery if an error occurs during an output operation. It is reset during the next initial selection sequence.

Dbl LW (J34): Double last word is set when the next to the last doubleword is being transferred. This latch is used for main channel count recovery if an error occurs during an output operation. It is reset during the next initial selection sequence.

Irpt Pend (J35): The interrupt pending latch requests an interrupt response from the CPU. It remains on until interrupt response is granted. It is used for an ending interrupt, a control unit interrupt, and a log interrupt.

Clock On (J36): The selector subchannel clock is on.

CE Console Toggle Switches

Simulate Storage Bus Out Switches (K1-K36 and L1-L36)

These switches (72) are active only in the test mode. In a manual store operation, the switch settings determine the data placed in storage. If the simulate storage switch is also on and the channel performs a CCW fetch, the switches are gated as follows:

Row K	1-9	Command register and first byte of the data register
Row K	10-36	Bytes 1-3 of the control register (data address)
Row L	1-9	Byte 4 of the control register (flags)
Row L	19-36	Bytes 6 and 7 of the control register (count)

Switches L10-L18 are ignored and may represent any data configuration.

If the channel performs a data fetch and the simulate storage switch is on, all the switches are gated to the data register and also to the selector subchannel A register, if a selector subchannel is selected. Therefore, three limitations occur when using the switches:

1. The same CCW configuration is used repeatedly during chaining operations.
2. The same eight bytes of data are used repeatedly during a write operation.
3. The data word must represent a valid CCW and CAW.

Unit Address Switches (M1-M9)

These nine switches are active only in the test mode and are gated to the unit address register as though they had come over the unit address bus. If the simulate I/O switch is on, the switches may simulate any address. If the simulate I/O switch is off, the switches should represent a valid I/O address. If they do not, and a start I/O, test I/O, or halt I/O instruction is simulated, a no selection occurs. If a no selection occurs, the channel must be reset before any other operation is performed.

Local Store Address Modify Switches (M4 and M5)

These two switches are used in addition to the unit address switches to generate a local storage address for displaying or loading local storage.

Control Switches

Auto/Test (N34-5): In the auto position, this switch disables all CE console switches and pushbuttons

except the log-on-machine-check switch, selector subchannel display switches, and test indicator pushbutton. In the test position, the channel simulates the CPU, all CE console switches and pushbuttons are active, and the channel customer clock is stopped. When the switch is changed from test to auto, a complete reset of the 2870 is performed.

Simulate Test Clock (M33): This switch keeps the channel clock cycling to permit examination and adjustment of the clock timing. The clock contains tapped delay lines that are adjusted according to the instructions in the FE Maintenance Manual, IBM 2870 Multiplexer Channel (70,000 Series), Form Y27-2154. This switch must be off for all other operations.

Simulate Storage (M32): This switch permits the channel to operate without a storage or BCU. All communications with the BCU and storage are blocked. The storage bus out is simulated by the CE console switches, and the storage and BCU control lines are simulated within the 2870. All data normally stored is lost. The channel simulate storage controls are normally set to represent a 1-usec storage cycle time. This time is measured from the rise of storage request to the rise of advance pulse.

Simulate I/O (M31): This switch permits the channel to operate without a device or control unit. All in lines from the I/O devices to the channel and the channel select out line are blocked. A nine-bit simulate I/O register between the bus out and the bus in receives the bytes sent over the bus out during a write or control operation. This register retains the last byte written and places it on the bus in when reading. The simulated data rate is adjusted for 10 usec between the rise of successive request ins for multiplex operation, and approximately 4 usec (SSC1-3) or 8 usec (SSC4) between the rise of successive service ins for selector subchannel operations.

Auto Restart (M30): This switch is active only in test mode. The switch, when active, causes repetitive resetting of the channel every 16 ms, or until an error condition is sensed. After the reset is over, a start I/O is initiated, and the channel executes the instruction until the next restart pulse. The cycle is repeated as long as a storage cycle is not in progress. All CE console pushbuttons are inactive when this switch is on.

Selector Subchannel Display (M2, M3): These two switches determine which of the four selector subchannels are displayed in indicator rows H and J. These switches are always active except when a log-on-machine check is in process, at which time rows H and J display the contents of the selector subchannel that is being logged.

Load/Fetch (M13): The position of this toggle switch determines whether a load or fetch operation will be performed when the local store or main store pushbutton is depressed.

Continuous Store Cycle (M12): When this switch is on, a load or fetch operation initiated by the local store or main store pushbutton is executed continuously.

Log On Mach Chk (M36): This switch is active in either the auto or test mode. However, its function is not the same for both cases.

When the switch is down and the 2870 is in the auto mode, the channel stops and logs out three log words and a CSW when a machine check occurs.

The logout function causes the channel to raise the interrupt request line and wait for the CPU to respond. When response is received, the first double word is stored, starting at byte address 304. The next channel to main storage cycle is allowed to pass; then another request is made. This continues until the four double words have been stored.

In the test mode, with the log-on-machine-check switch down, the channel stops when it detects a machine check or a data check. The logout function is further explained in the Maintenance Features section.

A channel machine check includes:

1. Storage Data Check -- Main storage detected a parity check on the CAW or CCW sent to the channel.
2. Storage Address Check -- Main storage detected a parity check on the address or mark parity or the protection keys sent by the channel.
3. Unit Address Check -- The unit address on the I/O bus out had incorrect parity.
4. Command Check -- The command on the I/O bus out had incorrect parity.
5. Byte Counter Check -- The byte counter predicted parity and actual parity does not agree in either the main channel or one of the selector subchannels.
6. Unit Control Word Check -- The channel detected a parity check on the control register when it was stored in local storage.

7. Local Storage Address Check -- The address used by local storage had incorrect parity.

8. Priority Check -- The main channel priority circuits gave priority to a subchannel not requesting it, or the requesting subchannel failed to stop requesting priority after receiving it.

9. Channel Time-Out -- The CPU had not been released an abnormal period of time after issuing select channel.

10. Address In Check -- The channel detected a parity check on the address received from the device, following request in.

11. Status In Check -- The channel detected a parity check on the status received from the device.

12. Incorrect Selection -- The address received from an I/O unit during initial selection does not agree with the address sent from the channel.

13. No Response -- The I/O unit did not respond to address out for reselection during a chain command operation.

14. Incorrect Tag Sequence -- The selected I/O unit dropped its operational in line before the channel dropped the select out line.

Checks 1-8 turn on the channel control check trigger; checks 9-14 turn on the interface control check trigger.

Detection of checks 3 and 7-10 or detection of any second check during logout causes a full reset of the 2870 and any attached control units after completion of the logout.

A data check includes:

1. Storage Data Bus In Parity Check -- The channel detected a parity error on the data sent to main storage.

2. Storage Data Check -- Main storage detected a parity error on the data sent to or fetched from main storage.

3. Bus In Parity Check -- Data on the I/O bus in had incorrect parity.

4. Bus Out Parity Check -- Data on the I/O bus out had incorrect parity.

Note: Channel logout words are stored in main storage only when the 2870 is in the auto mode. In test mode, the logout words are stored in local storage only.

CE Console Pushbuttons

Reset: If the log-on-machine-check switch is up (off), this pushbutton causes all channel registers and triggers (except the simulate I/O registers and SSC byte counter) to be reset and resets all local storage words to 0 with correct parity.

If the log-on-machine-check switch is down (on), all channel registers and triggers (except the simulate I/O registers and SSC byte counter) are reset, but the contents of local storage are not disturbed.

For either position of the log-on-machine-check switch, all attached I/O units are also reset if the simulate I/O switch is off.

Clear Interrupt: This pushbutton simulates the interrupt response line from the CPU in answer to an interrupt request from the channel. It is used when an interruption is outstanding in the channel.

Load Data Address: This pushbutton causes switches K10-36, to be gated to the control register. However, only switches K10-33 should be used, because the channel addresses main storage on double word boundaries. When a manual store or fetch operation is performed, the contents of the data address are gated to the storage address bus, determining the location addressed in storage. At the completion of the storage operation, the data address is incremented by eight bytes. When the maximum storage address is reached, the address wraps around to zero and continues. If the continuous storage cycle switch is down, the address is not incremented.

Local Store: This pushbutton, in conjunction with the load/fetch toggle switch, initiates a local store load or fetch. In either case, the local store address is that contained in the unit address and local storage address modifier switches.

During the load operation, the contents of the simulate storage bus out switches are gated to the data register and from the data register to local storage.

During a fetch operation, the contents of the local storage location specified replace the contents of the control register, unless local storage address modify switch 8 is off and switch 9 is on. In this case, the word is fetched to the data register, then gated to the control register for display. In either case, the contents of the local storage word fetched are automatically restored.

Main Store: This pushbutton, with the load/fetch switch, initiates a main storage load or fetch. In either case, the main storage address is that contained in bytes 1-3 of the control register (data address).

During the load operation, the contents of the simulate storage bus out switches are gated to the

data register. The contents of the data register are gated to the storage data bus in and stored in the location specified by the contents of the data address.

During a manual (single cycle) fetch operation, a doubleword of information is fetched from the storage location specified by the data address and placed in the data register, then gated to the control register for display. It is necessary to load the data address again in order to perform another data fetch. If the continuous storage cycle switch is down, the address is not incremented, and the data register contents are not gated to the control register for display.

Test I/O: This pushbutton permits the channel to issue a test I/O command to a connected I/O device, or to simulate the test I/O sequence within the channel.

If the channel is in the test mode and not simulating I/O, the unit address switches are sent to the initial unit address register and determine which I/O unit is selected. When the instruction is completed, the channel is in the interrupt state with the I/O unit status in local storage.

If the channel is simulating I/O, the channel's manual controls simulate an I/O unit, responding to the test I/O command with a status byte containing no status bits.

Start I/O: This pushbutton simulates the issuing of the start I/O instruction by the CPU. If the channel simulate storage switch is off, the instruction proceeds as a normal start I/O.

If the simulate storage switch is on, the channel does not fetch the CAW. Instead, a CCW is fetched from the channel switches. The unit address switches are gated to the initial unit address register. During the operation, the channel uses the switches to represent data or additional CCWs fetched from storage.

If a chain flag is set in the switches, the channel runs continuously. Otherwise, the channel ends with the interrupt queue full trigger on (MSC) or the interrupt pending trigger (SSC) on.

Halt I/O: This pushbutton simulates the halt I/O instruction issued by the CPU, and causes the addressed subchannel to stop its present operation, disconnects the I/O device, and turns on the interrupt queue trigger (MSC) or the interrupt pending trigger. (SSC).

Test Indicators: This switch is active in test or auto mode and tests all indicators on the CE console. If no selector subchannels are installed, indicators C10-C18, H1-H36, J2, J5, J8, J11 and J13-J36 will not light.

Power Panel Switches, Jacks, Indicators, and Meter (Figure 6-2)

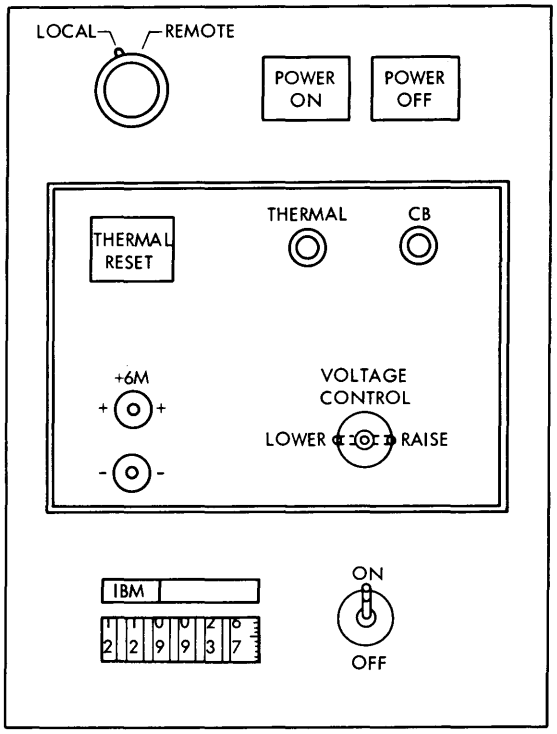


Figure 6-2. Power Control Panel

Power on Pushbutton: This pushbutton initiates a channel power-on sequence. This pushbutton is active only if the local/remote switch is at LOCAL, and is back-lighted to indicate power on.

Power off Pushbutton: This pushbutton initiates a power-off sequence for the channel. It is enabled for either position of the local remote switch and is active only when power is on the channel.

Thermal Reset Pushbutton: This pushbutton resets the thermal interlock circuitry after a thermal fault occurs in the channel. This reset precedes power restoration to the channel after a thermal fault.

+6M Jacks: This set of two jacks permits external voltage measurement of the output of the +6M volt regulator.

Local/Remote Switch: This two-position rotary switch selects power control at either the channel frame (local) or the MCF (remote).

Voltage Control Switch: This three-position (spring loaded to center off) switch controls variations in the channel +6M regulator. Release of this switch locks the voltage setting at the value created by the hold-down. This switch is active only when the local remote switch is at LOCAL.

Enable Meter Switch: This two-position switch controls running of the customer time meter. The time meter runs if the switch is at the enable position and stops if the switch is at the off position. The same positions enable or disable channel operation with the CPU.

Time Meter: This is a usage meter to record customer running time on the channel frame.

Thermal Trip Indicator: This indicator turns on when the thermal CB trips to monitor excessive temperature conditions in either the regulators or the logic gates. Depressing thermal reset turns off the indicator.

CB Trip Indicator: This indicator turns on when any CB within the channel, except main line disconnect, has tripped. Possible causes are overcurrent at the input of the bulk supply, overcurrent or overvoltage within one of the regulator modules, or overcurrent at the gate blowers. Resetting the tripped CB turns off the indicator. The power-on pushbutton must be used to restore channel power.

SECTION 2. CE CONSOLE (SERIAL NO. 60,000 AND 60,002 THROUGH 69,999)

CONSOLE CONTROLS AND INDICATORS

Switches and indicators for channel tests on the CE console are arranged vertically and horizontally in an alphameric matrix. The rows of switches and indicators are labeled A-N (from top to bottom) and 1-36 (from left to right). Rows A-K are indicators, and rows L-N are switches (Figure 6-3).

The power panel contains switches and jacks for controlling and regulating power and a meter for recording channel running time (Figure 6-2).

CE Console Indicators

Indicators in rows A and B represent the control register; those in rows C and D represent the data register. Rows E through H are for main channel and multiplex subchannel. Rows J and K display the contents of the major control triggers and registers of the selector subchannel (SSC) except when an SSC log-on-machine-check operation is in progress. During an SSC log-on-machine-check operation, rows J and K display the contents of the triggers and registers in the SSC being logged. The console indicators are described below.

CTRL REG (A1-A36 and B1-B36): These indicators display the 64 data bits plus 8 parity bits of the control register. The control register is divided into fields that represent a CAW, CCW, or CSW (word 0, word 2, or word 3). A master reset clears the register and sets the parity bits. Otherwise, the indicators display the contents of the control register as left by the last operation performed.

DATA REG (C1-C36 and D-D36): These indicators display the 64 data bits plus 8 parity bits of the data register. The DATA REG indicators display WD-1 on a manual LS fetch and display data being stored or fetched during a manual main storage operation. A master reset at the end of a main channel sequence clears the register and sets the parity bits.

MPX Simulate I/O Register (E1-9): This is a data register (eight bits plus parity) used in simulate I/O operations for the multiplex interface. The register is loaded by a write operation. Data is obtained from this register during a read operation. Machine reset does not affect the contents of this register.

SSU Simulate I/O Register (E10-18): This is a data register (eight bits plus parity) used in simulate I/O operations for any selector subchannel interface. The register is loaded by a write operation. Data is obtained from this register during a read operation. Machine reset does not affect the contents of this register.

Command Register (E19-27): The command byte (eight bits plus parity) is stored in this register during a multiplex start I/O CCW fetch. A master reset, or a multiplex start I/O CCW fetch changes the contents of this register.

MPX CC Command Register (E28-36): The command byte (eight bits plus parity) is stored in this register during a multiplex chain command CCW fetch.

Note: The command register may also contain a command. Master reset or multiplex chain command CCW fetch changes the contents of this register.

Instructions

S I/O (F1): The start I/O latch is set during a CAW fetch. It is reset when CPU drops the select channel line.

T I/O (F2): A main channel test I/O sequence is in progress. (The CPU may or may not be released at this time.)

H I/O (F3): A main channel halt I/O sequence is in progress. (The CPU may or may not be released at this time.)

IPL (F4): The channel is performing an initial program load sequence. This latch is reset when CPU is released.

FLT (F5): An FLT operation is in progress with a selector subchannel.

Diag (F6): The diagnose line is active from CPU. This causes channel to operate in the simulate I/O mode.

LOG (F7): This indicator is on when a log-in or logout is in progress; it remains on from the time a control check is detected until the logout is completed.

TIC (F8): A TIC command is decoded on a CCW fetch. It is reset during the TIC cycle sequence.

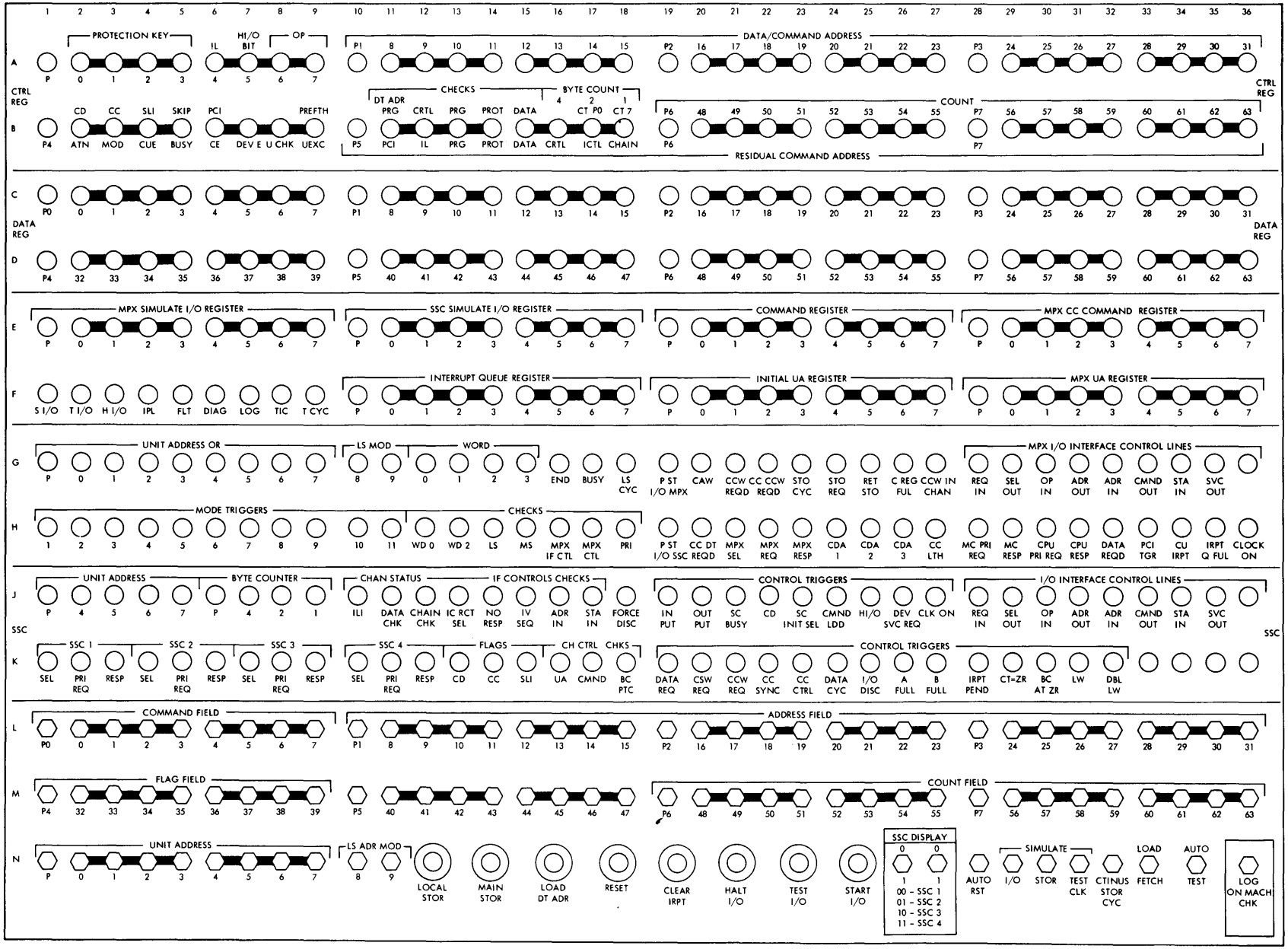


Figure 6-3. CE Console (Serial No. 60,002 through 69,999)

T Cyc (F9): This trigger controls the main channel update of the command address and the fetch of the new CCW. It is reset at completion of the CCW fetch cycle.

Interrupt Queue Register (F10-18): This eight-bit (plus parity) register holds the address of the subchannel that has an outstanding interrupt request ('interrupt buffer full' trigger on). This register is used for multiplex subchannel interrupts and selector subchannel PCI interrupts. Master reset, diagnostic test local store, or the setting of 'interrupt buffer full' changes the contents of this register.

Initial UA Register (F19-27): This register contains the address (eight bits plus parity) of the device for an initial selection. It is loaded from the CPU interface via UABO. It is also loaded from the unit address OR on a pseudo test I/O. Master reset clears this register and sets the parity bit.

MPX UA Register (F28-36): This eight-bit (plus parity) register is set from the initial unit address register during a multiplex initial selection sequence or from the address on bus-in presented (by a control unit) during a device service request sequence. Master reset clears this register and sets the parity bit.

Unit Address OR (G1-9): This eight-bit (plus parity) OR displays the device address for which the main channel sequence is active. The address presented to local storage is obtained from this OR.

LS Mod (G10-11): These two bits represent a decode of one of the four local storage words for the device address indicated by the unit address OR. The contents of this register represent the word fetched or stored on the last local storage operation.

Word 0 (G12): Word 0 is fetched for the device displayed in the unit address OR.

Word 1 (G13): Word 1 is fetched for the device displayed in the unit address OR. Word 1 control is also used during a master reset or test local storage operation.

Word 2 (G14): Word 2 is fetched for the device displayed in the unit address OR.

Word 3 (G15): Word 3 is fetched for the device displayed in the unit address OR.

End (G16): 'End' is turned on to complete a main channel sequence. This turns off 'busy' when main channel operations are completed. The release of the priority circuits resets this trigger.

Busy (G17): 'Busy' is set by priority circuits at beginning of a main channel sequence and remains on until 'end' turns it off.

LS Cycle (G18): A local storage fetch or store cycle is in progress.

PST I/O MPX (G19): The multiplex pseudo start I/O trigger causes a CCW to be fetched for a multiplex subchannel chain-command operation. Pseudo start I/O has priority over a start I/O operation. This latch is reset at the end of the main channel response for the CCW fetch.

CAW (G20): A CAW is being fetched for a start I/O instruction. This latch is reset at the completion of the CAW fetch.

CCW Reqd (G21): CCW required fetches a CCW for start I/O operation. This latch is reset at the end of the CCW fetch.

CC CCW Reqd (G22): This trigger causes a CCW to be fetched during the MS response sequence for the multiplex pseudo start I/O instruction. This trigger is reset at the completion of the CCW fetch.

Stor Cyc (G23): A storage cycle with the BCU is in progress.

Sto Req (G24): A storage request is outstanding to the BCU.

Ret Sto (G25): 'Retain storage' causes main channel to perform two main storage fetches.

C Reg Full (G26): A local store fetch to the control register is completed. It is reset at the end of the main channel sequence.

Multiplex Subchannel I/O Interface Control Lines

Req In (G28): Monitors the 'request in' line.

Sel Out (G29): Monitors the 'select out' line.

Op In (G30): Monitors the 'operational in' line.

Adr Out (G31): Monitors the 'address out' line.

Adr In (G32): Monitors the 'address in' line.

Cmnd Out (G33): Monitors the 'command out' line.

Sta In (G34): Monitors the 'status in' line.

Svc Out (G35): Monitors the 'service out' line.

Svc Out (G36): Monitors the 'suppress out' line.

Mode Triggers

Mode triggers are reset at the end of their sequence.

Mode Trg 1 (H1): Controls data sequences for both multiplex and selector subchannels.

Mode Trg 2 (H2): Indicates that a CDA sequence for either the multiplex or selector subchannel is in process. The new CCW is fetched during this sequence.

Mode Trg 3 (H3): A CDA sequence which modifies (for use by the 2870) the new CCW obtained during trigger 2.

Mode Trg 4 (H4): A multiplex write CDA operation which fetches data using the data address in the new CCW.

Mode Trg 5 (H5): A SSC CSW cycle that assembles channel and control unit status.

Mode Trg 6 (H6): A SSC CSW cycle. This trigger is turned on at the completion of a trigger 5 sequence. Trigger 6 assembles the CSW and stores it in local storage.

Mode Trigger 7 (H7): Assembles, and stores in main storage, a CSW for a pseudo test I/O or an initial selection status sequence (code 01 response to start I/O, test I/O, or halt I/O).

Mode Trigger 8 (H8): A selector subchannel chain command sequence. Trigger 8 is turned on if a control unit returns a status byte with the status modifier bit on. The trigger 8 sequence increments the command address by 8 before fetching the next CCW.

Mode Trigger 9 (H9): A multiplex subchannel CSW sequence that assembles channel and control unit status, stacks status, or turns on the multiplex chain command trigger if chaining is indicated.

Mode Trigger 10 (H10): Turned on by trigger 9 if interrupt status is not stacked. Trigger 10 assembles a CSW and stores it in local storage.

Mode Trigger 11 (H11): Stores a CSW (assembled and stored in local storage UCW 2 during a previous operation) into main storage when the channel receives an interrupt response or test I/O instruction from the CPU.

Main Channel Checks

All checks are reset at the end of the sequence.

WD-0 (H12): A parity error was detected while storing UCW 0 from the control register into local storage.

WD-2 (H13): A parity error was detected while storing UCW 2 from the control register into local storage.

LS (H14): A parity error was detected at the unit address OR during a local storage cycle.

MS (H15): A storage data check occurred on a CCW fetch, or a storage address check occurred during a BCU operation.

MPX IF CTL (H16): An address-in check, a status-in check, incorrect selection, no response, or an incorrect sequence occurred. The check condition is reset by the next subchannel operation, by an initial selection sequence, or by a device service request sequence.

MPX CTL (H17): A multiplex unit address check or a command check occurred.

Pri (H18): A priority circuit failure caused by the response not equal to the request or by the request not reset by the response.

PST I/O SSC (H19): Pseudo start I/O selector subchannel executed a chain command operation for a selector subchannel. The entire operation is performed under one SSC response. This latch is reset at the completion of the CCW in channel sequence.

CC DT Reqd (H20): This latch is set if a chain command multiplex write data fetch is interrupted by a subchannel priority request, causing data to be fetched during the next main channel response. This latch is reset at the completion of the data fetch sequence.

MPX SEL (H21): A multiplex subchannel initial selection is to be executed. This latch is reset when the CPU is released.

MPX Req (H22): The multiplex subchannel is requesting priority for a data or status cycle.

MPX Resp (H23): Multiplex subchannel priority response is active.

CDA 1 (H24): CDA 1 is set during multiplex CDA operation with count equal to 1 and no CCW prefetched. CDA 1 is reset at the completion of the CDA operation.

CDA 2 (H25): A multiplex CDA operation is in progress for a prefetched CCW (local storage UCW 3). This latch is reset at the completion of the CDA operation.

CDA 3 (H26): A multiplex write CDA CCW is being prefetched and stored in UCW 3 of local store. This latch is reset at the completion of the CDA operation.

CC LTH (H27): This latch is set when command-chaining is in progress.

MC Pri Req (H28): Main channel is requesting priority for a CPU instruction, multiplex subchannel chain command, a no selection, or a multiplex subchannel burst mode operation.

MC Resp (F31): Main channel response is active.

CPU Pri Req (H30): CPU priority is active for an interrupt register full condition or a log interrupt request.

CPU Resp (H31): CPU response is active.

Data Reqd (H32): This latch is turned on if a multiplex subchannel write data fetch during a start I/O operation is interrupted by an outstanding request. The write data is fetched when main channel again receives priority. This latch is reset at the completion of the main channel sequence that fetches the write data.

Interrupt

PCI Tgr (H33): A PCI interrupt is outstanding for the multiplex subchannel or a selector subchannel. This trigger is reset when the PCI interrupt is cleared or when the PCI bit is stored in the CSW.

CU Irpt (H34): A control unit interrupt is outstanding for the multiplex subchannel, and status is stacked in the device. This latch is reset by multiplex initial selection.

Irpt Q Ful (H35): A PCI interrupt, a multiplex subchannel control unit interrupt, or a multiplex subchannel interrupt is outstanding. The device address is in the interrupt register. This latch is reset when the interrupt is cleared.

Clock On (H36): Indicates that the main channel clock is on. The main channel clock is reset at the end of every sequence.

Unit Address (J1-5): This register displays the low-order four bits (+P) of the SSC address. The high-order four bits are prewired. Parity is determined by all eight bits. This register represents the address of the last operation performed.

Byte Counter (J6-9): This three-bit (plus parity) register displays the SSC byte count. A master reset does not change the contents of this register.

Channel Status

ILI (J10): This indicator is turned on, regardless of the SLI flag, if a wrong-length record condition occurs. It is reset by the next initial selection sequence.

Data Chk (J11): A parity error occurred on bus out or bus in during a data sequence. It is reset by the next SSC operation.

Chain Chk (J12): A loss of data occurred during a read chain data operation. It is reset by the next SSC operation.

IF Control Checks

These checks are reset by the next SSC operation.

ICRCT Sel (J13): An address mismatch occurred during an initial selection sequence.

No Resp (J14): A no-selection occurred during a chain command operation.

IV Seq (J15): An invalid tag sequence was caused by the fall of 'operational in' before the fall of 'select out.'

Adr In (J16): A parity error occurred on bus in when the control unit returned its address and address in.

Sta In (J17): A parity error was detected in a status byte.

Control Triggers

Input (J19): An input operation is in progress (read, read backward, sense). It is reset at the end of the operation.

Output (J20): An output operation is in progress (write or control). It is reset at the end of the operation.

SC Busy (J21): This trigger is turned on during an initial selection sequence and remains on until the subchannel is free to accept a new operation (instruction or device service request).

CD (J22): A write or read chain data operation is in progress. It is reset when the subchannel uses the first doubleword of data under the new CCW.

SC Init Sel (J23): This trigger is set at the beginning of an initial selection sequence and remains on until the initial status byte is accepted or a status cycle is requested.

CMND LDD (J24): This trigger is set to indicate that a CCW has been loaded into the SSC from main channel. It is reset when the CCW operation is terminated.

H I/O (J25): This trigger is set when the halt I/O sequence is executed on the subchannel interface. It is reset when the halt I/O instruction is released.

Dev Svc Req (J26): This trigger is set by 'operational in' and 'address in' for an interrupt sequence. It is reset by the fall of 'operational in' and 'status in.'

Clock On (J27): The selector subchannel clock is on.

I/O Interface Control Lines

These indicators display the status of the I/O interface lines.

Req In (J28): Monitors the 'request in' line.

Sel Out (J29): Monitors the 'select out' line.

Op In (J30): Monitors the 'operational in' line.

Adr Out (J31): Monitors the 'address out' line.

Adr In (J32): Monitors the 'address in' line.

Cmnd Out (J33): Monitors the 'command out' line.

Sta In (J34): Monitors the 'status in' line.

Svc Out (J35): Monitors the 'service out' line.

Svc In (J36): Monitors the 'service in' line.

SSC1, SSC2, SSC3, SSC4 (K1-12)

These indicators are not controlled by the SSC display switch settings. Because the four groups of lights are identical, only the SSC1 group is described.

Sel (K1): Turned on when main channel requests an initial selection sequence by this subchannel. Remains on until the CPU is released. Also turned on during an SSC logout to force an SSC response to reset the interrupt pending trigger.

Pri Req (K2): Indicates that a subchannel priority request to main channel is active for a data transfer, a CSW assembly, or an interrupt response. Reset by subchannel response.

Resp (K3): Indicates that selector subchannel 1 priority is active.

Flags

Reset occurs on a master reset.

CD (K13): Indicates that a chain data address operation is to be performed on the SSC. Set by CCW gate to SSC and the CD flag in the CCW.

CC (K14): Indicates that a chain command operation is to be performed on the SSC. Set by CCW gate to SSC and the CC flag in the CCW.

SLI (K15): Inhibits wrong-length record indication in the CSW and allows chain command operations to be executed with ILI on. Set by CCW gate to SSC and the SLI flag in the CCW.

Channel Control Checks (Ch Ctrl Chks)

Reset by the next SSC operation.

UA (K16): An address out parity error was detected during an initial selection sequence.

CMND (K17): A parity error occurred on bus out (during an initial selection sequence) when 'command out' was raised in response to 'address in'.

BC PTY (K18): A parity error was detected in the byte count register.

Control Triggers

Data Req (K19): A main channel trigger 1 sequence is being requested. It is reset by subchannel response.

CSW Req (K20): A trigger 5 or trigger 7 request is active. It is reset by SSC response.

CCW Req (K21): A chain command CCW operation is requesting a main channel SSC pseudo start I/O operation. It is reset by the CCW gate for the new CCW.

CC Sync (K22): This control latch is set during an SSC status sequence if the CC flag is on and no interrupt conditions exist. It remains on, from its turn-on by 'channel end status', until the fall of 'operational in' causes a subchannel reset (to prepare for reselection), or it is reset during the next device end status sequence if an interrupt condition exists.

CC CTRL (K23): This latch is set if the device end status bit is presented, no interrupt conditions exist, and CC sync is on. CC control causes a device reselection sequence for the chain command operation. It is reset by the response to initial selection status during the reselection sequence.

Data Cyc (K24): This is set by a zero initial selection status byte and remains on until ending status is received.

I/O Disc (K25): This is turned on when interrupt status is received and causes an I/O disconnect sequence when the subchannel is free to generate a status cycle request or perform a chain command operation.

A Full (K26): This indicates that buffer register A contains a doubleword of data. It is reset when the A register contents are transferred to the B register.

B Full (K27): This indicates that buffer register B contains a doubleword of data. It is reset when the last byte of data is transferred to the control unit during an output operation or when the doubleword of data is stored in the main channel data register during an input operation.

Irpt Pend (K28): The interrupt pending latch requests an interrupt response from the CPU. It remains on until interrupt response is granted. It is used for an ending interrupt, a control unit interrupt, and a log interrupt.

CT=ZR (K29): This trigger is set when the last byte of data for the current CCW is transferred for an input or an output operation. It is reset during the next initial selection or when the first byte of data is transferred under the new CCW on a CDA operation.

BC at ZR (K36): This trigger is set when the byte count latches are stepped to zero. This latch is reset during the next initial selection sequence or the next data transfer.

LW (K31): The last word is set when the last doubleword of data for the CCW is being transferred by the SSC. This latch is used for main channel count recovery if an error occurs during an output operation. It is reset during the next initial selection sequence.

Dbl LW (K32): Double last word is set when the next to the last doubleword is being transferred. This latch is used for main channel count recovery if an error occurs during an output operation. It is reset during the next initial selection sequence.

Time Out (K33): A main channel busy condition (for an initial selection sequence) lasted longer than 16 ms during a CPU instruction.

No Sel (K34): A select-in was received during an initial selection sequence. It is reset with the next main channel priority request or CPU priority request.

Psdo T I/O (K35): This trigger is turned on to clear a control unit interrupt during CPU priority response, causing a test I/O to be executed to clear the device status. This trigger remains on until the CPU is released.

Log Irpt (K36): A log interrupt request is outstanding to BCU. This latch is reset at the beginning of the logout operation.

CE Console Toggle Switches

Simulate Storage Bus Out Switches (L1-L36 and M1-M36)

These switches (72) are active only in the test mode. In a manual store operation, the switch settings determine the data placed in storage. If the simulate storage switch is also on and the channel performs a CCW fetch, the switches are gated as follows:

Row L	1-9	Command register and first byte of data register
Row L	10-36	Bytes 1-3 of control register (data address)
Row M	1-9	Byte 4 of control register (flags)
Row M	19-36	Bytes 6 and 7 of control register (count)

Switches M10-M18 are ignored and may represent any data configuration.

If the channel performs a data fetch and the simulate storage switch is on, all the switches are gated to the data register and, also, to the selector subchannel A register if a selector subchannel is selected. Therefore, three limitations occur when using the switches:

1. The same CCW configuration is used repeatedly during chaining operations.

2. The same eight bytes of data are used repeatedly during a write operation.

3. The data word must represent a valid CCW and CAW.

Unit Address Switches (N1-N9)

These nine switches are active only in the test mode and are gated to the unit address register as though they had come over the unit address bus. If the simulate I/O switch is on, the switches may simulate any address. If the simulate I/O switch is off, the switches should represent a valid I/O address. If they do not, and a start I/O, test I/O, or halt I/O instruction is simulated, a no selection occurs. If a no selection occurs, the channel must be reset before any other operation is performed.

Local Store Address Modify Switches (N4 and N5)

These two switches are used in addition to the unit address switches to generate a local storage address for displaying or loading local storage.

Control Switches

Auto/Test (N34-35): In the auto position, this switch disables all CE console switches and pushbuttons except the log-on-machine-check switch, selector subchannel display switches, and test indicator pushbutton. In the test position, the channel simulates the CPU, all CE console switches and pushbuttons are active, and the channel customer clock is stopped. When the switch is changed from test to auto, a complete reset of the 2870 is performed.

Test/ND (N31): Provides a test for all indicators. If the SSC feature is not installed, the SSC simulated I/O register and rows J and K (except J7-J9, J34, K1-12, and K32-K36) indicators will not light.

Simulate Storage (N30): This switch permits the channel to operate without a storage or BCU. All communications with the BCU and storage are blocked. The storage bus out is simulated by the CE console switches, and the storage and BCU control lines are simulated within the 2870. All data normally stored is lost. The channel simulate storage controls are normally set to represent a 1-usec storage cycle time. This time is measured from the rise of storage request to the rise of advance pulse.

Simulate I/O (N29): This switch permits the channel to operate without a device or control unit. All in lines from the I/O devices to the channel and the channel select out line are blocked. A nine-bit simulate I/O register between the bus out and the bus in receives the bytes sent over the bus out during a write or control operation. This register retains the last byte written and places it on the bus in when reading. The simulated data rate is adjusted for 10 usec between the rise of successive request-in's for multiplex operation, and approximately 4 usec (SSC1-3) or 8 usec (SSC4) between the rise of successive service-in's for selector subchannel operations.

Auto Restart (N28): This switch is active only in test mode. The switch, when active, causes repetitive resetting of the channel every 16 ms, or until an error condition is sensed. After the reset is over, a start I/O is initiated, and the channel executes the instruction until the next restart pulse. The cycle is repeated as long as a storage cycle is not in progress. All CE console pushbuttons are inactive when this switch is on.

Selector Subchannel Display (N26, N27): These two switches determine which of the four selector subchannels are displayed in indicator rows J and K. These switches are always active except when a log-on-machine check is in process, at which time rows J and K display the contents of the selector subchannel that is being logged.

Load/Fetch (N33): The position of this toggle switch determines whether a load or fetch operation will be performed when the local store or main store pushbutton is depressed.

Continuous Store Cycle (N32): When this switch is on, a load or fetch operation initiated by the local store or main store pushbutton is executed continuously.

Log On Mach Chk (N36): This switch is active in either the auto or test mode. However, its function is not the same for both cases.

When the switch is down and the 2870 is in the auto mode, the channel stops and logs out three log words and a CSW when a machine check occurs.

The logout function causes the channel to raise the interrupt request line and wait for the CPU to respond. When response is received, the first doubleword is stored, starting at byte address 304. The next channel to main storage cycle is allowed to pass; then, another request is made. This continues until the four doublewords have been stored.

In the test mode, with the log-on-machine-check switch down, the channel stops when it detects a machine check or a data check. The logout function is further explained in the Maintenance Features section.

A channel machine check includes the following:

1. Storage data check: Main storage detected a parity check on the CAW or CCW sent to the channel.
2. Storage address check: Main storage detected a parity check on the address or mark parity or the protection keys sent by the channel.
3. Unit address check: The unit address on the I/O bus out had incorrect parity.
4. Command check: The command on the I/O bus out had incorrect parity.
5. Byte counter check: The byte counter predicted parity and actual parity do not agree in either the main channel or one of the selector subchannels.
6. Unit control word check: The channel detected a parity check on the control register when it was stored in local storage.
7. Local storage address check: The address used by local storage had incorrect parity.
8. Priority check: The main channel priority circuits gave priority to a subchannel not requesting it, or the requesting subchannel failed to stop requesting priority after receiving it.
9. Channel timeout: The CPU had not been released an abnormal time after issuing select channel.
10. Address-in check: The channel detected a parity check on the address received from the device, following request in.
11. Status-in check: The channel detected a parity check on the status received from the device.
12. Incorrect selection: The address received from an I/O unit during initial selection does not agree with the address sent from the channel.
13. No response: The I/O unit did not respond to address out for reselection during a chain command operation.
14. Incorrect tag sequence: The selected I/O unit dropped its operational-in line before the channel dropped the select-out line.

Checks 1-8 turn on the channel control check trigger; checks 9-14 turn on the interface control check trigger.

Detection of checks 3 and 7-10 or detection of any second check during logout causes a full reset of the 2870 and any attached control units after completion of the logout.

A data check includes the following:

1. Storage data bus-in parity check: The channel detected a parity error on the data sent to main storage.
2. Storage data check: Main storage detected a parity error on the data sent to, or fetched from, main storage.
3. Bus-in parity check: Data on the I/O bus-in had incorrect parity.
4. Bus-out parity check: Data on the I/O bus-out had incorrect parity.

Note: Channel logout words are stored in main storage only when the 2870 is in the auto mode. In test mode, the logout words are stored in local storage only.

CE Console Pushbuttons

Reset (N18): If the log-on-machine-check switch is up (off), this pushbutton causes all channel registers and triggers (except the simulate I/O registers and SSC byte counter) to be reset and resets all local storage words to 0 with correct parity.

If the log-on-machine-check switch is down (on), all channel registers and triggers (except the simulate I/O registers and SSC byte counter) are reset, but the contents of local storage are not disturbed.

For either position of the log-on-machine-check switch, all attached I/O units are also reset if the simulate I/O switch is off.

Clear Interrupt (N19): This pushbutton simulates the interrupt response line from the CPU in answer to an interrupt request from the channel. It is used when an interruption is outstanding in the channel.

Load Data Address (N16): This pushbutton causes switches L10-36 to be gated to the control register. However, only switches L10-33 should be used, because the channel addresses main storage on doubleword boundaries. When a manual store or fetch operation is performed, the contents of the data address are gated to the storage address bus, determining the location addressed in storage. At the completion of the storage operation, the data address is incremented by eight bytes. When the maximum storage address is reached, the address wraps around to zero and continues. If the continuous storage cycle switch is down, the address is not incremented.

Local Store (N12): This pushbutton, in conjunction with the load/fetch toggle switch, initiates a local-store load or fetch. In either case, the local-store address is that contained in the unit address and local storage address modifier switches.

During the load operation, the contents of the simulate storage bus-out switches are gated to the data register and from the data register to local storage.

During a fetch operation, the contents of the local storage location specified replace the contents of the control register unless local storage address modify switch 8 is off and switch 9 is on. In this case, the word is fetched to the data register and then gated to the control register for display. In either case, the contents of the local storage word fetched are automatically restored.

Main Store (N14): This pushbutton, with the load/fetch switch, initiates a main storage load or fetch. In either case, the main storage address is that contained in bytes 1-3 of the control register (data address).

During the load operation, the contents of the simulate storage bus-out switches are gated to the data register. The contents of the data register are gated to the storage data bus-in and stored in the location specified by the contents of the data address.

During a manual (single-cycle) fetch operation, a doubleword of information is fetched from the storage location specified by the data address, placed in the data register, and then gated to the control register for display. It is necessary to load the data address again in order to perform another data fetch. If the continuous storage cycle switch is down, the address is not incremented, and the data register contents are not gated to the control register for display.

Test I/O (N23): This pushbutton permits the channel to issue a test I/O command to a connected I/O device or to simulate the test I/O sequence within the channel.

If the channel is in test mode and not simulating I/O, the unit address switches are sent to the initial unit address register to determine which I/O unit is selected. When the instruction is completed, the channel is in the interrupt state, with the I/O unit status in local storage.

If the channel is simulating I/O, the channel's manual controls simulate an I/O unit, responding to the test I/O command with a status byte containing no status bits.

Start I/O (N25): This pushbutton simulates the issuing of the start I/O instruction by the CPU. If the channel simulate storage switch is off, the instruction proceeds as a normal start I/O.

If the simulate storage switch is on, the channel does not fetch the CAW. Instead, a CCW is fetched from the channel switches. The unit address switches are gated to the initial unit address register. During the operation, the channel uses the switches to represent data or additional CCWs fetched from storage.

If a chain flag is set in the switches, the channel runs continuously. Otherwise, the channel ends with the interrupt queue full trigger (MSC) on or the interrupt pending trigger (SSC) on.

Halt I/O (N21): This pushbutton simulates the halt I/O instruction issued by the CPU and causes the addressed subchannel to stop its present operation, disconnects the I/O device, and turns on the interrupt queue trigger (MSC) or the interrupt pending trigger (SSC).

SECTION 3. MAINTENANCE FEATURES

LOGOUT (2870 and 2870A)

Logout is initiated by a channel control check or interface control check; channel status is not disturbed because the log sequence uses special circuitry. When the check occurs, if the log-on-machine-check switch is down, the channel stops, three doublewords (Figure 6-4) are stored in local storage, an interrupt request is sent to the CPU, and the channel continues to service other subchannels. When an interrupt response is received from the CPU, these three log words and a CSW are stored in main storage. The logout is performed as follows: A storage request is initiated and when honored, the first of the three log words is placed in main storage, starting at address 304. A channel to main storage cycle is allowed (could be a data store or fetch, or a chain command CCW fetch), and then the next doubleword is stored. This continues until all three log words and the CSW (location 64) are stored. The channel then continues to a normal end. If the log-on-machine-check switch is up, the log words and the CSW are stored in local storage and not in main storage.

Note: Logout in automatic mode does not occur unless one of the following occurs:

1. A start I/O, test I/O, or halt I/O to a busy channel is being executed at the time the logout condition occurs.
2. The CPU sends an interrupt response answer to the channel interrupt request.
3. A test I/O instruction is issued to a device that has an outstanding interrupt request.

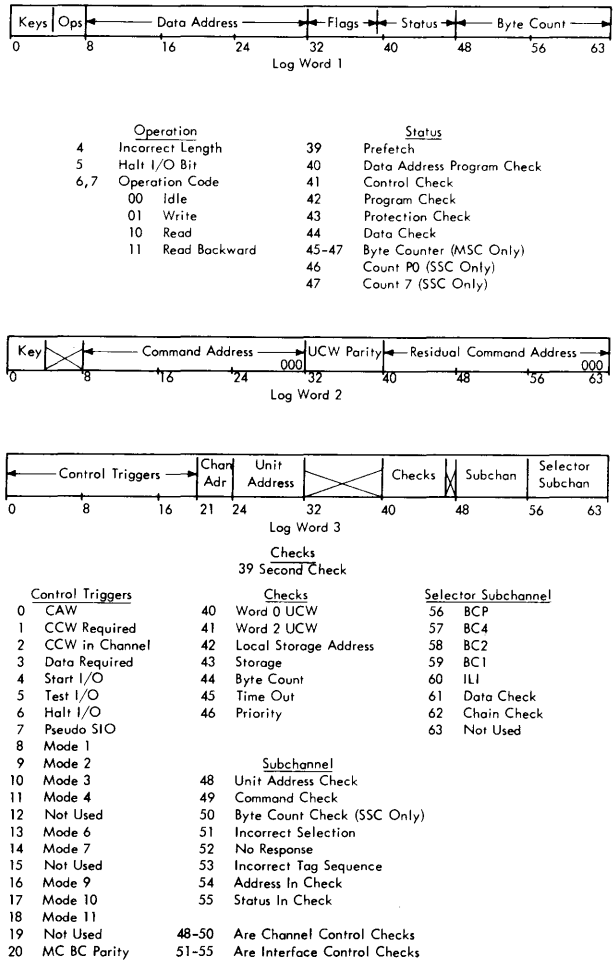


Figure 6-4. Log Words (2870 and 2870A)

The errors that turn on channel control check (CCC) are:

1. Storage Data Check -- Main storage detected a parity error on the CAW or CCW sent to the 2870.
2. Storage Address Check -- Main storage detected a parity error on the address, mark bits, or protection key sent by the 2870.
3. Unit Address Check -- The device address on the I/O bus out had incorrect parity.
4. Command Check -- The I/O command on the I/O bus out had incorrect parity.
5. Byte Counter Check -- A byte counter's predicted and actual parity do not agree in either the main channel or one of the SSCs.
6. Unit Control Word Check -- The main channel detected a parity error on the contents of the control register when it was stored in local storage.
7. Local Storage Address Check -- A parity error occurred on a local storage address.
8. Priority Check -- Main channel's priority circuit gave priority to a unit not requesting it, or the requesting unit failed to drop the request when priority was granted.

The errors that turn on interface control check (IFCC) are:

1. Channel Time-Out -- After CPU raised select channel, either the main channel was busy for more than 16 ms or the initial selection of the I/O device took more than 16 ms.
2. Address-In Check -- The 2870 detected a parity error on the address received from an I/O device after 'request in.'
3. Status-In Check -- The 2870 detected a parity error on the status byte received from an I/O device.
4. Incorrect Selection -- The address received from an I/O device during initial selection did not match the address sent out by the 2870.

5. No Response -- The I/O device did not answer 'address out' sent during the device reselection sequence for a chain command operation.

6. Incorrect Tag Sequence -- A selected I/O device dropped its 'operational-in' line before the 2870 dropped the 'select out' line.

For the logout sequence, the preceding errors are regrouped as either a type I or type II error. This regrouping does not change the definition of the error indications. The type I errors are considered recoverable, and the channel indications are first logged into local storage. When CPU is available, the log words are sent to main storage between data or CCW cycles. The type II errors require that the 2870 be machine reset at the end of the logout. Therefore, local storage is not used, logout proceeds as fast as possible, other subchannel operations are blocked, and a full reset of the 2870 and all attached I/O devices occurs after the logout.

Type I errors are:

Storage Data Check (CCC)
Storage Address Check (CCC)
Command Check (CCC)
Byte Counter Check (CCC)
Unit Control Word Check (CCC)
Status-In Check (IFCC)
Incorrect Selection (IFCC)
No Response (IFCC)
Incorrect Tag Sequence (IFCC)

Type II errors are:

Unit Address Check (CCC)
Local Storage Address Check (CCC)
Priority Check (CCC)
Channel Time Out (IFCC)
Address-In Check (IFCC)
Any-Second Error During a Logout (IFCC or CCC)

Log Word Definitions (2870 and 2870A)

Figure 6-4 shows the format of the three log words. Log word numbering, local storage assignments, and contents are:

Log Word	Stored in UCW	Contents
1	0	UCW 0
2	3	UCW 2
3	1	Control triggers and Check Indications

Log Word 1 (Figure 6-4) is the equivalent of UCW 0 and is logged into local storage word 0 of the device which caused the error. The byte count (Bytes 6 and 7) is not adjusted for actual bytes transferred. Bit 41 indicates a main channel control check, and is not present for a subchannel detected control check. Log word 1 is invalid if log word 3 indicates a word 2 UCW check in bytes 1, 2, or 3, a storage check, and a CCW required.

Log Word 2 is the equivalent of UCW 2, and is logged into local storage word 3 of the device which caused the error. Byte 4 indicates which byte had bad parity if log word 3 indicates either a word 0 or a word 2 UCW check. If log word 3 indicates a storage check and CAW trigger, byte 5 of log word 2 indicates the following checks (rather than the residual command address):

Bit	Means
41	Control Check
42	Program Check
43	Protect Check
44	Data Check

Log Word 3 contains operational triggers and latches that are useful in determining what sequence was being performed when the error occurred. These triggers and latches can be grouped as follows:

Bits 0-18 are main channel controls. Be careful in analyzing these indications because mode triggers 1-10 could break into the logout operations under control of bits 1-7.

Bit 20 is the parity bit for the MSC byte counter.

Bits 20-31 are the channel and device address.

Bits 39-46 are the detected main channel check conditions. Note: Bits 42, 45, and 46 are type II errors and only bits 20-31 and 40-46 are valid in this log word if they are on.

Bits 48-55 are subchannel errors. All except bit 50 (SSC only) can occur in either the MSC or the SSCs.

Bits 56-63 are SSC conditions. Bits 56-59 are the byte count latches, and 60-62 are SSC errors that do not cause a logout.

Logout Operations (2870 and 2870A)

This section describes the channel operations that occur if a logout is performed. With the 2870 in auto mode there are four ways to handle a machine check (IFCC or CCC). The manner in which an

error is handled depends on the position of the log-on-machine-check switch and the type (I or II) of error that occurs. The logout circuits are also active if the auto/test switch is in the test position and the log-on-machine-check switch is off. In this case, the log words only appear in local storage. Logout operation descriptions follow. Details of the logout operation are in the flow charts in the 2870 FE Diagram Manual.

Log Switch On and Type I Error (2870 and 2870A)

If the log-on-machine-check switch is on and a type I error occurs, the 2870 logs in three doublewords of logout information into local storage words 0, 1, 3 of the subchannel which detected the error. Data transfers by other subchannels are then allowed. When requests for data transfers are exhausted and either 'interrupt response' is granted by CPU or a 'test I/O' is issued to the subchannel with the error, or if the error occurred during a CPU instruction other than test channel, the three log words are stored in main storage one at a time; a CSW is stored at location 64 and CPU is released. Between the main storage cycles for the log words, other subchannels are allowed to transfer data.

A type I error with the log-on-machine-check switch on and the auto/test switch in auto, turns on the log in 1 latch (FC661). The main channel clock is turned off and control trigger outputs are blocked to stop main channel operations at the place the error occurred. Any local or main storage cycles are allowed to complete. UCWs 0 and 2 are stored if they are in main channel. UCWs 1 and 3 are fetched with 'block' on (to reset them). The main channel clock is turned back on and control trigger and check indications are stored in UCW 1. UCW 1 will later be logged out as log word 3. UCW 2 is now fetched to both the control and data registers and the log in 2 latch is set.

Log in 2 (FC661) forms log words 1 and 2, signals the subchannel of the error condition and prepares for a CSW assembly. Log in 1 and the main channel clock are turned off. If the error is a UCW 0 check, UCW 0 is fetched into the control register and replaces the UCW 2 data. Log word 2 is stored from the data register (contains UCW 2) into UCW 3. If the error is a UCW check, byte 4 of log word 2 will contain the parity check indications from each byte of the control register.

UCW 0 is now fetched (FC661 & FC663) (unless already fetched), and the main channel clock is turned on. The subchannel address is gated from the UAOR to the logout register, error conditions are gated into the control register (log word 1), and the main channel control triggers are reset. Log word 1 is now stored in UCW 0 and the main channel check latches are reset. The 'log in process' latch is now set (remains on until logout is completed). If the error occurred during a CPU instruction prior to selecting the subchannel, 'log CSW cycle' is turned on and a trigger 7 sequence begins.

If the error was presented by the MSC or an SSC during a CSW cycle, 'log CSW cycle' is turned on and either trigger 5, 7, or 9 is set depending on conditions in the channel. If neither of the two preceding conditions exists, 'ending' is set and the logout circuits wait for the MSC or SSC to request a CSW cycle. Any CSW cycle request will turn on 'log compare.'

'Log compare' (FC653) is used to determine if the subchannel requesting a CSW cycle is the one stopped due to the logout, or if a second machine check has occurred. 'Log compare' is set by 'CSW cycle request' and 'log in process.' The logout register is compared to the UAOR, and if equal, 'log CSW cycle' is set and a trigger 5, 7, or 9 sequence is begun, depending upon main channel conditions. If the addresses do not compare and 'log line' is not active, a normal CSW cycle occurs. If the addresses do not compare and 'log line' is active, this is a second machine check condition. A second machine check causes a bypass of the CSW cycle, sets the 'log CSW complete,' 'freeze,' and 'not status cycle' latches, and the logout proceeds without interruptions.

During logout a CSW is formed under triggers 5-6, 7, or 9-10 with 'log CSW cycle' on. For the trigger 5-6 sequence, 'log CSW cycle' causes 'log CSW complete' to be set at the end of trigger 6 and blocks 'release' or 'ending.' During trigger 7, 'log CSW cycle' causes UCW 0 to be saved in local storage, the CSW to be stored in main storage directly from the control register (before the storing of the three log words), 'release' is prevented, and 'log CSW complete' and 'log CSW stored' are set. During the trigger 9-10 sequence, 'log CSW cycle' prevents the turn-on of 'queue full,' 'ending,' and 'release.' At the end of trigger 10 it causes 'log CSW complete' to be set.

The 'log CSW complete' sequence (FC665) is used to determine whether the logout can occur under an existing CPU instruction or if an interrupt must be requested. Trigger 6, 7, 10 and 'log CSW cycle' are reset, and the main channel clock is turned on. If a CPU instruction was in process for the subchannel when the error occurred, 'log requires response' is set. If no instruction is available, 'log interrupt required' is set. For either case, 'log first word' and 'ending' are set. At this time, the local storage contains three log words and (usually) a CSW. If 'freeze' is not on, the log circuits now

release the priority circuits for other subchannels' data transfers.

'Log requires response' is used to make 'CPU priority request' active to the main channel priority circuits. This is the log circuit priority request level. The log circuits release the priority circuit after each log word is stored in main storage so that all outstanding subchannel requests can be serviced before logging out the next word. Once turned on, 'log requires response' remains on until the log CSW word sequence has begun.

'Freeze' blocks all priority requests, except the log circuits. To allow the log circuits to ignore the status of the freeze latch, the priority circuits still generate the response delayed pulse. As soon as 'ending' is turned on at the end of each log sequence, an immediate 'response delayed' pulse turns on the following log sequence. 'Freeze' also indicates that a machine reset will occur at the completion of the logout. Once turned on, 'freeze' remains on until the machine is reset.

'Log interrupt required' is used to raise 'CPU interrupt request.' The CPU answer, 'CPU interrupt response,' is blocked from reaching the interrupt queue register or the SSCs. This gives the log sequences priority over other outstanding 2870 interrupts. If 'CPU interrupt response' becomes active, 'log first word' is set (FC671). If 'freeze' is on and any instruction except test channel arrives, 'log requires response' is set to force a 'CPU response' from the priority circuits; 'log first word is set.' If a test I/O instruction arrives and 'freeze' is off (FC665), the device address is compared with the logout register contents. Equal addresses set 'log requires response' and 'ending'; the test I/O clears the logout interrupt. If the addresses do not compare (FC665), 'log TI/O no compare' is set and the test I/O proceeds normally; the logout interrupt remains pending.

'Log first word' is used to store log word 1 (UCW 0) into main storage (FC671). 'CPU interrupt response' and 'log interrupt required,' or 'CPU response' from the priority circuits and 'log requires response' turn on 'log first word.' UCW 0 is fetched. 'Log requires response' is set (if not on) and 'log interrupt required' is reset. A main storage cycle is performed to store log word 1 at location 304 (130 hex). When the main storage cycle is over, 'log second word' and 'ending' are set. Data transfers from other subchannels can now occur.

'Log second word' (FC671) is used to store log word 2 (UCW 3) into main storage. 'CPU priority response' and 'response delayed,' fetch UCW 3 and reset 'log first word.' A main storage cycle is performed to store log word 2 at location 312 (138 hex). When the main storage cycle is over, 'log third word' and 'ending' are set. Data transfers for other subchannels can now occur.

'Log CSW word' (FC673) is used to store the CSW associated with the machine check (IFCC or CCC) and to release the CPU. 'CPU priority response' and 'response delayed,' fetch UCW 2 and reset 'log third word.' A main storage cycle is performed to store the CSW at location 64 (40 hex). If 'no status cycle' is on, indicating that for some reason a CSW was not formed, the control check (bit 45) is forced on the SBI and the transfer of the control register contents to the SBI is blocked. If 'log CSW stored' is on, indicating that some previous sequence stored the CSW, a CSW is not stored at this time. When the CSW storage cycle is over, 'log requires response,' 'SSC interrupt pending,' and 'log CSW stored' are reset, and UCW 0 is fetched. The op code field is reset (bits 6, 7) and UCW 0 is stored. CPU is released with condition code 00 if 'CPU interrupt response' is active, or condition code 01 if 'CPU select channel' is active. If the 'freeze' latch is off, 'log CSW word' and 'log in process' are reset, and 'ending' is set; the logout is complete. If the 'freeze' latch is on, indicating a second check condition, the entire 2870 including local storage and all attached I/O devices are reset.

Log Switch On and Type II Error (2870 and 2870A)

If the log-on-machine-check switch is on and a type II error occurs, the 2870 stops all data transfers and raises 'interrupt request' to the CPU. Upon receiving 'interrupt response' or any instruction other than test channel, the 2870 logs out three doublewords into main storage. These words only contain the following information:

Log Word 1	Channel control check or Interface control check.
Log Word 2	Blank.
Log Word 3	Unit address and type of error.

The 2870 then stores a CSW with the interface control check or channel control check bit and releases CPU. The address sent to the CPU on the UABI is whatever is in the UAOR (with good parity). After the logout interrupt is completed, the 2870 performs a complete reset of everything including local storage, and all attached I/O devices.

The pseudo log 1 sequence (FC681) is used to request an interrupt (if necessary) and to store log words 2 and 3 in main storage. In this log sequence, the status of local storage words is ignored, all operations are stopped, and logout proceeds with a minimum amount of information logged out. The main channel clock is turned off, control trigger outputs are blocked, and any active local storage or main storage cycles are allowed to end. The control register is reset, and if any instruction other than test channel is in process in the channel, a main storage request is made to store log word 2 at location 312 (138 hex). This log word contains all zeros. If there is no instruction in process, 'log interrupt required' is turned on. Either a 'CPU interrupt response' or an instruction other than test channel issued to any device address on the 2870 causes a store of log word 2 in main storage. In either case, 'freeze' is turned on and 'log interrupt required' is turned off. When the main storage cycle is over (FC683), a main storage request is made to store log word 3 at location 320 (140 hex), and 'pseudo log 2' is turned on. The only information stored in log word 3 is an address from the UAOR and the check triggers.

'Pseudo log 2' (FC683) is used to store log word 1 in main storage. 'Pseudo log 1' is turned off. When the main storage cycle for log word 3 is completed, the control register is reset and a main storage request is made to store log word 1 at location 304 (130 hex). If the control check latch is on, bit 41 is forced on the SBI at this time and the channel control check status trigger is set. If a time out error occurred, the interface control check status trigger is set. These status triggers are used to generate the CSW. 'Pseudo log 3' is turned on.

The 'pseudo log 3' sequence (FC685) is used to store a CSW in main storage and release the CPU. 'Pseudo log 2' is turned off, the control register is reset, and the channel status latches are gated into byte 5 of the control register. A main storage request is made to store the CSW at location 64 (40 hex). When the main storage cycle is over, the CPU is released with condition code 00 (CPU interrupt response active) or 01 (CPU select channel active). After the CPU is released, the entire 2870, including local storage and all attached I/O devices, is reset.

Log Switch Off and Type I Error (2870 and 2870A)

A type I error causes 'log in 1' to be set. A log in (assembly of log words in local storage) proceeds in the same manner as if the log-on-machine-check switch were on, except that the 'store' line to BCU is blocked to prevent storing the three log words in main storage. The CSW is stored in location 64 (40 hex). For details of the log word formation, see the Log Switch On and Type I Error section.

If the 2870 is in test mode and a type I error occurs during an instruction cycle (simulated CPU), the instruction is released, and the 'log in process' latch is turned off. Local storage contains the log words and the CSW. UCW 1 may have bad parity.

If the 2870 is in test mode and a type I error occurs after the instruction cycle, the log-in sequence completes, but the logout stops to wait for an 'interrupt response' or 'test I/O' to the unit address held in the logout register. At this time, UCW 0, 1, 3 represent the logout words as previously described, but may have bad parity. To complete the logout, set the unit address switches to the address in the logout register and depress the 'clear interrupt' or 'test I/O' pushbutton. This causes the 'log first word' (FC671) through 'log CSW word' (FC673) sequences to be completed. 'Log in process' is turned off. UCW 0, 1, 3 still contain the logout data, but UCWs 0 and 3 should have good parity. UCW 1 may still have bad parity.

Log Switch Off and Type II Error (2870 and 2870A)

A type II error with the log-on-machine-check switch off, turns on the pseudo log 1 latch and the 2870 proceeds as though the log switch were on. The only difference is that 'store' is blocked to BCU for the three log words. This occurs in either auto or test mode. At the completion of the 'pseudo log 3' (FC685) sequence, a machine reset is performed. Details of the pseudo log sequences can be found in the Log Switch On and Type II Error section.

LOGOUT (2870B)

Logout is initiated by a channel control check or interface control check; channel status is not disturbed because the log sequence uses special circuitry. When the check occurs, if the log-on-machine-check switch is down, the channel stops. three doublewords (Figure 6-5) are stored in local storage, and an interrupt request is sent to the CPU. When an interrupt response is received from the CPU, these three log words and a CSW are stored in main storage. The logout is performed as follows: A storage request is initiated and when honored, the first of the three log words is placed in main storage, starting at address 304 (130 hex). This continues until all three log words and the CSW (location 64) are stored. The channel then continues to a normal end. If the log-on-machine-check switch is up, the log words and the CSW are stored in local storage and not in main storage.

Note: Logout in automatic mode does not occur unless one of the following occurs:

1. A start I/O, test I/O, or halt I/O to a busy channel is being executed at the time the logout condition occurs.
2. The CPU sends an interrupt response answer to the channel interrupt request.

The errors that turn on channel control check (CCC) are:

1. Storage Data Check -- Main storage detected a parity error on the CAW or CCW sent to the 2870.
2. Storage Address Check -- Main storage detected a parity error on the address, mark bits, or protection key sent by the 2870.
3. Unit Address Check -- The device address on the I/O bus out had incorrect parity.
4. Command Check -- The I/O command on the I/O bus out had incorrect parity.
5. Byte Counter Check -- A byte counter's predicted and actual parity do not agree in either the main channel or one of the SSCs.
6. Unit Control Word Check -- The main channel detected a parity error on the contents of the control register when it was stored in local storage.
7. Local Storage Address Check -- A parity error occurred on a local storage address.
8. Priority Check -- Main channel's priority circuit gave priority to a unit not requesting it, or the requesting unit failed to drop the request when priority was granted.

The errors that turn on interface control check (IFCC) are:

1. Channel Time-Out -- After CPU raised select channel, either the main channel was busy for more than 8 seconds or the initial selection of the I/O device took more than 8 seconds.
2. Address-In Check -- The 2870 detected a parity error on the address received from an I/O device after 'request in'.
3. Status-In Check -- The 2870 detected a parity error on the status byte received from an I/O device.
4. Incorrect Selection -- The address received from an I/O device during initial selection did not match the address sent out by the 2870.
5. No Response -- The I/O device did not answer 'address out' sent during the device reselection sequence for a chain command operation.
6. Incorrect Tag Sequence -- A selected I/O device dropped its 'operational-in' line before the 2870 dropped the 'select out' line.

For the logout sequence, the preceding errors are regrouped as either a type I or type II error. This regrouping does not change the definition of the error indications. For type I errors, the indications are first logged into local storage. When the CPU is available, the log words are then sent to main storage. For type II errors, local storage is not used, logout proceeds as fast as possible, and all other subchannel operations are blocked.

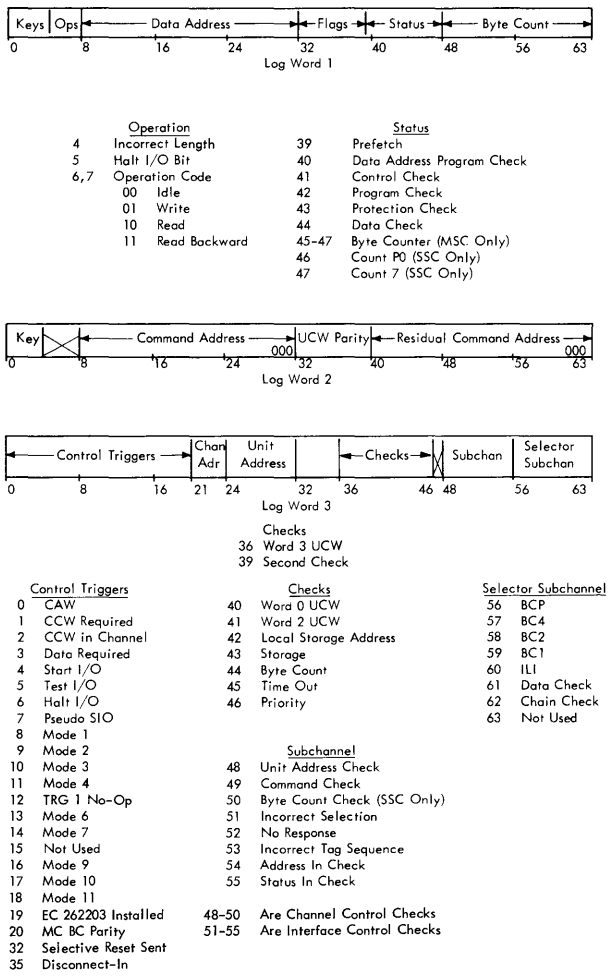


Figure 6-5. Log Words (2870B)

Type I errors are:

Storage Data Check (CCC)
Storage Address Check (CCC)
Command Check (CCC)
Byte Counter Check (CCC)
Unit Control Word Check (CCC)
Status-In Check (IFCC)
Incorrect Selection (IFCC)
No Response (IFCC)
Incorrect Tag Sequence (IFCC)

Type II errors are:

Unit Address Check (CCC)
Local Storage Address Check (CCC)
Priority Check (CCC)
Channel Time Out (IFCC)
Address-In Check (IFCC)
Any-Second Error During a Logout (IFCC or CCC)

Log Word Definitions (2870B)

Figure 6-5 shows the format of the three log words. Log word numbering, local storage assignments, and contents are:

Log Word	Stored in UCW	Contents
1	0	UCW 0
2	3	UCW 2
3	1	Control triggers and Check indications

Log Word 1 (Figure 6-5) is the equivalent of UCW 0 and is logged into local storage word 0 of the device which caused the error. The byte count (bytes 6 and 7) is not adjusted for actual bytes transferred. Bit 41 indicates a main channel control check, and is not present for a subchannel detected control check. Log word 1 is invalid if log word 3 indicates a word 2 UCW check in bytes 1, 2, or 3, a storage check, and a CCW required.

Log Word 2 is the equivalent of UCW 2, and is logged into local storage word 3 of the device which caused the error. Byte 4 indicates which byte had bad parity if log word 3 indicates either a word 0 or a word 2 UCW check. If log word 3 indicates a storage check and CAW trigger, byte 5 of log word 2 indicates the following checks (rather than the residual command address):

Bit	Means
41	Control Check
42	Program Check
43	Protect Check
44	Data Check

Log Word 3 contains operational triggers and latches that are useful in determining what sequence was being performed when the error occurred. These triggers and latches can be grouped as follows:

Bits 0-18 are main channel controls. Be careful in analyzing these indications because mode triggers 1-10 could break into the logout operations under control of bits 1-7.

Bit 20 is the parity bit for the MSC byte counter.

Bits 20-31 are the channel and device address.

Bits 39-46 are the detected main channel check conditions. Note: Bits 42, 45, and 46 are type II errors and only bits 20-31 and 40-46 are valid in this log word if they are on.

Bits 48-55 are subchannel errors. All except bit 50 (SSC only) can occur in either the MSC or the SSCs.

Bits 56-63 are SSC conditions. Bits 56-59 are the byte count latches, and 60-62 are SSC errors that do not cause a logout.

Logout Operations (2870B)

This section describes the channel operations that occur if a logout is performed. With the 2870 in auto mode there are four ways to handle a machine check (IFCC or CCC). The manner in which an error is handled depends on the position of the log-on-machine-check switch and the type (I or II) of error that occurs. The logout circuits are also active if the auto/test switch is in the test position and the log-on-machine-check switch is off. In this case, the log words only appear in local storage. Logout operation descriptions follow. Details of the logout operation are in the flowcharts in the 2870 FE Diagram Manual.

Log Switch On and Type I Error (2870B)

If the log-on-machine-check switch is on and a type I error occurs, the 2870 logs in three doublewords of logout information into local storage words 0, 1, 3 of the subchannel which detected the error.

If the error occurred during a CPU instruction other than test channel, the three log words are stored in main storage one at a time; a CSW is stored at location 64 and CPU is released.

A type I error with the log-on-machine-check switch on and the auto/test switch in auto, turns on the log in 1 latch (FC661). The main channel clock is turned off and control trigger outputs are blocked to stop main channel operations at the place the error occurred. Any local or main storage cycles are allowed to complete. UCWs 0 and 2 are stored if they are in main channel. UCWs 1 and 3 are fetched with 'block' on (to reset them). The main channel clock is turned back on and control trigger and check indications are stored in UCW 1. UCW 1 will later be logged out as log word 3. UCW 2 is now fetched to both the control and data registers and the log in 2 latch is set.

Log in 2 (FC661) forms log words 1 and 2, signals the subchannel of the error condition and prepares for a CSW assembly. Log in 1 and the main channel clock are turned off. If the error is a UCW 0 check, UCW 0 is fetched into the control register and

replaces the UCW 2 data. Log word 2 is stored from the data register (contains UCW 2) into UCW 3. If the error is a UCW check, byte 4 of log word 2 will contain the parity check indications from each byte of the control register.

UCW 0 is now fetched (FC661 and FC663) (unless already fetched), and the main channel clock is turned on. The subchannel address is gated from the UAOR to the logout register, error conditions are gated into the control register (log word 1), and the main channel control triggers are reset. Log word 1 is now stored in UCW 0 and the main channel check latches are reset. The 'log in process' latch is now set. If the error occurred during a CPU instruction prior to selecting the subchannel, 'log CSW cycle' is turned on and a trigger 7 sequence begins.

If the error was presented by the MSC or an SSC during a CSW cycle, 'log CSW cycle' is turned on and either trigger 5, 7, or 9 is set depending on conditions in the channel. If neither of the two preceding conditions exists, 'ending' is set and the logout circuits wait for the MSC or SSC to request a CSW cycle. Any CSW cycle request will fetch UCW 0, and if bit 41 is on, the LOG CSW latch is set.

During logout a CSW is formed under triggers 5-6, 7, or 9-10 with 'log CSW cycle' on. For the trigger 5-6 sequence, 'log CSW cycle' causes 'log CSW complete' to be set at the end of trigger 6 and blocks 'release' or 'ending.' During trigger 7, 'log CSW cycle' causes UCW 0 to be saved in local storage, the CSW to be stored in main storage directly from the control register (before the storing of the three log words), 'release' is prevented, and 'log CSW complete' and 'log CSW stored' are set. During the trigger 9-10 sequence, 'log CSW cycle' prevents the turn-on of 'queue full,' 'ending,' and 'release.' At the end of trigger 10 it causes 'log CSW complete' to be set.

The 'log CSW complete' sequence (FC665) is used to determine whether the logout can occur under an existing CPU instruction or if an interrupt must be requested. Triggers 6, 7, 10 and 'log CSW cycle' are reset, and the main channel clock is turned on. If a CPU instruction was in process for the subchannel when the error occurred, 'log requires response' is set. If no instruction is available, 'log interrupt required' is set. For either case, 'log first word' is set. At this time, local storage contains three log words and (usually) a CSW. No other subchannel requests are allowed until the log interrupt is cleared. For any CPU instruction except test channel, a log pending CSW (only bits 5 and 45 on) is stored, and a condition code of 01 is sent to the CPU.

'Log requires response' is used to make 'CPU priority request' active to the main channel priority circuits. This is the log circuit priority request level.

'Freeze' blocks all priority requests, except the log circuits. To allow the log circuits to ignore the status of the freeze latch, the priority circuits still generate the response delayed pulse. As soon as 'ending' is turned on at the end of each log sequence, an immediate 'response delayed' pulse turns on the following log sequence.

'Log interrupt required' is used to raise 'CPU interrupt request.' The CPU answer, 'CPU interrupt response,' is blocked from reaching the interrupt queue register or the SSCs. This gives the log sequences priority over other outstanding 2870 interrupts. If 'CPU interrupt response' becomes active, 'log first word' is set (FC671).

'Log first word' is used to store log word 1 (UCW 0) into main storage (FC671). 'CPU interrupt response' and 'log interrupt required,' or 'CPU response' from the priority circuits and 'log requires response' turn on 'log first word.' UCW 0 is fetched. 'Log requires response' is set (if not on) and 'log interrupt required' is reset. A main storage cycle is performed to store log word 1 at location 304 (130 hex). When the main storage cycle is over, 'log second word' is set.

'Log second word' (FC671) is used to store log word 2 (UCW 3) into main storage. 'CPU priority response' and 'response delayed,' fetch UCW 3 and reset 'log first word.' A main storage cycle is performed to store log word 2 at location 312 (138 hex). When the main storage cycle is over, 'log third word' is set. Data transfers for other subchannels can now occur.

'Log CSW word' (FC673) is used to store the CSW associated with the machine check (IFCC or CCC) and to release the CPU. 'CPU priority response' and 'response delayed,' fetch UCW 2 and reset 'log third word'. A main storage cycle is performed to store the CSW at location 64 (40 hex). If 'no status cycle' is on, indicating that for some reason a CSW was not formed, the control check (bit 45) is forced on the SBI and the transfer of the control register contents to the SBI is blocked. If 'log CSW stored' is on, indicating that some previous sequence stored the CSW, a CSW is not stored at this time. When the CSW storage cycle is over, 'log requires response,' 'SSC interrupt pending,' and 'log CSW stored' are reset, and UCW 0 is fetched. The op code field (bits 6 and 7) and status field is reset, and UCW 0 is stored. CPU is released with condition code 00 if 'CPU interrupt response' is active, or condition code 01 if 'CPU select channel' is active. 'Log CSW word' and 'log in process' are reset, and 'ending' is set; the logout is complete.

Log Switch On and Type II Error (2870B)

If the log-on-machine-check switch is on and a type II error occurs, the 2870 stops all data transfers and raises 'interrupt request' to the CPU. Upon receiving 'interrupt response' or any instruction other than test channel, the 2870 logs out three doublewords into main storage. These words only contain the following information:

Log Word 1	Channel control check or interface control check.
Log Word 2	Blank.
Log Word 3	Unit address and type of error.

The 2870 then stores a CSW with the interface control check or channel control check bit and releases CPU. The address sent to the CPU on the UABI is whatever is in the UAOR (with good parity).

The pseudo log 1 sequence (FC681) is used to request an interrupt (if necessary) and to store log words 2 and 3 in main storage. In this log sequence, the status of local storage words is ignored, all operations are stopped, and logout proceeds with a minimum amount of information logged out. The main channel clock is turned off, control trigger outputs are blocked, and any active local storage or main storage cycles are allowed to end. The control register is reset, and if any instruction other than test channel is in process in the channel, a main storage request is made to store log word 2 at location 312 (138 hex). This log word contains all zeros. If there is no instruction in process, 'log interrupt required' is turned on. A 'CPU interrupt response' causes the 2870 to store log word 2 into main storage. In either case, 'freeze' is turned on and 'log interrupt required' is turned off. When the main storage cycle is over (FC683), a main storage request is made to store log word 3 at location 320 (140 hex), and 'pseudo log 2' is turned on. The only information stored in log word 3 is an address from the UAOR and the check triggers.

'Pseudo log 2' (FC683) is used to store log word 1 in main storage. 'Pseudo log 1' is turned off. When the main storage cycle for log word 3 is completed, the control register is reset and a main storage request is made to store log word 1 at location 304 (130 hex). If the control check latch is on, bit 41 is forced on the SBI at this time and the channel control check status trigger is set. If a time out error occurred, the interface control check status trigger is set. These status triggers are used to generate the CSW. 'Pseudo log 3' is turned on.

The 'pseudo log 3' sequence (FC685) is used to store a CSW in main storage and release the CPU. 'Pseudo log 2' is turned off, the control register is reset, and the channel status latches are gated into byte 5 of the control register. A main storage request is made to store the CSW at location 64 (40 hex). When the main storage cycle is over, the CPU is released with condition code 00 (CPU interrupt response active) or 01 (CPU select channel active). After the CPU is released, 'ending' is turned on and the priority circuits are interrogated.

Log Switch Off and Type I Error (2870B)

A type I error causes 'log in 1' to be set. A log in (assembly of log words in local storage) proceeds in the same manner as if the log-on-machine-check switch were on, except that the 'store' line to BCU is blocked to prevent storing the three log words in main storage. The CSW is stored in location 64 (40 hex). For details of the log word formation, see the Log Switch On and Type I Error section.

If the 2870 is in test mode and a type I error occurs during an instruction cycle (simulated CPU), the instruction is released, and the 'log in process' latch is turned off. Local storage contains the log words and the CSW. UCW 1 may have bad parity.

If the 2870 is in test mode and a type I error occurs after the instruction cycle, the log-in sequence completes, but the logout stops to wait for an 'interrupt response'. At this time, UCWs 0, 1, 3 represent the logout words as previously described, but may have bad parity. To complete the logout, depress the 'clear interrupt' pushbutton. This causes the 'log first word' (FC671) through 'log CSW word' (FC673) sequences to be completed. 'Log in process' is turned off. UCWs 0, 1, 3 still contain the logout data, but UCWs 0 and 3 should have good parity. UCW 1 may still have bad parity.

Log Switch Off and Type II Error (2870B)

A type II error with the log-on-machine-check switch off, turns on the pseudo log 1 latch and the 2870 proceeds as though the log switch were on. The only difference is that 'store' is blocked to BCU for the three log words. This occurs in either auto or test mode. At the completion of the 'pseudo log 3' (FC685) sequence, 'ending' is turned on. Details of the pseudo log sequences can be found in the Log Switch On and Type II Error section.

DIAGNOSE

Diagnose performs dynamic tests of all checking circuits in the 2870 under control of the MCW. The same signal to proceed, sent to the CPU by the MCW, affects the channel as follows: the channel is selected for diagnostic action by bits 0-2 of the MCW. Channels 0-6 are selected in binary fashion; that is, 000 is channel 0, 001 is channel 1, etc.

The select line to the multiplexer channel also conditions the simulate interface line. The simulate interface line permits the channel to operate without communicating with a device, control unit, or even having one connected to the I/O interface. The interface controls are operated at their upper limit, while all operations within the channel appear normal. There is also a nine-bit simulate data register between the interface bus out and bus in that receives the bytes sent over bus out during a write operation. It retains the last byte written and sends it over bus in during a read operation.

Diagnose action is initiated by the following bit positions of the MCW:

Position 3: When a channel is selected, the parity bit from the simulate data register is reversed, allowing an invalid byte to be brought into the channel on bus in. This function may also be used to correct bad parity sent from the channel on bus out to the simulate data register.

Position 4: Causes data transfer between main storage and local storage in the selected channel. This provides a means of checking local storage.

Position 5: Causes a selected channel to block the setting of a (storage data) control error while fetching a CCW or data. This function allows invalid CCWs to be brought into the channel to test sections of the channel's circuits.

Position 6: Affects only the CPU and is described in the appropriate processor maintenance manual.

Position 7: Must be on to select a channel with bits 0-2.

The 2870 diagnostic controls are used to perform four functions:

1. To test the channel checking circuits.
2. To test local storage.
3. To cause the channel to do a logout when an error occurs.
4. To store bytes with incorrect parity in storage. These bytes can be used to test the CPU or I/O unit checking circuits.

The diagnostic lines between the channel and CPU originate in the MCW. These lines are:

Diagnostic Select Channel (Bits 0-2 -- MCW): A simplex line that causes the channel to simulate the I/O interface and gates the multiplex diagnostic lines to the specified channel.

Reverse Data Parity (Bit 3 -- MCW): A multiplex line that causes a reversal of the parity bit coming out of the simulate I/O register to the bus in, and blocks the parity checking of the bus in.

Diagnostic Test Local Store (Bit 4 -- MCW): A multiplex line that causes data transfer between main storage and local storage in either direction. Note that this line is called 'reverse byte counter parity' at the interface.

Block Storage Data Check (Bit 5 -- MCW): A multiplex line that causes the channel to block the setting of a control check or data check because of incorrect parity on a CCW or data fetched from main storage and blocks the parity checking of the storage bus in.

When using diagnostic control lines, it is necessary to activate the appropriate diagnostic select channel line for the multiplex diagnostic lines to be effective. This line causes the selected channel to go into the simulate I/O mode. The simulate I/O register between the bus out and bus in becomes the source of data for a read operation, and retains the last byte written during a write operation.

To Load Incorrect Parity into Main Storage

1. Issue a write command to the channel. At the end of the operation, the simulate I/O register should contain a valid byte of data.
2. Raise the block storage data check line.
3. Raise the reverse data parity line.
4. Issue a read command to the channel.

The data transferred from the channel to main storage will have incorrect parity.

To Load Incorrect Parity into Local Storage

1. Raise the reverse data parity line.
2. Raise the block storage parity check line.
3. Raise the diagnostic test local store line.
4. Issue a start I/O instruction to the channel with incorrect parity in one or more bytes of the CCW. The bad parity will be stored in local storage.

Testing the Channel Parity Check Circuits

To Test the Unit Control Word Parity Check:

1. Raise the block storage parity check line.
2. Issue a start I/O instruction to the channel with incorrect parity in one byte of the CCW. The unit control word parity check consists of eight 8-bit parity checks. To check these circuits, it is necessary to issue separate instructions to test one byte at a time. The channel stores a CSW with the control check bit in the status byte. Byte 5 cannot be checked because bits 40-47 of the CCW are ignored.

To Test the Bus Out Parity Check:

1. Raise the block storage parity check line.
2. Issue a write command to the channel with incorrect parity in at least the last byte of data.
3. The channel ends the operation with a data check in the status byte and incorrect parity in the simulate I/O register.

To Test the Bus In Parity Check:

1. Raise the block storage parity check line.
2. Issue a read command to the channel. The simulate I/O register must contain incorrect parity.
3. The channel ends the operation with a data check in the status byte. The stored data should have incorrect parity.

To Test the Storage Data Bus In Parity Check:

1. Issue a write command to the channel. The data transferred from storage to the channel must have correct parity.
2. Raise the reverse data parity line.
3. Issue a read command to the channel. By using a count of one byte and varying the last three bits of the data address from 0-7, all eight storage bus in parity checks may be tested. The channel ends each operation with a data check in the status byte.

Testing Local Storage

Local storage is tested in the diagnostic mode by using a start I/O instruction. The following interface lines must be active:

Diagnostic select channel

Diagnostic test local store

Block storage data check

CPU select channel

Start I/O

The diagnostic lines must be active before the rise of CPU select channel.

The address on the unit address bus out determines the starting address to be checked in local storage. The UABO bits form the eight high-order bits of the ten bits needed to address local storage. Initially, the two low-order bits are 0. Local storage is addressed on double word boundaries; therefore, the programmer may start the test at address 0, or at any fourth doubleword thereafter. The address is incremented by one double word after each data transfer between main storage and local storage.

On receiving the start I/O instruction, the channel fetches a command address word (CAW) and a channel command word (CCW); the channel does not perform an I/O operation. The CAW and CCW must meet the requirements of their respective formats.

The CCW is interpreted as follows:

Command Field: This field must contain a read or write command. A write command causes the channel to fetch data from main storage and store it in local storage. A read command causes the channel to fetch data from local storage and store it in main storage.

Data Address Field: This field must contain an address on doubleword boundaries. The address specifies where data is to be stored in or fetched from main storage. The address is incremented by one doubleword after each transfer of data.

Flag Field: This field is ignored.

Count Field: The three low-order bits of this field must be 0. The count determines how many doublewords of local storage will be tested per CCW. A count of 8192 byte tests all local storage addresses. The count is decremented by eight bytes after each transfer of data. The testing of local storage continues until the count reaches 0, or until a channel control check or program check occurs.

Upon successful completion of the test, the channel releases the CPU with condition code 00. If a channel control check or program check occurs, the channel releases the CPU with condition code 01 and stores the channel status byte in location 64 of main storage.

Data is transferred from local storage to main storage without parity correction.

The fall of 'diagnostic select channel' causes the 2870 to do a complete reset.

Testing I/O Unit Parity Checking Circuits

When the channel is functioning properly, it is impossible to send a unit address or command with incorrect parity from the channel to the I/O unit. However, bytes of data with incorrect parity may be transferred by the channel from storage to the selected I/O unit. No diagnostic lines should be active during the operation. The channel ends the operation with a data check and unit check in the status bytes.

TEST I/O

The test I/O instruction causes a CSW to be stored when the tested device has conditions for interrupt (error or otherwise), either within the channel or stacked in the device. Normally, the instruction requests only device status, but, in the maintenance mode, it may be used to test existing error conditions in the device.

TEST CHANNEL

The test channel instruction requests the channel to send a condition code to the CPU describing present channel status, at which time the CPU is released.

EXTERNAL SYNC

An address compare sync pulse is brought into the channel as a fault detection aid. This line carries an approximately 200 ns pulse, when the storage address sent to the BCU by the channel matches the address set in the switches on the CPU console.

TIME CLOCK STEP PULSE

The time clock step pulse provides a timing signal for determining when an abnormally long CPU instruction or I/O selection sequence occurs (in auto mode) or for triggering the channel circuits in test mode. This pulse is approximately 200 ns and occurs every 16.7 ms (60 cycle). If the 2870 is in test mode and the auto restart switch is on, this pulse causes a reset of the channel every 16.7 ms (60 cycle). After the reset, a start I/O instruction is initiated and the channel executes the instruction until the next time clock step pulse. This pulse can also be used to provide repetitive triggering of singleshots for scoping and adjusting them.

STOP ON CONDITION AND STOP ON CHECK

In test mode with the log-on-machine-check switch in the down position, the 2870 will stop without a logout if a machine check or a data check occurs. The error may be detected in the main channel, the MSC, or a SSC. A master reset must be performed to clear the stop condition.

An error condition in either the main channel or a subchannel: blocks all control triggers, stops the main channel clock at the clock time the error is detected, blocks auto restart, and stops all subchannels by stopping the subchannel clocks and blocking the turn-off to service out or command out (if on). Any main storage or local storage cycles in progress are completed.

To condition the 2870 to stop on a machine check or data check in the auto mode, temporarily jumper pin 01A-B4C5D05 (MC651) to ground.

As a diagnostic aid, a condition other than a data check or a machine check can be wired to stop the machine. First, activate the stop-on-check condition by temporarily grounding pin 01A-B4C5D05 (MC651). Then temporarily jumper the minus signal that it is desired to stop on to pin 01A-C3K4D04 (MC463). When the wired condition occurs, the machine stops and the CE console can be used to help isolate the failure.

MARGINAL CHECKING

Marginal checking detects the marginal operation of voltage-sensitive circuits in the channel. The electronic circuits of the channel are designed to operate at nominal voltage level ratings. Examination of the operating characteristics at a voltage slightly above and slightly below the nominal voltage levels often yields information concerning present failures or possible future failures of the circuits. This information can be used to prevent failures because of aging and other factors that cause a gradual deterioration in the operating characteristics of the circuits. Marginal checking is, therefore, effective in locating existing, potential, and intermittent troubles and prevents costly machine downtime.

Channel Margins

The status of each channel frame 6M voltage can be monitored at the system control panel or by plugging a meter into jacks on the channel frame control panel. As there is only one 6M regulator for each channel frame, when a margin is applied, it is simultaneously applied to all subchannels in the frame. The 6M voltage levels can be margined on a per frame basis from the system control panel or channel frame.

When the channel frame is in local mode, margins can be applied only at the channel frame; when in remote mode, only at the system control panel. In either mode, margins can be monitored at both the system control panel and the channel frame. Indication of the 6M regulator in its margin status is sent to the system control panel. Indication of the 6M regulator being at the nominal or home position is also sent to the system control panel. Neither indication is shown at the channel frame.

Margins are applied by a motor-driven rheostat controlled by the raise/lower switch on the channel control panel. The rheostat is driven by the motor through a clutch. The clutch is picked by either a raise or lower signal to the motor. Limits are set by mechanical stops on the rheostat. When a limit is reached, the rheostat stops, but the motor continues to drive until the raise/lower switch is returned to the neutral position. When the clutch slips, it prevents damage to the motor. The rheostat is connected to the 6M regulator control circuit, causing the 6M volts to raise or lower. Marginal limits are +0. 5v and -0. 5v.

FLT

Fault locating tests (FLTs) provide the CE with the ability to test CPU circuits and controls. The FLT operation requires a large volume of data broken up into short tests. This data is on tape, and must be brought into storage without benefit of CPU instructions or interruptions. This means that the 2870 must work with the CPU FLT controls to supply the data, keep the FLT controls aware of progress, retry when errors are discovered, and start and stop data transmission (as directed by the FLT controls).

On the 2870, FLTs can only be entered through the selector subchannels. This is accomplished by placing the system in FLT mode and then handling the tape load as a normal IPL. In FLT mode, release IPL is issued at the end of tape record 2, but the operation continues. Record 2 causes the records that follow to be read into buffers 1 and 2, with a signal being sent to the FLT controls every time the 2870 encounters a TIC command. When the end of a record is reached, the incorrect record length indication is suppressed and a chain command CCW causes the next record to start loading buffer 1 again. A gap pulse is sent to the FLT controls during movement from one record to the next.

If a data error is discovered in the channel, a data error line is brought up to the FLT controls. The tape is backspaced by executing the command at main storage location 128 (the first command from tape record 2). This results in a restart of the error record. A control error activates a line, to the FLT controls, that signals the channel is unable to proceed.

The FLT controls can stop data transmission at any point in a record. A restart is accomplished by backspacing the tape as in error retry.

APPENDIX A. UNIT CHARACTERISTICS

Operating Speed:

Multiplex Subchannels (kilobytes)	Selector Subchannel 1 (kilobytes)	Selector Subchannel 2 (kilobytes)	Selector Subchannel 3 (kilobytes)	Selector Subchannel 4 (kilobytes)
110	0	0	0	0
88	180	0	0	0
66	180	180	0	0
44	180	180	180	0
30	180	180	180	100

Mode of Operation: Multiplex or burst

Power Requirements:

60 cycles (± 1 cps)	3 phase, 4 wire "delta" 208 or 230v + 10%, -8%
50 cycles (± 1 cps)	3 phase, 4 wire "delta" 195, 220, 235v + 10%, -8%
50 cycles (± 1 cps)	3 phase, 5 wire "wye" 380 or 408v + 10%, -8%

Environmental Conditions:

	Nonoperating	Operating
Temperature	50-110°F	60-90°F
Relative Humidity	8-80%	8-80%
Maximum Wet Bulb	80°F	78°F
Maximum Altitude	7,000 feet	7,000 feet

Cooling: Forced room air by single-phase blowers: two in each gate, and two in the power area.

Dimensions:

Height	5 feet, 10-3/4 inches
Width	2 feet, 8-1/4 inches
Depth	5 feet, 7-1/2 inches

REFERENCE VOLTAGE (V_{REF})

- Provides temperature-compensated voltage for current regulation.
- Maintenance data is in Field Engineering Maintenance Manual, IBM 2870 Multiplexer Channel, Form SY27-2302.

The reference voltage circuit provides temperature-compensated voltage to regulate the XY drive current.

A temperature-compensated voltage divider, consisting of resistors R1, R2, and R3, potentiometer P1, and thermistor RT, provides the input level to transistor T1 (Figure B-1). Transistor T1 serves as an emitter follower, and transistor T2 provides voltage regulation. Proper output voltage is obtained by adjusting potentiometer P1 at 77°F. Resistor R4 is the output load resistor, and capacitor C1 is for decoupling. The thermistor in the circuit is mounted on a memory core array card.

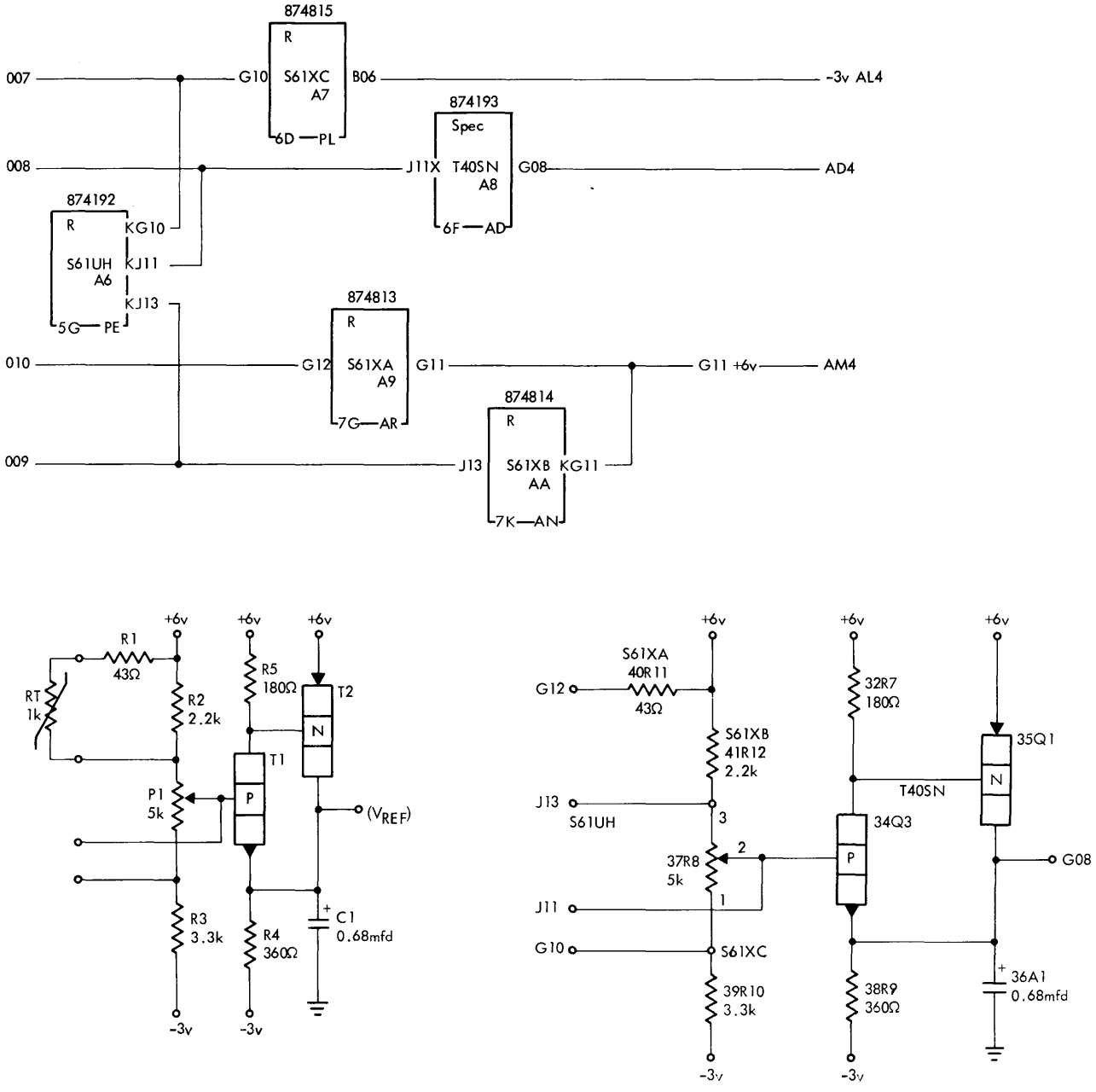


Figure B-1. Reference Voltage (V_{ref})

SENSE LEVEL (V_{SL})

- Provides voltage to emitter of second stage of the sense amplifier.
- Voltage is adjustable to distinguish between a minimum "1" and a maximum "0" (noise) signal.
- Maintenance data is in the maintenance manual.

The sense level circuit provides voltage to the emitter of the second stage of the sense amplifiers. This sense level voltage can be adjusted to distinguish between a minimum "1" and a maximum "0" (noise) signal. Because of changes in diode drops in transistors T1 and T2, the output voltage varies with the temperature. However, since the same type of transistors used in the sense amplifier are used in the sense level circuit, sensitivity of the sense amplifier remains constant.

Transistor T1 (Figure B-2) is a constant current sink, and the operating point of the transistor is established by resistors R1 and R2. Resistor R3 and potentiometer R4 determine the voltage drop in the collector circuit. Transistors T2, T3, T4, and T5 act as a constant current source, with T2 operating as a linear amplifier and T3, T4, and T5 serving as a constant current sink. The base voltage and output load resistor R6 determine the operating point of transistor T2. Resistors R7 and R8 control current in T3, T4, and T5. The amount of current drawn is determined by R7 and is limited by R8.

Changes in output current requirements and the voltage drop across load resistor R6 cause the collector operating point to change which tends to turn on transistor T3, thereby regulating the output voltage and current. Resistor R5 is the load for diode D1, and capacitor C1 is a decoupling for power supply noise.

SENSE AMPLIFIER

- The sense amplifier detects and amplifies a switched core output.
- The amplifier distinguishes between 1s and 0s.
- Maintenance data is in the maintenance manual.

The sense amplifier is a differential amplifier which detects and amplifies the output voltage of a switched memory core (Figure B-3). Diodes D1 and D2 form an OR gate which allows only the negative portion of the amplified sense signal to be applied to the base of transistor T3. Transistor T3 amplifies the signal and drives transistor T4 (the output transistor). A negative strobe pulse at diode D3 allows only the signal appearing at read time to be amplified by transistor T3.

The sense amplifier discriminates between 1s and 0s from memory, amplifying only those input voltages which are larger than a predetermined magnitude. The emitter of T3 is returned to the sense level voltage. The sense level voltage is adjusted to provide optimum discrimination between maximum noise and the minimum input signal which must be detected.

INHIBIT DRIVER

- The inhibit driver prevents the writing of a 1.
- The inhibit driver is driven by an AND inverter without a load (U03AD).
- The magnitude of the inhibit current is constant with temperature.
- Maintenance data is in the maintenance manual.

The inhibit driver prevents the writing of a 1 in memory by supplying current to the core array inhibit winding.

An AND inverter without a load (U03AD) is used to drive the inhibit driver. Transistor T1 is normally held off by resistor R2. When a negative pulse is applied to the base of T1 (input A1), the transistor acts as a constant current source and saturates transistor T2. The output of transistor T2 drives the inhibit winding of local storage. The magnitude of the inhibit current is constant with temperature. Special voltages +v and -v, shown in Figure B-4, are +3 volts and -3 volts, respectively.

STROBE DRIVER

- The strobe driver provides a timing gate (strobe) for the sense amplifiers.
- Strobe timing is adjustable.
- Maintenance data is in the maintenance manual.

The strobe driver circuit controls the gating of the sense amplifiers during a local storage read cycle. When the strobe pulse is active, the sense amplifiers can distinguish between 1s and 0s read from the array. When the strobe pulse is inactive, the sense amplifiers are deconditioned. Strobe timing is adjusted by a potentiometer on the strobe driver card.

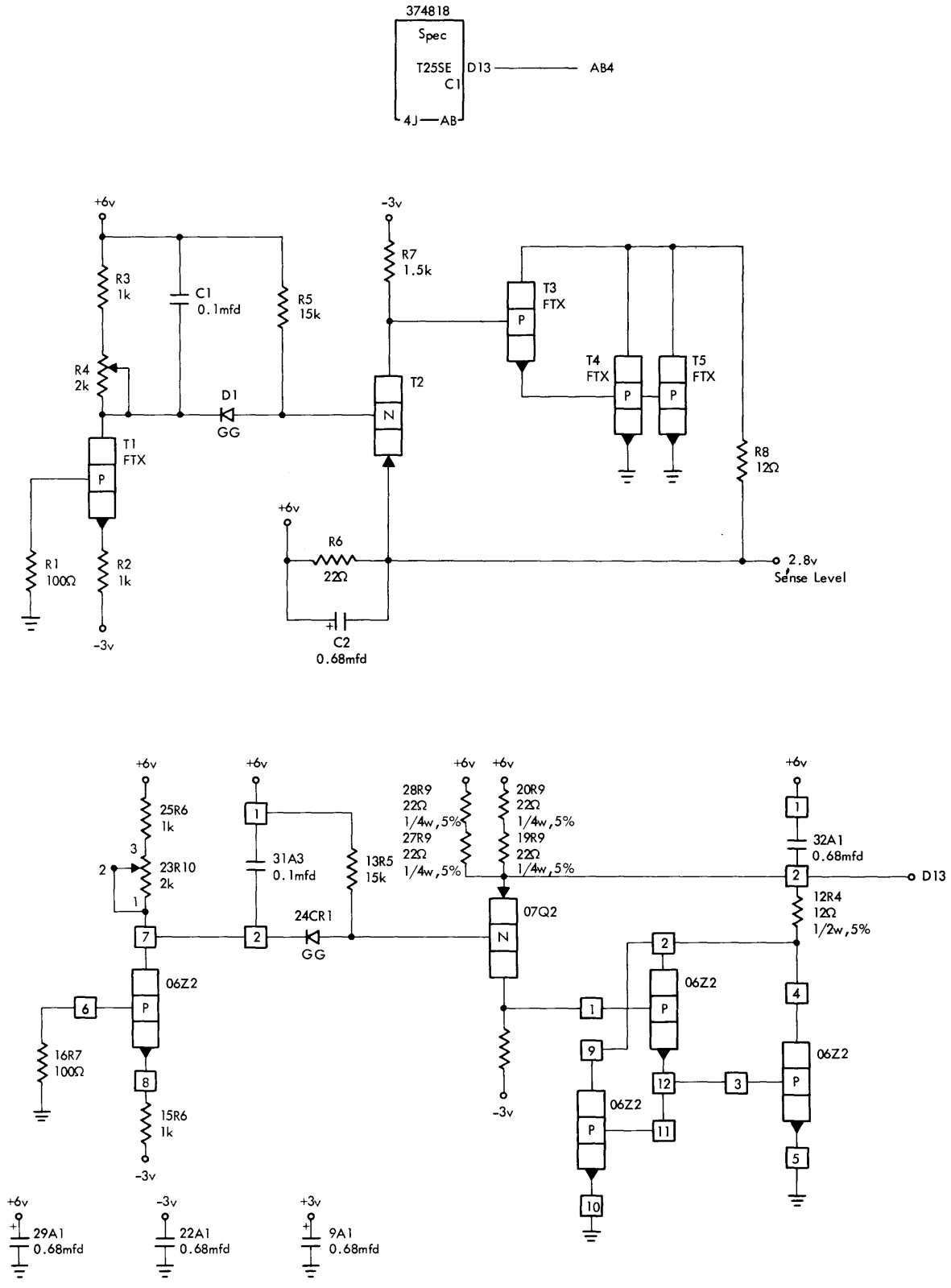


Figure B-2. Sense Level (T25SE)

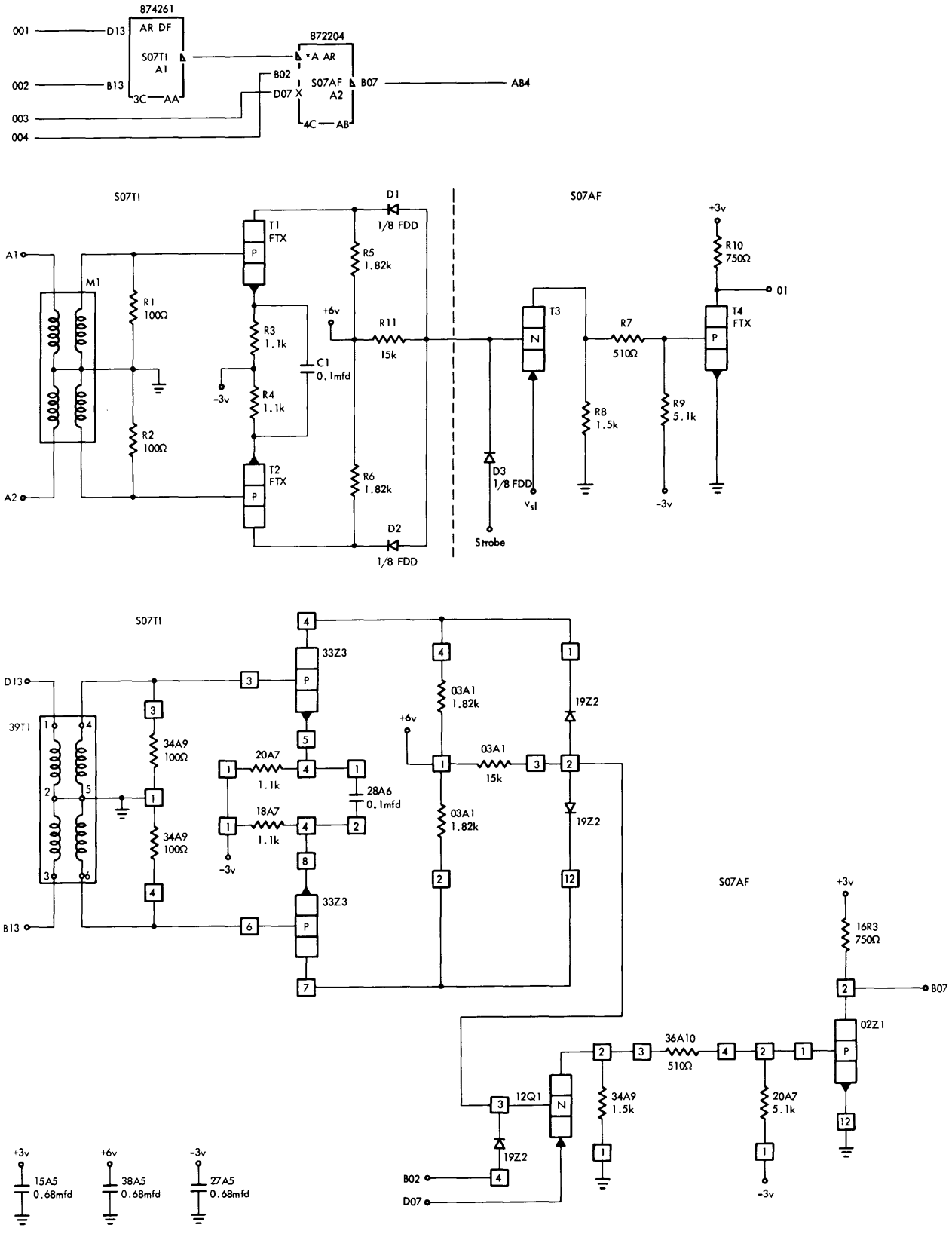


Figure B-3. Sense Amplifier (S07AF, S07T1)

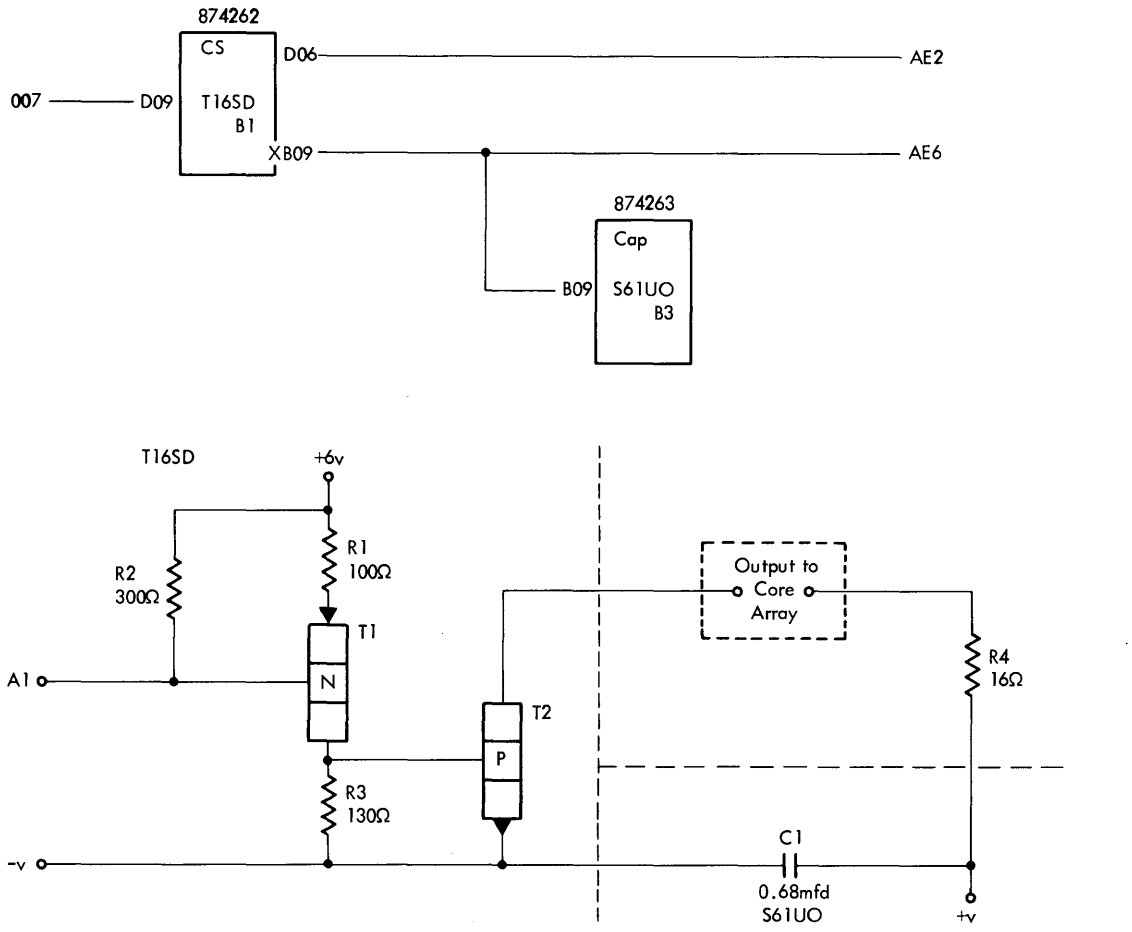


Figure B-4. Inhibit Driver (T16SD)

Input A1 is driven by a loaded AOI (U03AF) circuit and is normally positive (Figure B-5). Transistors T1 and T2 are normally on, transistor T3 is normally off, and the output (01) is clamped to approximately 4.4v. When the read Y gate becomes active, the input drops to ground level and T1 is reverse biased by the initial voltage across C1. With T1 off, capacitor C2 is charged with the polarity shown in the diagram. T1 remains off for the period of time determined by the RC network R1, R2, and C1. As C1 discharges, T1 becomes forward biased and is driven into saturation. With T1 on, the voltage across C2 reverse biases T2. When T2 turns off, T3 is driven into saturation. The output (B02) then falls to approximately 2.2v. T2 remains off for the period of time determined by the RC network R4, R5, and C2. As T2 again turns on, the output returns to its initial level (4.4v). Potentiometer R1 varies the delay between the input and the output pulse. The method of adjusting R1 is in the maintenance manual.

AMPLIFIER CURRENT SOURCE

- This circuit provides a constant, temperature-controlled current to the core drivers for read or write cycles.

- Maintenance data is in the maintenance manual.

The amplifier current source circuit provides current for the X and Y core drivers. This circuit controls the current through the array by controlling the current in the core drivers. The temperature controlled voltage (V_{ref}) is used to provide constant current output over a wide range of temperatures.

Input A1 is driven by the output of an AND circuit (U03AD) (Figure B-6). The output of the AND circuit is down when a read or a write cycle is desired. Normally, A1 is at the up-level and transistor T1 is off. When a read or write cycle is desired, A1 goes to a down level and point E is clamped to the voltage determined by the reference voltage on

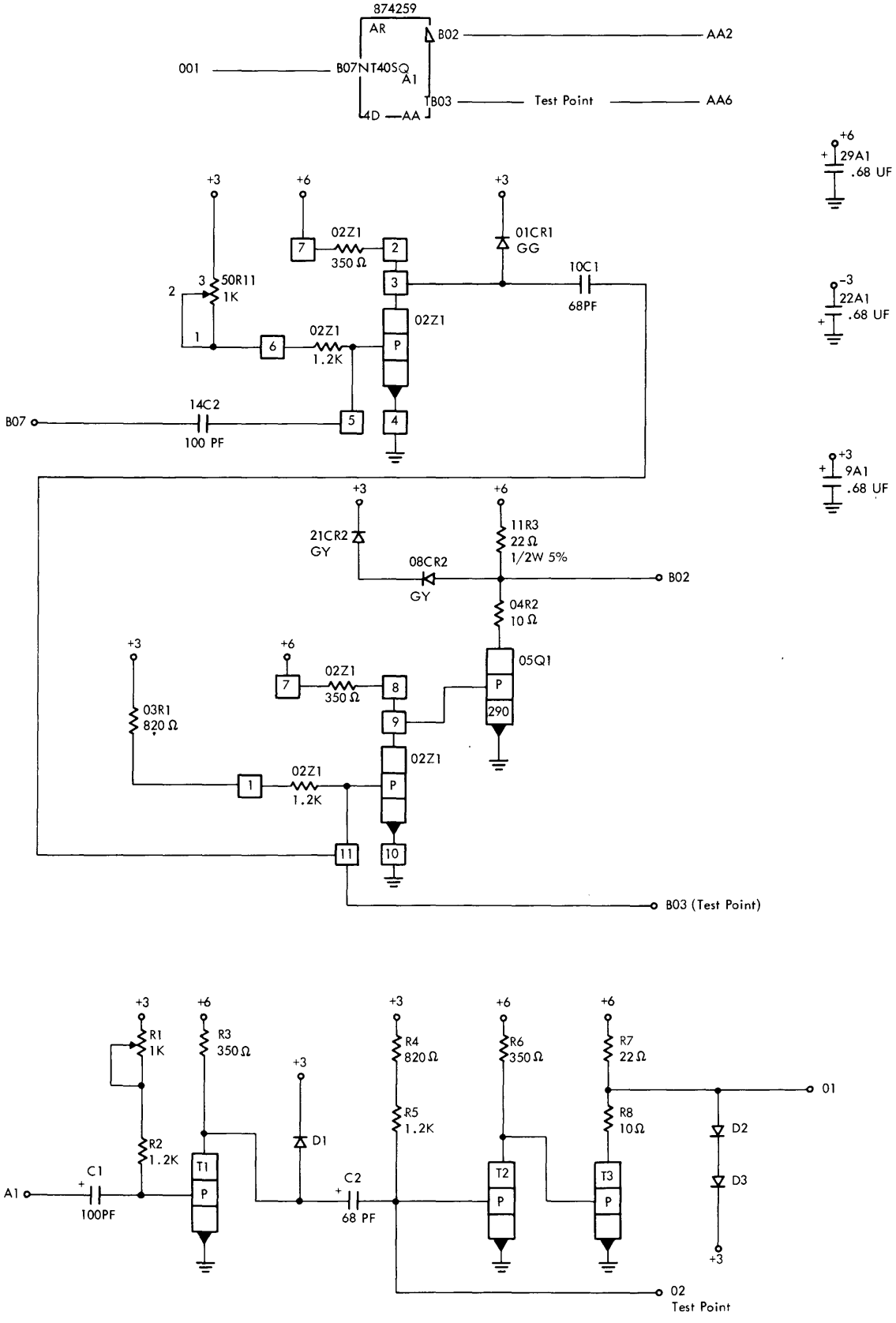


Figure B-5. Strobe Driver (T40SQ)

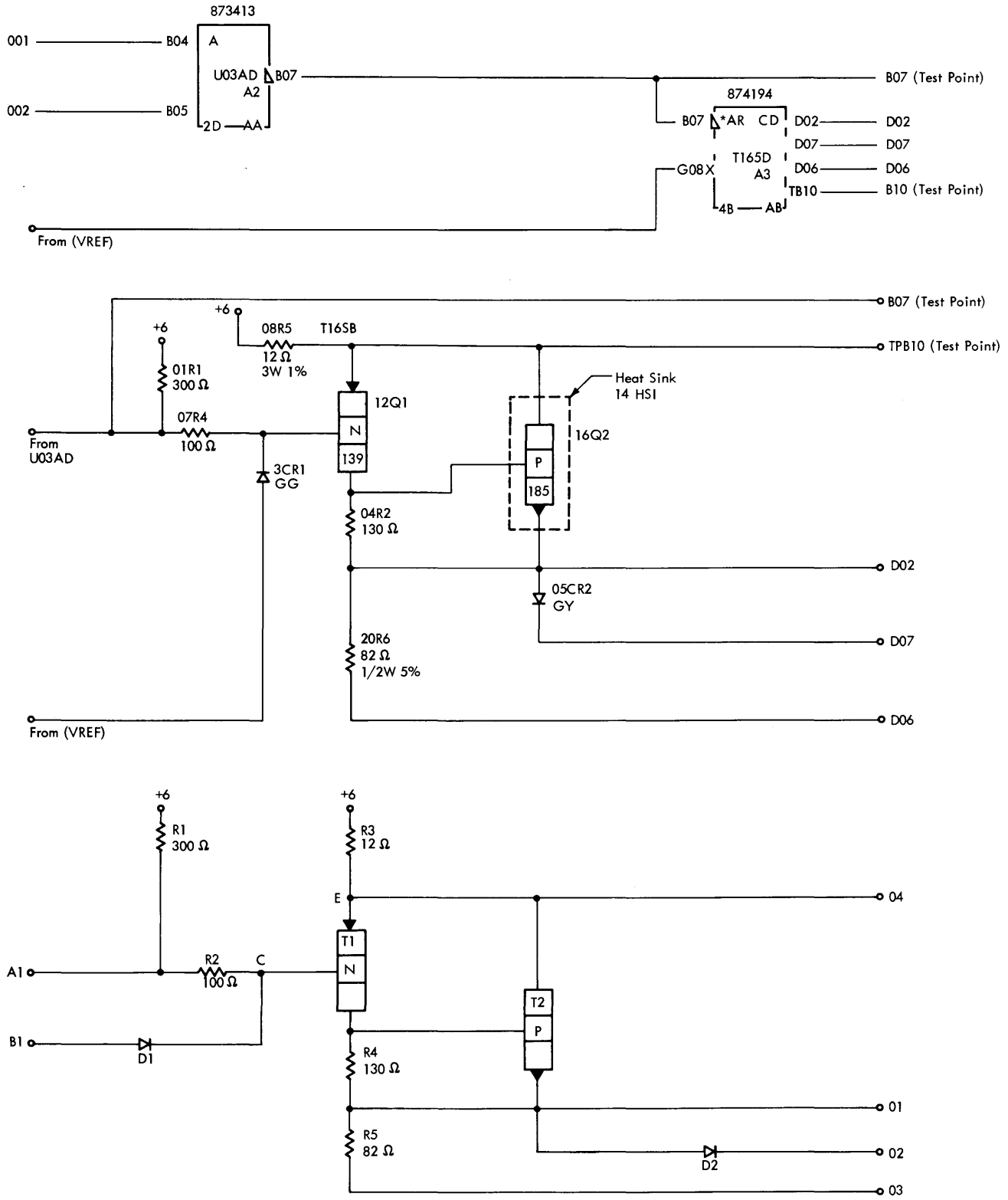


Figure B-6. Amplifier Current Source (T16SB)

input B1 (V_{ref}). V_{ref} is temperature compensated and as V_{ref} varies, the voltage at point E follows. The output current is determined by the voltage difference between +6v and point E divided by R3 $\left(\frac{+6v - E}{R3}\right)$. Resistor R1, is the load resistor for the U03AD circuit. R2 is the load resistor for the reference voltage. R4 is the bias resistor for the second stage transistor (T2).

In the 2870, output 02 and 03 are grounded. With 02 and 03 grounded, D2 prevents T2 from saturating and R5 terminates the output line.

CORE DRIVER AND GATE

- These circuits supply switching current to the local storage X and Y lines.
- Two identical circuits are used to form the driver and gate combination.
- Array current is controlled by the amplifier current source circuit which drives the core driver.
- Maintenance data is in the maintenance manual.

The core driver and gate circuits are two identical circuits connected by a local storage X or Y array line. When these circuits are conditioned, switching current is supplied to the array line. To condition a core driver and a gate, the local storage address bits activate two AND circuits (one to condition the core driver and one to condition the gate).

Input A1 is driven by the amplifier current source circuit (T16SB) (Figure B-7). The amplifier current source circuit acts as a constant current source to control the current through the array. Input B1 and B2 are controlled by logic AND gates, which are conditioned by decoding the local storage address bits. With the two AND gates active, transistors T1 and T3 are turned on simultaneously. T1 and T3 saturate transistors T2 and T4. Because the emitter of T2 is connected to the collector of T4 through an array line, switching current now passes through array line. The amount of current through the array is controlled by the amplifier current source circuit (T16SB).

POST CHARGE CIRCUIT

- The post charge circuit is used to suppress noise on the local storage array lines.
- When the drivers and gates of an array line are turned off, the post charge circuit is used to clamp both ends of the array lines near ground.
- Maintenance data is in the maintenance manual.

The post charge circuits are used to suppress the noise on array lines caused by the "flipping" of cores. To suppress noise, the post-charge circuit clamps both ends of the array lines to a level near ground when the core drivers and gates are not conditioned. In the 2870, the post-charge circuit is off when read or write are active, and on when read and write are inactive.

Input pin D06 is connected to a special negative power supply (-15v), and pin B08 drives both post-charge circuits (Figure B-8). When the local storage read or write lines are active, the input (B08) is at an up level and the post-charge circuits are off. When read or write falls, the input to pin B08 falls and the post-charge circuits are turned on. Output pins D02, B02, B03, and B04 are connected to the array lines on the non-diode end. Output pins B07, D07, B13, D13, D12, B12, B10 and D09 are connected through the steering diodes to the other end of the array lines. There are two spare FDD diode pairs with inputs D11 and D05, and outputs D10, B09, D04, and B05.

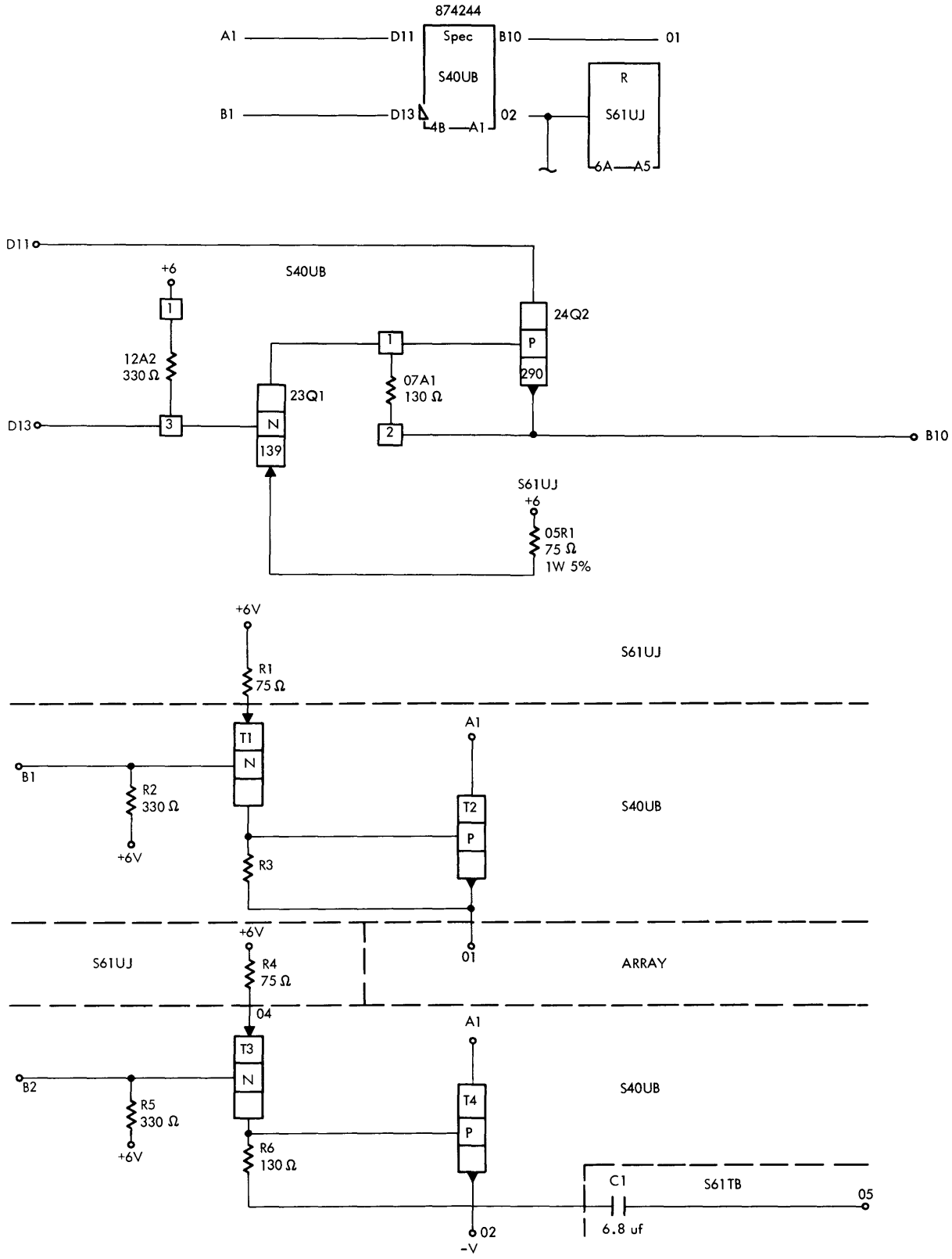


Figure B-7. Core Driver and Gate (S40UB, S61UJ)

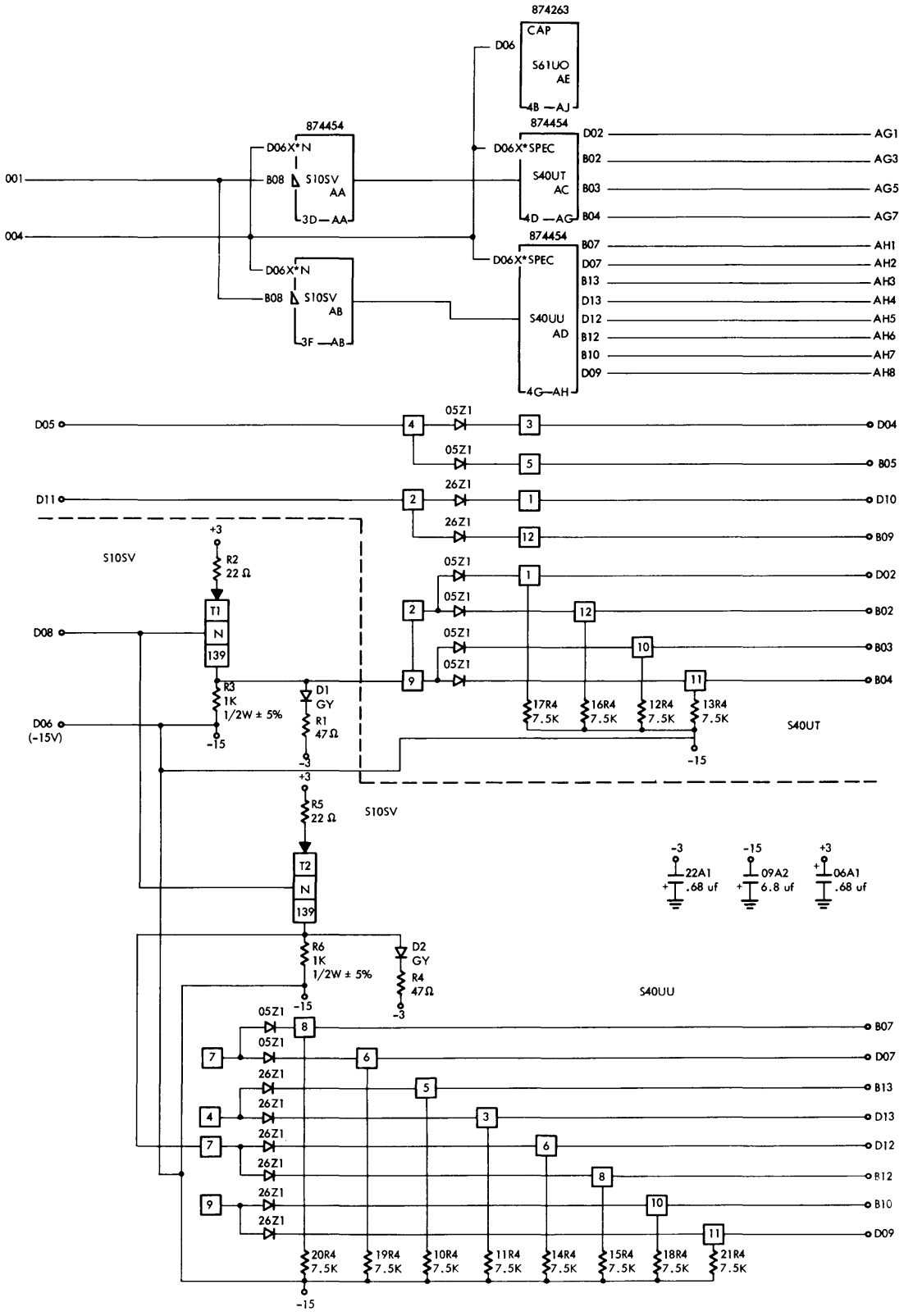


Figure B-8. Post Charge Circuit (S10SU, S40UT, S40UU)

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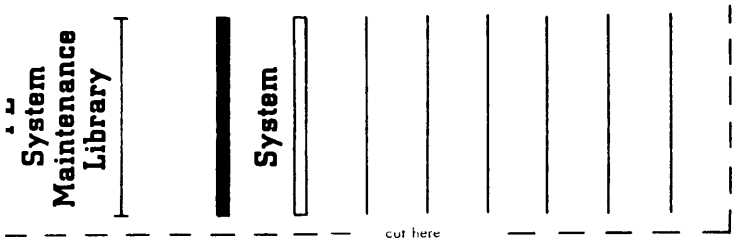

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