Troubleshooting

If the IBM 1401 Data Processing System fails to operate properly, the cause of the trouble must be found and corrected quickly to hold unproductive machine time to a minimum. Rapid and effective diagnosis depends upon thorough knowledge of machine logic and effective use of diagnostic tools available. Diagnostic programs, marginal checking, checking indicators and CE test panels are aids for troubleshooting the 1401 system.

Diagnostic Programming

The 1401 customer engineering tests are specifically designed to help the customer engineer in the field to test functional operations of the 1401 and its associated components.

These tests, when properly used, help the customer engineer to install the 1401 with a minimum of time and effort, thereby assuring efficient operation of the system before it is released to the customer.

A complete set of write-ups along with flow charts that describe the various tests are shipped with each 1401 system.

Marginal Checking

Marginal checking (MC) has two basic maintenance functions:

1. Scheduled maintenance — to increase system reliability.
2. Unscheduled maintenance — to minimize system down-time in troubleshooting for *intermittent* symptoms produced by degrading components. Marginal checking can force these into the region of solid failure.

In tube machines, marginal checking is of value in both of these functions. With the much higher reliability of solid-state machines, preventive maintenance becomes less important, and troubleshooting becomes the main purpose of marginal checking. Scheduled MC is required in order to clean up any bugs that excessively limit the MC range. This is necessary to ensure that adequate MC range will still be available when the next intermittent symptom occurs.

The marginal-checking scheme used in the 1401 system is an inherent part of the circuit design. Separate voltage busses are provided exclusively for marginal checking. Only those circuits which can benefit from marginal checking are connected to the MC bus. These connections to the MC bus are specifically designed to give each circuit approximately the same sensitivity to MC voltage variation. In every case, the MC connection to the circuit is designed so that good components cannot be damaged by the full ±3v marginal-check variation. The only possibility for component damage occurs with defective components that are already out-of-specification and on the brink of failure.

A ±3v variation on the +6M or −12M voltages will have very little effect on the steady state performance of normal circuits. Dynamically, the 3v MC shifts will cause about a 25 percent change in timing in most circuits.

The 1401 engineering specifications specify correct machine operation with a minimum variation of any marginal-check voltage by ±1.2v. This is a minimum variation. Many systems surpass this.

As soon as time permits after a new machine is installed, make a complete marginal check. Record the limits for future reference. Replace any out-of-specification cards that limit the MC range. After this, MC at two- or three-month intervals should be sufficient. If experience shows very little change in the limits, the MC interval can be increased. Make a complete MC check after installing any major machine changes.

When performing marginal checking, the combined 1401 CE diagnostic tests are to be used. These tests are arranged from the simple to the more complex operations. Refer to *Power Supplies* for a description of marginal checking.

Method of Performing Marginal Test

Note: Machines that have switches for selecting the gates to be marginal-checked have caused considerable trouble because of poor contacts. The marginal-check switches should be pushed in and left to eliminate the poor-contact problem. Future systems will eliminate these switches.

1. Select voltages to be biased by jackplug. Place the jackplug in the rest position when the marginal test is not being used.

The +6M voltage provides base bias on NPN inverters.

The −12M voltage provides base bias on PNP inverters.

The +12M voltage provides base bias on SDTDL circuits in TAU-9.

The +30M voltage provides base bias on current-source circuits for core storage by varying the +18v differential.

The remote hub provides bias to remote units. The voltage is selected at remote unit with another jackplug (Figure 13).

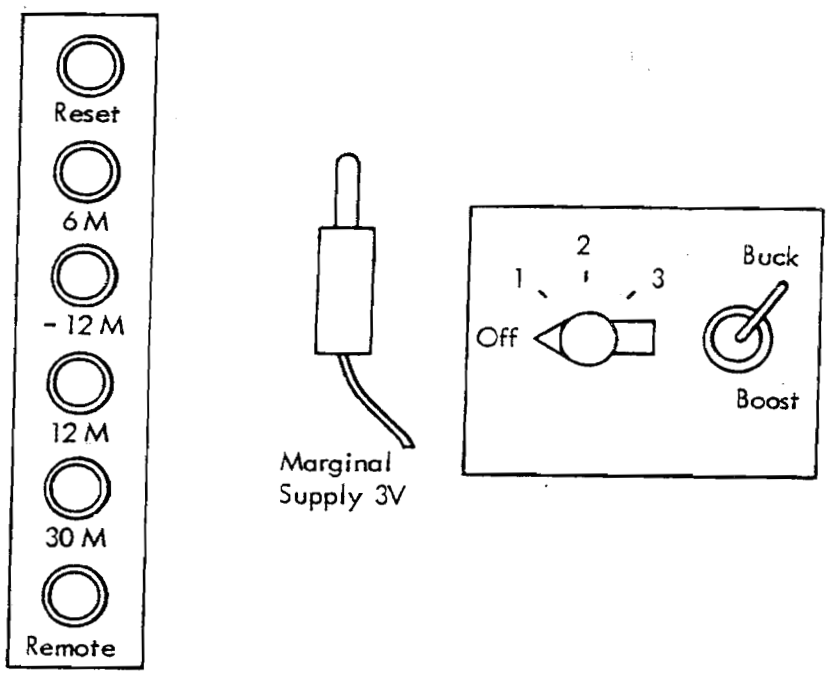


Figure 13. Marginal-Check Controls

2. Connect a meter to the supply selected with the jackplug. If the circuit breaker on the marginal 3v supply kicks out, no indication is made. The meter tells you exactly how much you are varying the supply being tested.
3. Set the buckboost switch.
4. Vary it with the Variac* switch.

VOLTAGE-LEVEL CHECKING

1. Periodic checking is recommended as a PM procedure.
2. Voltages should be exact; +12 variable is the exception.
3. Voltage should be measured at the place it is most likely to give trouble.
4. Voltage should be measured with the most accurate instrument available. A ½% dc meter is recommended.

RECAUTIONS TO OBSERVE

1. The—12v supply is referenced to —6v. Therefore, it must be adjusted after the —6v supply.
2. The +12v fixed and variable supplies are developed from the +30v supply. Therefore, they must be adjusted after +30v.
3. Ripple on a supply can give a false meter reading.

PURPOSE OF SUPPLIES

—6v	Emitter voltage for NPN transistors.
+6v	Collector voltage for NPN transistors.
—12v	Collector voltage for PNP transistors.
+12v	Supplies base of transistors in core storage circuits.
+12v extender	Supplies the TAU-9 circuitry.
+18v differential	(+12 variable) Supplies current source circuits in core storage.
—20v	Supplies row-bit cores.
—20v filtered	Supplies bias for decode switches.
+30v	Supplies bias current for switch cores, collector voltage for decode switches.
—36v	Supplies TAU-2 circuits.

SEQUENCE FOR CHECKING VOLTAGES

+6v, —6v, and —12v for frame 1 are located in 02A4 and 02A5. Measure at gate 01B3: clock circuits and distribution.

+6v, —6v, and —12v for frame 2 are located in 02A3 and 02A6. Measure at gate 02B2 — TAU. If TAU is not on the machine, check at available optional-feature gate 02A7 or 02A8.

+30v measure at 02B2. If there is no TAU, measure at 01B3.

If there is TAU-2, measure —36 at 02B2.

—60v located in 1402. Model D location 01B4. Measure at 01B8 on —60v bus bar.

—20v located in 1402. Model D location 02A8. Measure at 01A2 A24Q.

Marginal Check Techniques

Studies have proven that marginal failures in solid-state circuitry are not all aggravated by any single marginal-check technique. Laboratory and field tests determined that base-voltage variation, the standard technique now in use, is primarily effective where failures are caused by transistor turn-on delays. Other known techniques have proved superior where intermittent failures were caused by noise, incorrect levels, or critical timing conditions.

*General Radio Corporation

When troubleshooting an intermittent failure, analyze the symptoms very carefully; note all console error lights, contents of registers, cycle lights, etc. Work with the customer's program at the start. Try inserting a branch op to define a failing loop. Often a failure that appears intermittent will fail solidly if the same data, or the same sequence of operations, is repeated.

If the problem cannot be duplicated with this approach, or with the diagnostic tests, try the marginal techniques listed here. The failure rate of most intermittent problems can be increased by one of these techniques. Branch offices already using this approach report a high degree of success.

Two cautions should be carefully noted:

1. Techniques described here are presented as troubleshooting tools *only*. Their use as preventive maintenance tools results in excessive service time and unwarranted parts replacement.
2. On any of the techniques, a difficult-to-diagnose failure, unrelated to the customer problem, may be introduced. This point can be within voltage limits specified here, particularly on older machines. If these problems cannot be resolved in a reasonable length of time, move on to another voltage or to the next technique.

   Base-voltage variation should be the first marginal technique tried. Other techniques can be applied in any convenient sequence. A detailed description of each technique follows.

BASE-VOLTAGE VARIATION

The +6M and −12M voltages supply transistors base potential throughout the 1401. The standard technique of varying these two voltages is known as *base-voltage variation.*

Vary these voltages toward their ±3.0 volt limits. Attempt to correct any failures that occur within these limits, or to the limit where the customer failure is duplicated.

Note: Some twin SMS cards, P/N 373000, will fail above ±1.2 volts bias unless capacitors announced in 1401 EC-CEM 579 are installed.

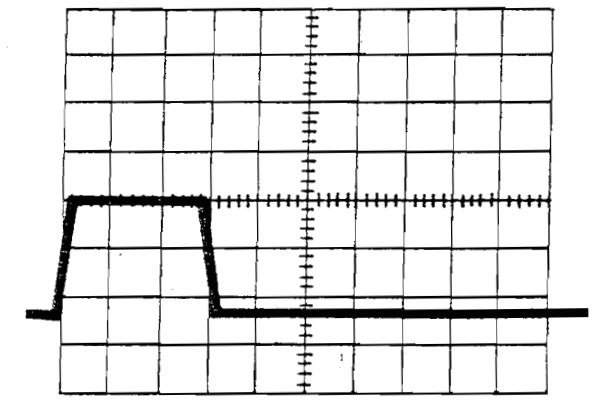
FREQUENCY VARIATION

Basic 1401 clock frequency is increased in this technique. It is most effective where failures are caused by marginal timing conditions (line delays, slow cards, etc.). Proceed as follows:

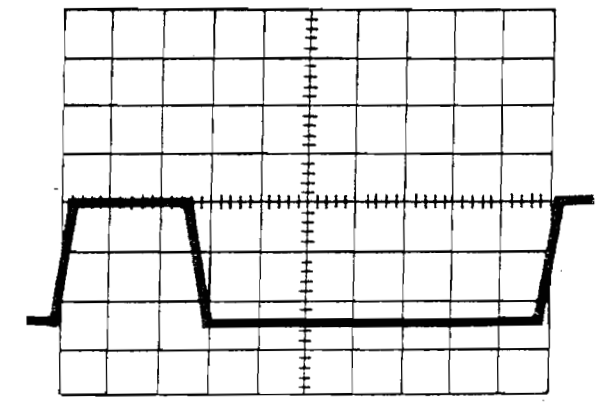
1. Set the scope as indicated in Figure 14. Display the output of the ±0 hub, located on the CE console with the machine in static condition. The output should appear as shown in Figure 14A.

SCOPE SETTING:
SYNC – INTERNAL +
VERTICAL DEFLECTION – 0.5 V / DIV.
(EFFECTIVELY 5V/DIV)
HORIZONTAL DEFLECTION – 1 MICRO. SEC./DIV.

A.



B.



C.

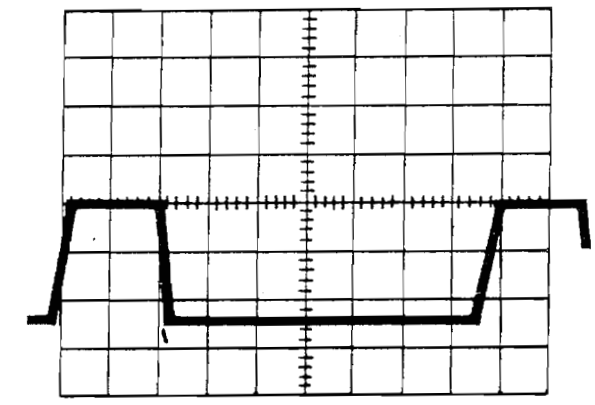


Figure 14. Clock Frequency Variation

2. By adjusting the time-per-division calibration knob counterclockwise, bring the positive-going portion of the next pulse onto the right side of the scope and line it up with the last vertical line on the scope face (Figure 14B).
3. Turn the power off and remove SMS card (RK –), P/N 371788, in location 01B3 A 26. Install variable oscillator SMS card, P/N 372561.
4. Turn the power on. Without changing the scope, adjust the pot on the variable oscillator card so that the scope picture is again identical to Figure 14B.
5. Run diagnostic tests. Vary the oscillator slowly so that the leading edge of the second pulse moves from the rightmost vertical line to a point 1⅕ horizontal divisions to the left (Figure 14C). This effectively increases the clock frequency from 11.5 to 10.0 microseconds.

CAUTION: The leading edge of the pulse should not be moved to the right of the last vertical line on non-print buffered systems. This *decreased* frequency causes hammer-driver fuses to blow on these systems when a print op is performed.

6. Troubleshoot all failures that occur within this range.
7. When limits have been met, drop the power and replace the oscillator card with a standard one.
8. On machines equipped with a print buffer, if machine failures are associated with a print operation:
   a. Rather than replace the basic block oscillator, observe the +U RO Time 000-030 pulse at 01A5 B14N, with the scope set as indicated in Figure 14.
   b. Adjust the scope as in Step 2, observing Figures 14A and B.
   c. Remove buffer clock oscillator SMS card (FT–), P/N 371405, from location 01A5 A07. Install variable oscillator SMS card, P/N 372561, using SMS card extender, P/N 451075.
   d. Follow the procedures as in Steps 4, 5, 6, and 7.

Note: Do not *decrease* frequency beyond 11.5 microseconds when printing.

MECHANICAL VIBRATION

Vibrating SMS cards is effective in showing failures caused by SMS socket contact resistance, cracked land patterns, or poor component connections.

With the palms up, run the backs of your fingers down the card rows, from top to bottom, while diagnostic tests are running. Vibrate the cards on any gate that may be associated with the machine problem.

CAUTION: Component damage can result from excessive vibration. If adjacent SMS cards contact, serious machine damage will result. To determine how hard to vibrate, a good rule to follow is: "If the vibration hurts your finger, slow down!" Vibrate the cards on all gates that may be associated with the failure.

COLLECTOR VOLTAGE VARIATION

This technique varies voltages (+6 and −12) that supply transistor collector potential. It is particularly effective in showing failures caused by electrical noise or bad levels.

From #22 gage (or larger) wire, make a jumper about 18 inches long. Solder spade clips to both ends. Proceed as follows:

1. Analyze the failure to determine the possible machine operation or unit involved.

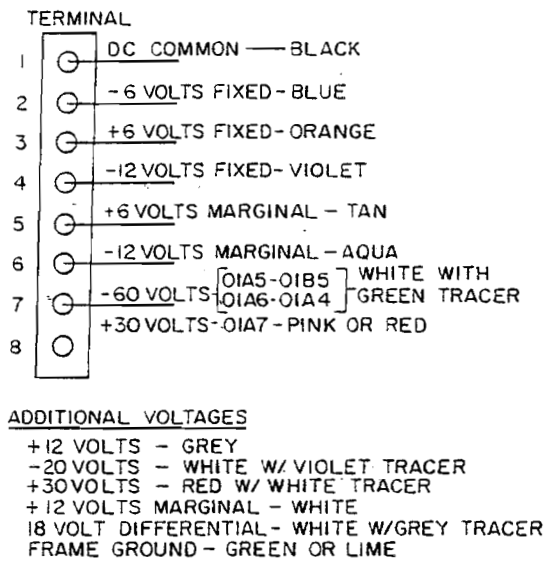


Figure 15. Voltage Terminal Block

2. Refer to the gate logic index pages in the front of Logic Book I. Select the gates containing the circuitry unique to this operation or machine function.

   As an example:

   a. Assume the failure appears to be a carriage problem. Logic indexes indicate Gates 01A5 and 01B1 contain this circuitry.
   b. If STAR-bit pickup is occurring, Gates 01A7, 01A8 (and 02B6, 02A7 if on the system) are affected.

   Note: TAU gates and memory gate 01A1 should not be collector-biased.

3. Select one of the affected gates. Drop the power and make the following changes at gate voltage terminal block. (Refer to Figure 15 located to the left of Row A.)
   a. Disconnect the external voltage (orange) wire from the +6v terminal and connect one end of the jumper to this terminal.

   CAUTION: Be certain the orange wire is positioned so that it does not short to frame, or the other connections.

   b. Connect the other end of the jumper to the +6M terminal (the terminal with the tan wire attached).

   Note: If no tan wire comes to this gate, connect the jumper to the terminal on the adjacent gate where this voltage is available.

   c. Connect a voltmeter to a +6v pin (Pin L) on the gate. Insert the marginal-voltage supply jack in the +6M hub (or set the marginal-supply switch to +6M on earlier machines).
4. For gates other than 01A4, 01A5, 01A6 and 01B5, proceed to Step 5. For Gates 01A4, 01A5, 01A6 and 01B5, disconnect −60v hammer-magnet return by

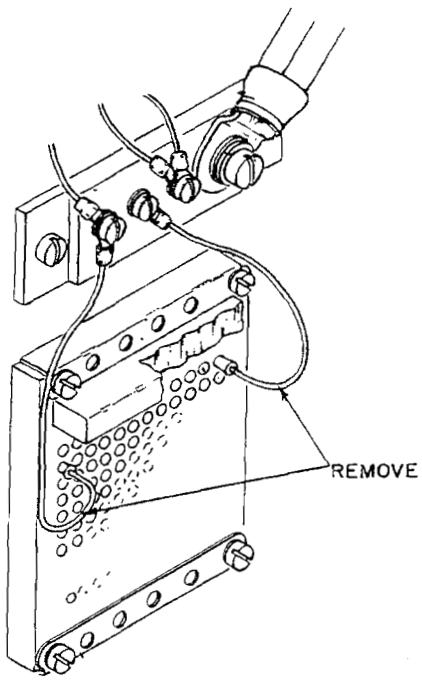


Figure 16. Relay Base Terminal Block

removing two black wires at the —60v return-relay, base-terminal block in 01B8 (Figure 16). Turn on the power. Begin by loading the print area with blanks and programming a simple print and branch loop. Observe the console-error lights and scope the output of the print-reset check latch at 01B5E01A to determine if errors occur. Now proceed to Step 6.

5. For gates other than 01A4, 01A5, 01A6 and 01B5:
   a. Turn on the power.
   b. Select the diagnostic tests applicable to failing machine function or operation.
   c. Run diagnostics and proceed to Step 6.
6. a. Vary the marginal-voltage supply. Collector voltages can be varied as much as +3.0 volts without causing machine damage. Vary the voltage to this limit in search of the trouble, if no other trouble occurs prior to this limit.

      Note: When biasing 01B7, a point is reached where all magnet drivers fire simultaneously. Do not continue to run the machine or bias beyond this point.

   b. Fix any failure that occurs before reaching the limits of 1.0v buck to 1.5v boost. If this trouble appears to be similar to the trouble, consider the machine fixed.
   c. When going beyond the limits of 1.0v buck to 1.5v boost, fix a trouble only if it appears to be the reported trouble. For future reference, it might be well to record the symptoms of failures in this area.

      Note: The trouble may appear somewhat different because the machine is undergoing a more severe test than it normally receives.
7. If customer-reported trouble has not been found, and the bias limits of the +6v on this gate have been reached:
   a. Drop the power and restore the voltage wires to normal.
   b. Disconnect the external voltage (violet) wire and connect one end of the jumper to the —12 volt terminal on the gate voltage terminal block (Figure 15). Be certain the violet wire is positioned so that it does not short to frame, or other connections.
   c. Connect the other end of the jumper to the —12v voltage terminal (the terminal with the aqua wire attached).

      Note: If no aqua wire comes to this gate, connect the jumper to the associated terminal on an adjacent gate.

   d. Connect a voltmeter to a —12v pin (Pin M) on the gate. Insert the marginal voltage-supply jack in —12M hub (set marginal check switch to —12M on early machines).
   e. Repeat Step 6.
8. If the trouble has not been found, and the —12v limits have been reached:
   a. Drop the power and restore gate voltages to normal.
   b. If other gates are involved, select one of these gates and continue, starting with Step 3.

DUAL BASE VOLTAGE VARIATION

Note: To utilize this technique, the machine must be equipped with a marginal-voltage jackplug receptacle. Obtain an additional marginal-voltage power supply. Plug the first supply into the +6M jack hub; plug the second supply into the —12 jack hub.

Vary marginal voltages ±1.5 volts separately or collectively, in any combination. Run diagnostic tests and follow this guide:

1. Set +6M to 4.5 volts; vary the —12M ±1.5 volts.
2. Set +6M to 7.5 volts; vary the —12M ±1.5 volts.
3. Set —12M to —10.5 volts, vary the + 6M ±1.5 volts.
4. Set —12M to —13.5 volts; vary the +6M ±1.5 volts.

A variable oscillator SMS card, P/N 372561, has been automatically shipped to each branch office, for use as an office tool.

Check Circuits

The following check circuits are used in the IBM 1401 Data Processing System: parity, validity, invalid address checking, and wrap-around checking.

PARITY CHECKING FOR A-REGISTER, B-REGISTER, AND INHIBIT CIRCUITS

Parity checking is accomplished by switching an even-digit and even-zone or an odd-digit and odd-zone bit combination to develop the error condition, when the bit sum is even.

The A-register error condition is gated with ACTIVATE STORAGE, NOT I-RING OP, and time 075-090.

The B-register error condition is gated with ACTIVATE STORAGE, and 045-060.

The storage parity check is gated with ACTIVATE STORAGE, NOT START OR ENTER, and 090-105.

ADDRESS VALIDITY CHECK

Address validity checking includes parity checking for a valid bit combination, and checking for a valid address.

Address parity checking is accomplished by switching an even-digit and odd-zone bit combination or an odd-digit and an even-zone bit combination to produce an odd-bit line on all bits combined. The absence of an odd-bit configuration signal switched with ACTIVATE STORAGE at times 015-030, 045-060, or 075-090 sets the check latch.

An invalid bit combination would show up either as a no-even or no-odd digit, or as zone-bit combination lines that indicate an error as previously stated in the section *Parity Checking for A-Register, B-Register, and Inhibit Circuits*. The invalid bit combination shows up in this manner because only valid bit combinations develop the even- and odd-digit bit-combination lines. Valid digits in the storage-address register are the digits 0 through 9.

INVALID ADDRESS CHECKING

Checking for a valid storage-register address is accomplished in a manner similar to validity checking. However, the validity of the address depends on the storage capacity of the system. Any 3-digit address, including the hundreds position zone, is valid for a 4k system. Only addresses between 0000 and 1399 are valid for systems with 1.4k storage. The invalid address is brought up when indexing to above-capacity storage.

Examination of the addresses that are involved with the 4k storage shows that there is no invalid address. The possible bit combinations of the hundreds position (zones) AB, AB, AB, and AB along with any valid digit), are all valid because they address locations between 0000 and 3999.

Close examination of the hundreds position of the invalid addresses involved with the 2k storage system (2000 to 3999) shows that they all have a B-bit in common. Because there is no B-bit output from the storage-address register on systems less than 4k storage, the B-bit will be lost and a parity check error will result.

The same invalid addresses (2000 to 3999) are detected the same way on systems with 1.4k storage. In addition, check circuits are provided to detect addresses between 1400 and 1999. This is accomplished by switching a 4-bit and an A-bit together (1400 and 1799) or an 8-bit and an A-bit together (1800 to 1999) at hundreds time, thereby detecting an invalid address.

WRAP-AROUND CHECKING

Wrap-around describes the process of modifying the highest address of a system by plus one, or the lowest address by minus one. For example, wrap-around on a 1.4k storage system would mean modifying 1399 by a plus 1 to obtain 0000, or modifying 0000 by minus 1 to obtain 1399.

If wrap-around is detected at any time other than during a storage-scan operation or a clear operation, it sets the storage-address register check latch at 075-090 time, thereby stopping the machine at the end of the next cycle.

A good analyzation of the 1401 console-error indicators, A- and B-registers and the op-register, assists in breaking down the type machine failures that have been encountered during the program routine. Figures 17, 18, and 19 act as a recall on what should happen when a specific error is encountered.

Additional charts showing which latches are affected when detecting these various errors can be found on Figures 20, 21, and 22.

General Service Hints

Diagnostic Procedure

Consult with the customer to determine what he has observed. Find out what the correct output should have been. See if he can demonstrate the failure.

Run the diagnostic function tests to see if they will fail. When they show the trouble, this is the best way to analyze the failure. If the machine does not fail, you must use accentuating methods: marginal checking, stopping blowers on gates, locking in program loops, etc.

When you get failures, compare correct and incorrect results, what tests failed, what effect varying data has, what is common to these results. Determine what unit of the machine is failing from this analysis.

Select and simplify the operation that causes failure; then lock the machine in a loop: switch B or D on diagnostic function tests, hand-enter the program loop, change the customer's program to loop, etc. Use the scope to trace down why your objective is not working. When you have determined where the trouble is, swap cards or substitute units to prove you are right.

D.F.T. on Tape

If you have a tape system, be sure to place the diagnostic function tests on tape soon after installation. Write the test tape and stop the program before rewinding. Unload tape, add a second load-point sticker, and rewrite the tests. This will give you a spare if one gets damaged.

The tests can be run from tape much faster than they can from cards.

Console Lamps

Burned out bulbs can cause circuit failures and be misleading in analyzing troubles from the console. Testing the bulbs also tests the error circuits. Tape console bulbs can all be lighted by grounding the jumper at the top of the panel.

Tape console lamps on TAU-2 machines make good sync points.

Muffin Fans

Fans should be checked at least once a week or on a service call. Some fans have been found to be running slow.

Thermal, Core

Power OFF can occur due to the thermal element in 01A1 opening because of a faulty fan or switch. This thermal should be checked at maximum two-month intervals for correct operation. This can be done by turning the power OFF and connecting an ohmmeter across the switch. Heat the element with a soldering iron and the meter circuit should open. This, however, does not determine the exact temperature setting at which the thermal element operates.

Clock Pulses

On intermittent and hard-to-analyze troubles, do not discount the possibility of incorrect levels or timing pulses from the clock. These pulses are very critical and should be checked at the edge connectors on their source chassis.

Observing a Latch Set Pulse

It is difficult to determine what sets a latch. When it latches back, the set line is up solid. The following procedure can be used to observe the set pulse to the latch:

Remove the card with the latch reset pin on it. Using an extender, remove the reset line, and tie the reset input pin on the card to the reset voltage level. This will prevent the latch from latching back, and therefore, enable the set pulse to be scoped easily.

CAUTION: Do not use this procedure on the print reset check latch unless the print area has C-bits only.

Example: A WM latch 31.06.11 3B-4B
Extend the card at 4B. Remove the wire on pin C and connect pin C to +6v.

SMS Voltage Shunt

The following service techniques help save scoping time and point out what to look for when tieing lines to voltages.

Figure 66A shows typical +A block. Notice extender input pin G goes directly to the base of the transistor. Scoping this point alone tells whether the block is switching or not. This saves scoping of inputs D, E, and F. This is especially helpful when a number of

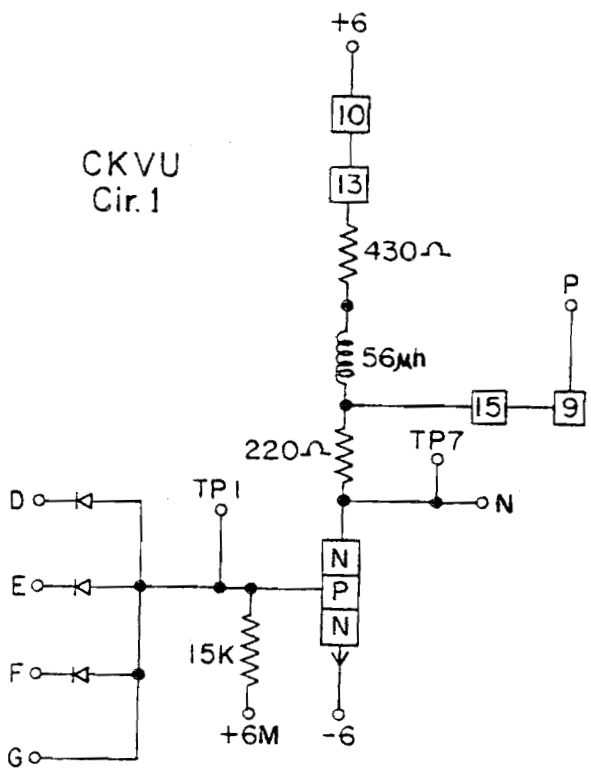


Figure 66A. +AND Voltage Shunt

blocks are dot-ORed together to determine which one is switching. If the block does not have extender input, an appropriate test point can be used. In this example, it would be TP1.

This block can safely be tied on. If output pin N is jumpered to —6v, the transistor is safely shunted out of circuit and no damage results. If pin N was jumpered to +6v, load would be shunted and a total of 12v would be across the transistor. With no current limiting the load, the transistor would burn out.

Figure 66B shows —A followed by a DE. The —A block can be tied ON but not tied OFF for the same reasons explained in the example. Notice the DE block following it is just the reverse. Output pin A can be tied to —12v, not to ground. The 20-ohm resistor in the collector circuit is negligible.

If the DE block is a high-speed one with diode from emitter to base (Figure 66B), it would not be safe to

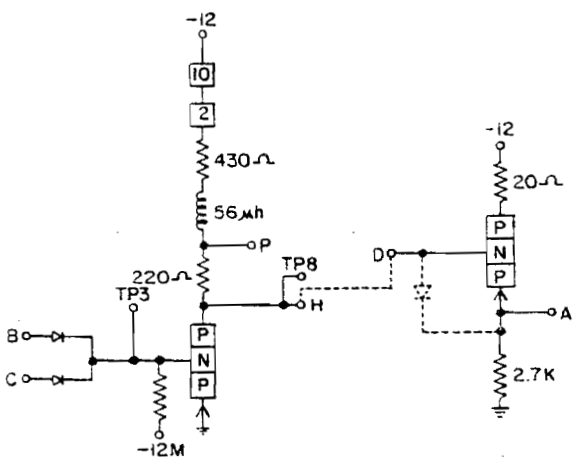


Figure 66B. —AND to DE Voltage Shunt

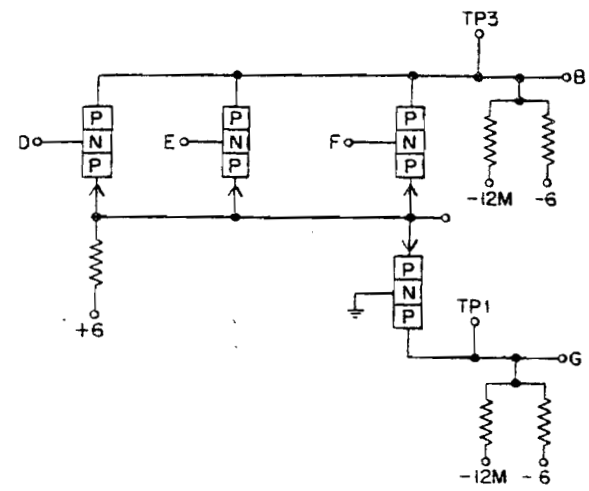


Figure 67. Current Mode Voltage Shunt

tie it OFF because of the possibility of destroying the preceding block.

Triggers can be tied ON or OFF. For example, the CW trigger can be tied ON by jumpering pin E to ground, and it can be tied OFF by tieing pin H to ground.

The foregoing refers to CTDL circuitry. Using extender to isolate circuitry, the following suggestions can be safely used in both CTDL and current mode. Placing a card in the extender and removing the input lines safely removes the preceding blocks from the circuit. Inputs can then be jumpered to the appropriate voltage to turn the block ON or OFF.

In current mode, swing is nominally ±0.8 volts; however, it is safe to tie isolated inputs to appropriate gate voltage. For example, in Figure 67, which is typical —0 or +A with U-line inputs, isolated input pins can be jumpered to 0v or to —12 volts.

Use proper probes and leads. Safe jumper wires and sync leads can be made by using terminal P/N 364471. As added precaution, the terminal on the end of the lead or jumper should be insulated with plastic electrical tape to prevent shorting between pins.

CAUTION: Securely fasten sync leads to scope the sync terminal before placing the other end of the SMS card pin. A sync lead coming loose at the scope can touch the scope case and ground out, possibly resulting in a destroyed card.

CE Panel Diodes

The diodes on the CE panel can be used as extender diodes for any AND switch or driver emitter in the 1401 (systems above 20000). For a —AND, use diodes on the right, and tie the common point to the base of the transistor in the AND block used.

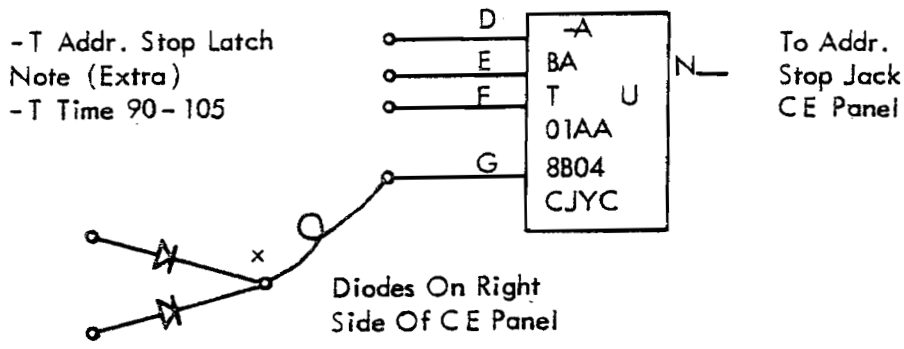


Figure 68. CE Panel Diode Wiring

Examples: 32.45.31.2 (Figure 68).

The diodes do not have a load resistor, nor are they tied down to any voltage. Therefore, they cannot be used as independent AND/OR circuits unless loading is provided.

Component Testing

Most defective components can be located by using an ohmmeter to check for an open or shorted condition. Be sure to consider parallel components when testing with an ohmmeter. An excellent method of determining the correct readings is to compare the readings of an identical, good card with those of the defective card.

The transistor is considered as a back-to-back diode. Check the forward and reverse resistance of each diode with an ohmmeter adjusted to ×100 ohm scale. The forward-to-reverse resistance ratio should be 10. Emitter-to-collector resistance should be the same as the reverse resistance (Figure 69).

MINIMUM INPUT VOLTAGES TO CONTROL TRANSISTORS

C, V and Z Lines Undefined

AND's and OR's
Plus N 0.4 Minus N -0.4
Plus P -5.6 Minus P -6.4
Plus R 5.6 Minus R 0.2
Plus S -0.2 Minus S -5.6
Plus T 1.4 Minus T -0.7
Plus U -5.3 Minus U -7.4
Plus Y -0.6 Minus Y -5.8

CW and JZ Triggers
Plus T 1.4 Minus T -0.7
Plus U -0.5 Minus U -7.4

AR and AS Triggers
Plus S -0.2 Minus S -5.6
Set Pulse 2.6 Volt Shift

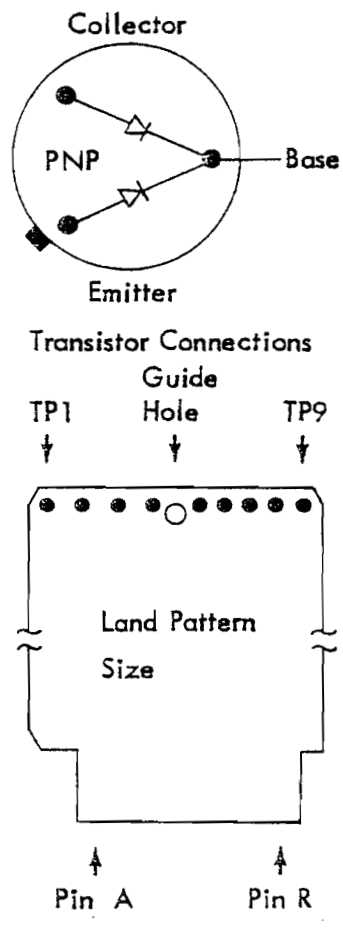


Figure 69. Transistor Connections

Test diodes with an ohmmeter in the same way transistors are tested.

OPEN COLLECTOR LOAD EFFECTS

Generally speaking, open collector circuits have the effect of removing the circuit control from the following stage.

External circuit connections to the logic block can sometimes provide a load resistance for the block when its own load resistor opens. This produces a weak output from the block and can produce highly intermittent failures that are hard to analyze.

The only positive method for checking the load resistor is to remove the output connection on the unit, either by taping the pin or using a card extender. The unit still switches correctly with the output disconnected if the load resistor is good.

Field Replacement SMS Cards

FIELD INVENTORY REDUCTION

Twenty-one field replacement cards, which are capable of replacing 122 standard production cards (Figure 70), are now supplied on 1401 initial spare parts orders. The flexibility of field replacement cards allows the stock of standard cards to be reduced, yet provides the the same number of card types.

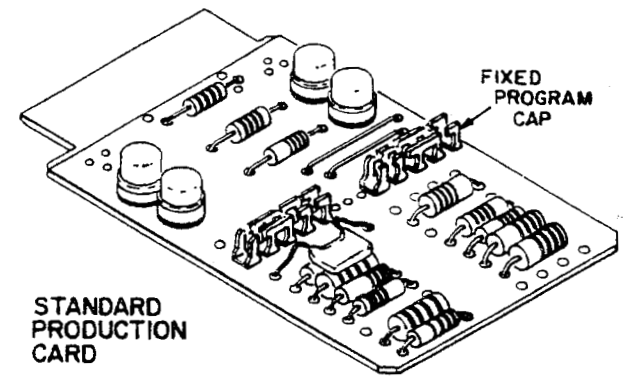


Figure 70. Standard Production Card

DEFINITION

A field replacement card (Figure 71) is a multipurpose card especially engineered for field use and contains a new *barrel-type* program receptacle. By manual pro-

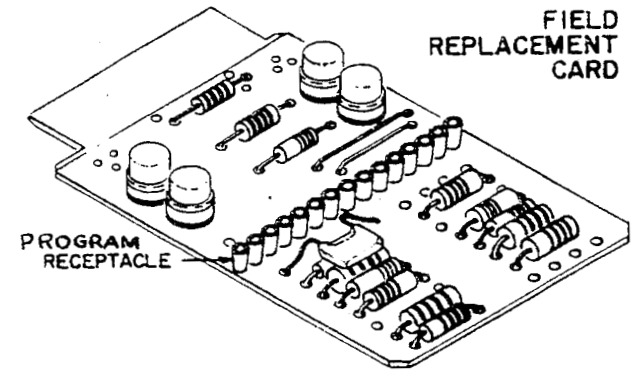


Figure 71. Field Replacement Card

gramming (plugging a contact strip into the receptacle), one card substitutes for 3 to 14 types of standard production cards. The contact strip, P/N 216259, is a group of 17 tapered plugs connected by a common strip.

USE

Programming a field replacement card is made easy by a new cap kit, B/M 451271. The kit contains simple step-by-step instructions, card indexes, which identify the field replacement card to use for a standard card, and templates. The templates are cut out to fit over the program receptacle and make programming a card practically foolproof. The following are the primary steps for using the kit, contact strip, and field replacement cards:

1. Refer to the kit index to find the part number of the field replacement card that can replace a troublesome standard card.
2. Select the proper cap-code template from the kit and place it over the program receptacle of the field replacement card.
3. Using a pair of diagonals, cut the contact strip, P/N 216259, according to the template pattern and insert the contacts into the receptacle, finger-tight.
4. Double-check the strip against the template pattern, remove the template, and insert the strip into the receptacles, using longnose pliers. Bend the common bar back.

The field replacement card is now ready for use as shown in Figure 72.

Note: Field replacement cards are authorized for use on 1401 systems and are now included on the initial spare parts lists. IBM Mechanicsburg cannot substitute field replacement cards for standard production card orders.

SMS Service Pointers

A CTDL single-shot card can be used to provide a delay for the 310 scope. Two SMS cards are available,

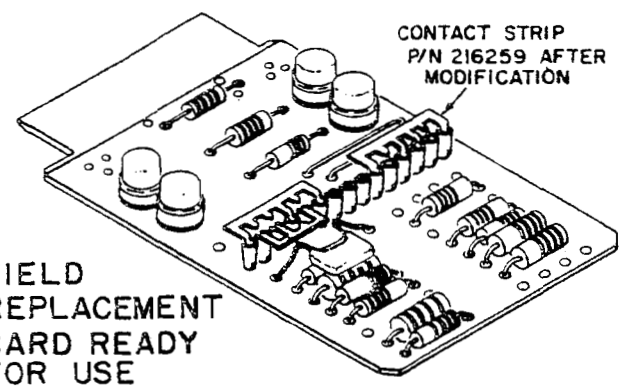


Figure 72. Field Replacement Card

one for +U lines (NC—, 371592) and one for —T lines (NB—, 371591). These cards will provide delays between 7.5 microseconds and 90 milliseconds. They can be plugged into any wired location.

CTDL triggers can easily be flipped by grounding one or the other of the output pins to aid in scoping circuits.

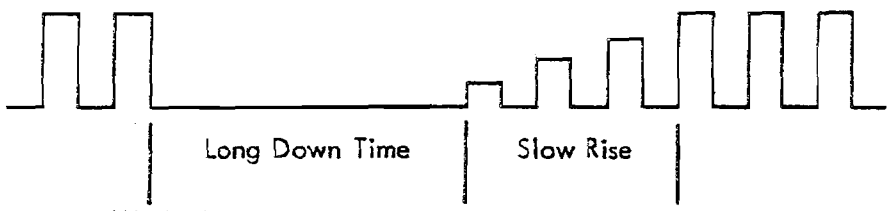
Care must be used when cleaning SMS card contacts. If the lubricant comes in contact with the clear plastic coating on the component portion of the card, the solvents in the lubricant can dissolve the plastic coating, which will act as an insulator if rubbed on the contacts. The following steps should be used to clean the contacts:

1. Apply the lubricant either directly to the contacts or indirectly by saturating any lint-free cloth or tissue.
2. Clean and lubricate the contacts by wiping with a moistened cloth from the leading edge toward the component section of the card.
3. Rub the contacts with a clean piece of cloth until there is no visible trace of lubricant. The cloth will darken if the contacts have not been properly cleaned.
4. Repeat the steps, if necessary, until the contacts are clean.
5. If you suspect that the contacts have been contaminated with the coating used on the back of the card, rub a pencil eraser over the contact. The clean contact will be bright, and the contaminated area very dull.

SMS back-panel wires are frequently routed around but not attached to an intermediate terminal. If the wire is pulled too tightly, or if undue pressure is exerted at the point of contact with the intermediate terminal, insulation damage or "cold flow" may result, shorting the wire to the terminal. This possibility should be considered when diagnosing hard-to-analyze troubles.

All removed SMS cards must be returned to the plants for analysis. Field return envelope, Form 920-8137, should be completed by the customer engineer for each SMS card replaced.

Many timing pulses are not square as one would believe. If trouble is encountered, square up the pulse as much as possible with card substitution. If trouble still exists, leave timing pulse and pursue other possibilities. *Sliver pulses* (very short pulses) that can flip triggers can be developed by slow transistors. Very close observance of scope pulses is needed to observe the presence and cause of these.



a. Works fine on core worst pattern.
b. Fails on some tape operation.

Figure 73. STAR Output Rise Time

Slow rise or fall after a circuit has been in one state or another for a long period should be considered on intermittent failures.

Example: Outputs of Main-star (Figure 73)

1. Works fine on core worst pattern.
2. Fails on some tape operation.

Voltage variation on the system varies the transit time of weak transistors. Use it to accentuate failures because of switching noise or timing.

Error Retention or Error Stop

A CTDL trigger (CW—PN 371543) installed in any spare socket can be used as an error- or condition-retention device by proper wiring of the set and gate pins. Because voltage wiring is already in place, many applications require only two jumper wires to turn on the trigger. In other cases, additional wiring and an additional card may be necessary to cause the proper condition to turn on the trigger.

The trigger output can be left unwired for interrogation by scope or can be jumper-wired to cause a machine stop.

In some cases, localizing the cause of an error can be retained by using a jumper wire and a diode from a given error latch to reset the delta-process latch. This prevents the machine from advancing to the next program step, and thereby preserves the machine conditions when the error is sensed.

Single-Cycle Mode

Many troubles do not allow you to set up a program loop and have to be approached in single-cycle mode. Although some troubles can be analyzed statically, many involve cycle or time controls.

When scoping in single cycle, use the delta-process latch rather than the start key as a sync. It is more stable.

To prove that a given block conducts, set up the scope as follows: + or — internal, depending upon the output level of the line you are checking, that is, + for a +U output. Set time/div. in the ms range, and stability to stop the trace from free running. Turn the intensity control to get a spot on the screen. Set the vertical amperes to keep full range on the scope face. With the vertical input probe free, adjust the trigger level so that as you move the vertical-position knob up or down (up for a +output), you get a sweep at a few volts less than the maximum of the line you want. Return the vertical-position knob to the base line, and connect the vertical probe to signal line. As you single-cycle to the point of failure, look for a trace on the scope. The slower the sweep time, the better the chance to see the sweep.

Branch-on Error

To facilitate checking the branch-on I/O error without running the reader, punch, printer, or tape; tie the error trigger or latch to its ON condition and run the branch program. These circuits can then be checked at 1401 speed.

Logic Errors

When troubleshooting logic or arithmetic errors, the B-field is usually altered and extra program steps are necessary to restore the B-field. For a tight loop, force a block operation as in single-cycle non-process in the run position. This insures the digit configuration remaining the same in a very tight loop. It can be checked in logic 31.03.21.

Repeat Cycle

Preventing the 1401 from advancing to the next cycle and repeating the same cycle can be useful when shooting main-frame troubles. The procedure is done by bringing up modifier control transfer and preventing the cycle latches from resetting. The program must be single cycled to the cycle preceding the cycle that is to be locked. The jumpers must be connected with power ON and the mode switch set to RUN. The start key then starts it looping. The circuits that have to be altered can be found on logics 32.44.31 and 31.20.11.

32.42.41

Repeat Instruction

To set up the 1401 so a single instruction can be repeated indefinitely without an intervening branch, the load latch can be forced on at the end of E-phase. The op code of the instruction to be repeated must be in 001. The load latch forces 001 into the address register, and then goes to 001 for the instruction. When errors occur that prevent a loop of the 1401, the error indication can also be used to turn on the load latch. The error indication always occurs after the error, so the circuit can be readily scoped. It may be necessary to prevent the 1 from being placed into the operation register.

Single Load

When a circuit is analyzed, sometimes multiple cards are tied to a single load card. Cards cannot normally be pulled to isolate the circuits. By adding a 500-ohm resistor, any card can be made a load card by tieing the output pin to the same voltage as the load card through this resistor. All cards in the dot function can now be pulled for isolation. CAUTION: Anytime a card or connector is pulled or inserted, power should be turned off.

Bias Checking

Always use a meter when bias checking. If the 3v buckboost rheostat is turned ON (or if the plug is not in a socket when power is turned ON or OFF), the circuit breaker for the marginal voltage can trip and no voltage indication is evident.