RAMAC 350 Restoration Project

by

David Nguyen, Viet Nguyen, and Jordan Villanueva

SENIOR DESIGN PROJECT REPORT – Phase II

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Project Abstract

For our senior design project, our group is responsible for the second phase of the RAMAC 350 Restoration Project. Last year, in May 2004, the first phase of this ongoing project was completed by a group of SCU engineers who designed a prototype microprocessor controller to successfully get the RAMAC 350's control arm to a selected disk and track. This year the goal for the second phase of the restoration project is to enable the read and write function of the RAMAC 350 hard disk drive.

Acknowledgements

This project would not be possible without the help and support of professors, fellow students, and help from the industry. Our group would like to extend our heart-felt thanks to the following people.

We greatly appreciate Professor Hoagland for all his advising. Without his guidance throughout the project, we would have been spending additional sleepless nights doing research for our design project.

We would also like to thank Halil Cirit and Bharat Sampath for the time they gave up from their graduate courses to help with our design. Whenever we got stuck, they were always there to help us work through to a solution.

We want to thank Patrick Connolly for helping us operate the RAMAC and also Donald MacCubbin for allowing us entry into the Mechanical Engineering Lab to use the high powered microscope for inspecting the RAMAC heads.

Our thanks also goes out to I.B.M./Hitachi for giving us the opportunity to work with the RAMAC. We wish to also thank IEEE for their funding support.

Lastly, thanks to everyone whose name we did not get to mention.

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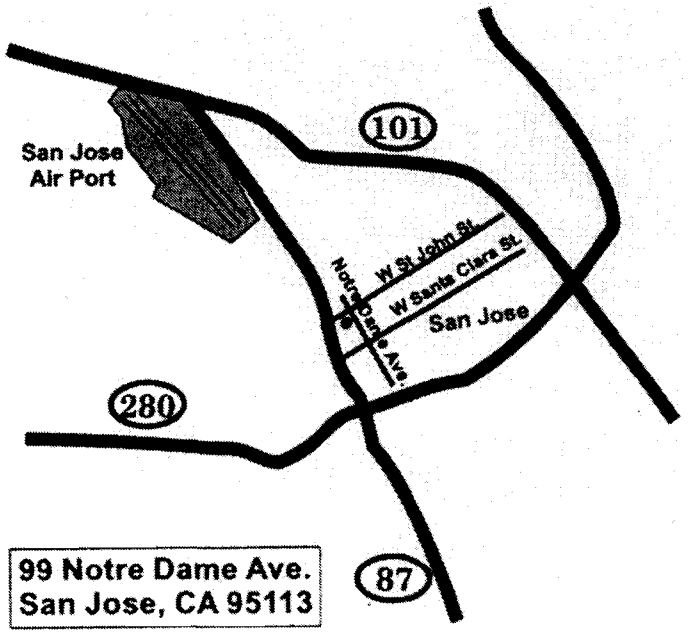
1.1 History and Background

The RAMAC 350 (Random Access Method for Accounting and Control) at Santa Clara University is one of IBM's first disk drives that led to revolutionizing the method of storing data. It was first created by a team, led by Reynold B. Johnson, in a small San Jose IBM research laboratory starting in 1952. This building is still intact as it was in 1952 today at 99 Notre Dame Street. The RAMAC was announced in 1956.



Over a thousand RAMAC 305s, the entire computer system with the RAMAC 350 storage system, were produced. In 1984, the ASME (American Society of Mechanical Engineers) recognized the RAMAC 350 as a Milestone. On April 28, 2004, nearly 20 years after, the IEEE (Institute of Electrical and Electronic Engineers) followed in recognizing it as a Milestone as well.

At this time, most data was stored conventionally by use of magnetic tapes. If magnetic tapes had a greater storage capacity than magnetic disks used by the RAMAC, why then, was it created then? To understand this, we must look at the advantages that magnetic disks have over magnetic tapes.

1) High capacity in reasonable volume

At this time, the cost of storage on magnetic disks was coming down, so research on the matter was possible. The RAMAC 350 was storage in a smaller volume. The RAMAC 350 was like a 55-gallon oil drum versus a magnetic tape machine that took up a small room.

2) Short access time

The access time of the hard disk drive was less than a second with its random access method, which zeroed the control arm to the specific track on a disk. The magnetic tape was prone to slower access time with its slower, sequential access by fast-forwarding or re-winding to the location without the same accuracy and speed. That was if a user was lucky enough to have the correct tape already loaded, several more minutes would be added onto the access time, or else the machine would have to unload the tape to find the correct tape to be loaded.

3) No head-contact

A major problem with tapes was that the read/write heads actually had contact with the tape. In time, the magnetic tape would wear down and need replacement. The RAMAC disk drive avoided this destructive contact by having the head "flying" over the disk at a distance of 1 mil.

1.2 Motivation

The RAMAC is a significant to the history of the City of San Jose, its birthplace, since it led to a huge contribution in magnetic disk storage technology that sparked the industrial boom here in Silicon Valley. With applications made possible by this magnetic disk storage system, we have been able to overcome major technological milestones. It is due to these significant contributions that our group wishes to take part in the restoration of the RAMAC disk drive. We want to preserve this historical landmark to better inform the public of the legacy of the magnetic disk drive industry.

1.3 Literature Review

Currently in today's technology, there is no system like IBM's RAMAC 350 hard disk drive. Being the first hard drive ever, there was nothing to compare it with at the time. Builders then had to improve upon the technology before finally building the next generation model, which could be comparable. However, a new disk drive product cannot be directly compared to the RAMAC given the advances in technology over 50 years.

Today, not a single hard drive is completely like the RAMAC in structure and performance. The hard drives are now much faster. Disk drives are dual layered and record at approximately $50x10^6$ higher density than the RAMAC. Spinning at a speed of 1,200 RPM, the RAMAC's seek time is measured at 600 ms. Today's hard drive can spin at 15,000 RPM with a seek time of 3.5 ms. Also, the overall diameter of the RAMAC is 24 inches versus the modern desktop hard disk diameter of 3.5 inches and laptop hard disk at 2.5 inches. The RAMAC has a transfer rate of 80 Kbit/sec versus today's 1,100,800 Kbit/sec. In addition, the head-to-disk spacing on the RAMAC is 1 mil versus the .5 on today's drives.

1.4 Project Objectives

In our senior design projects, there are two objectives: our group senior design objective and the long run objective of the entire project. Our group objectives are to successfully enable the read/write function of the RAMAC 350. Our design will consist of the use of Basic X coding in conjunction with read/write analog circuits using CMOS switches to control the current pulses sent to the heads. We want to make the entire system "user friendly" so that a user can interact with a simple interface so that they can read data off tracks or write to a track on a disk of the RAMAC 350.

The long-run goal of this project is to actually get the entire system functional. Our group would very much like to complete this task. With the fundamental design techniques proven, the disk drive will be repackaged and with added safety features for use by the public. With the entire system functional, we will be able to return the hard drive to the City of San Jose as a historical artifact for public education and use. We hope for it to be accessible by everyone in the world via the internet so that they can read/write data while watching the mechanics of it through a web cam as it performs the task specified by the user.

2.0 SYSTEM LEVEL . . .

2.1 Physical Sketch

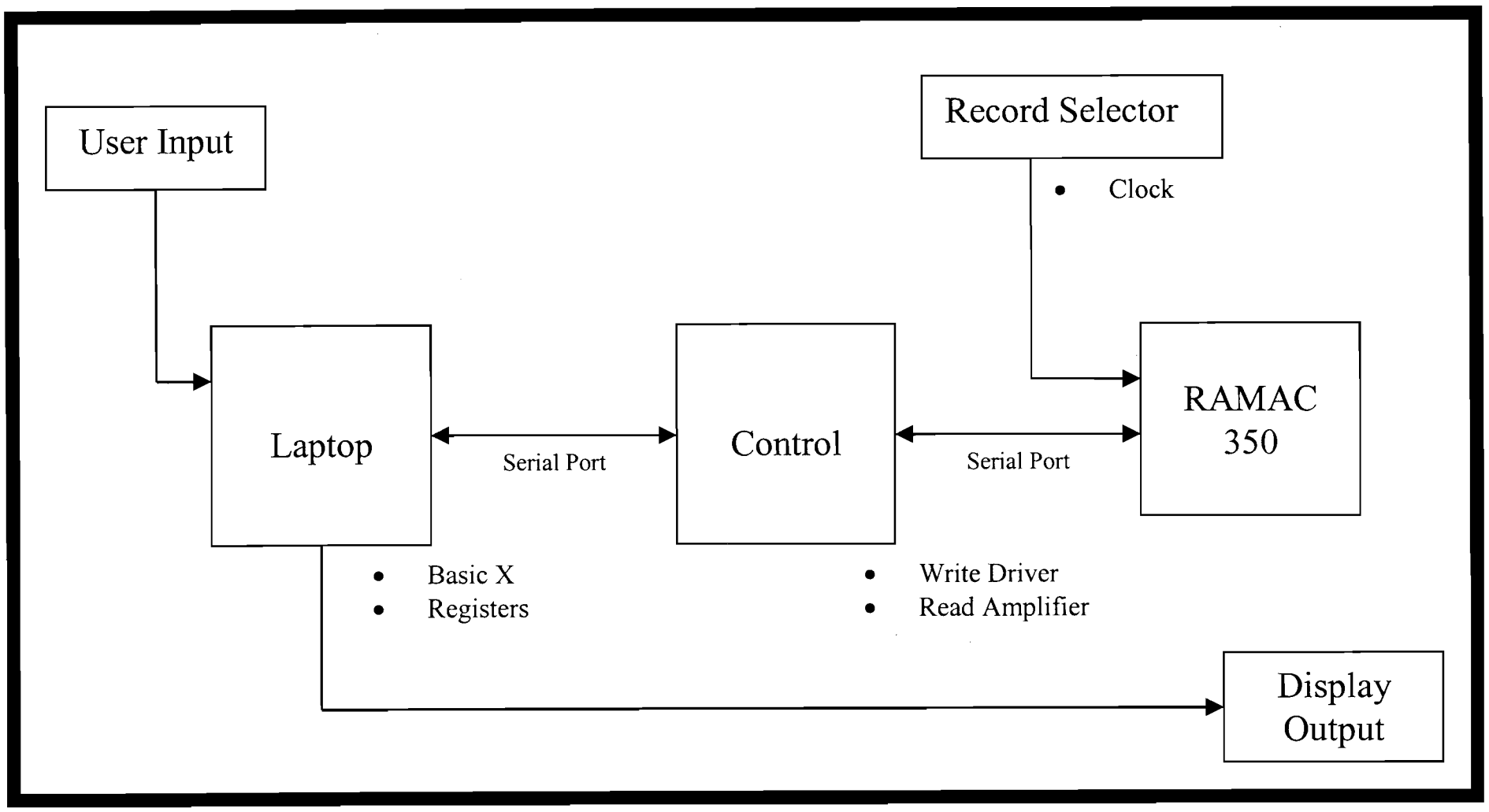
2.2 User Scenario

2.3 Challenges

2.3.1 System Constraints

2.3.2 Risks and Mitigations

2.1 System Sketch



2.2 User Scenario

Although the RAMAC 350 was meant only for commercial use by companies for accounting and financial purposes, our group is attempting to make it user friendly to demonstrate the operational behavior of the first disk drive. In order to allow maximum usability, the hard drive control system should be simple enough so that users can interact with a simple interface to store and retrieve data from the disk drive. We want a user to be able to write data to a known address X and move to another address Y to retrieve known data. After this, the user should be able to go back to address X and be able to retrieve the same data they had entered earlier. Embedded in this user scenario are the goals of our project. The main goal of our group is to successfully enable the read/write function of the RAMAC 350. The ultimate goal is the usability and accessibility of this project to a large audience.

2.3 Project Challenges

2.3.1 System Constraints

With the RAMAC Restoration Project, there are three main constraints. The first one is time; we must manage our time wisely in order to bring out the best result. We have to wait for a long period to receive parts and materials that we need.

Another constraint is the lack of resources, such as the magnetic heads. If the two magnetic heads we possess do not work, we will have to delay our original plans and then try and see what we can use from modern technology as a substitute since we mush develop new approaches rather than go back to old ways.

The next problem is to actual designing and testing the ac to dc and switch circuits. They look great on paper, but then again, what we do on paper and on computer simulators in lab are just ideal circuits under ideal conditions. To overcome this problem, we must first, check and see if there are parts that meet our specifications and then see if those parts will fit and work on a breadboard. We will have to tweak and adjust the circuit accordingly to fix problems that may be encountered in this process due to real world conditions, if any. If they do not work on a breadboard, then we must fabricate the boards and solder the parts on.

2.3.2 Risks and Mitigation

The only known risks that our project has are with the limited number of head elements we are working with. There is a risk that they will not work as they did as new. The only solution is to fabricate another head for our conditions. This would require support from IBM/Hitachi and even if all our circuits work correctly, the project may not finish in time.

3.0 SUBSYSTEM LEVEL . .

3.1 Subsystem Roles
3.2 RAMAC 350 Heads
3.3 Circuit Design
  3.3.1 AC to DC Circuit
  3.3.2 CMOS Switch Circuit
3.4 System Spec. and Coding
  3.4.1 NRZ vs. NRZI
  3.4.2 Change in Plan for Coding

3.1 Subsystem Roles

* Refer back to System Chapter 2.1.

Laptop

- The user interface that receives input commands from user and outputs through display.
- Uses Basic X.
- Serial port.

Control System

- Write driver to send two-level current waveforms to heads for write.
- Read amplifier to detect and amplify the small signals from magnetic flux changes on disk.

Record Clock

- To tell circuit to write as soon as it detects start of a sector.
- Tells circuit to stop writing when it detects end of a sector.

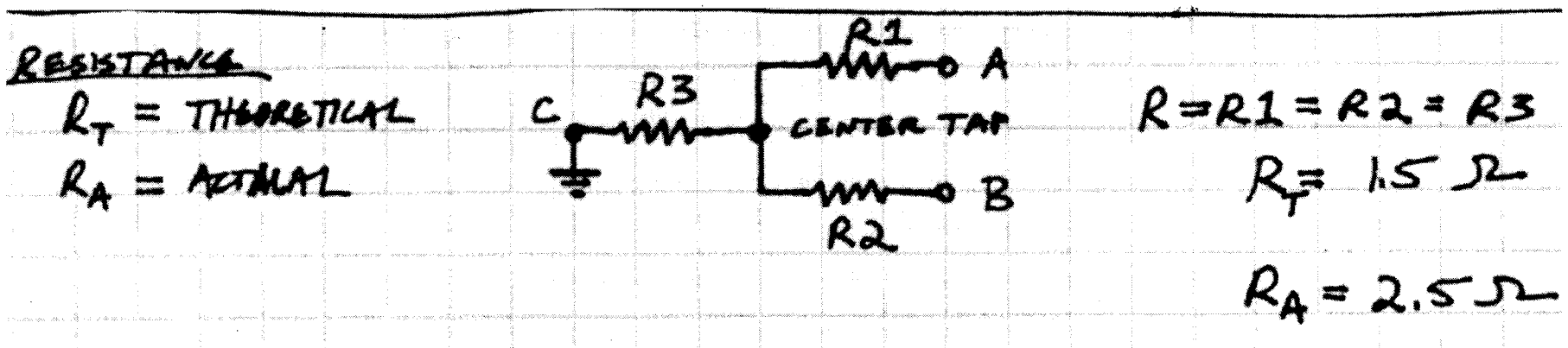
RAMAC

- The RAMAC storage itself. Our design is to enable its read/write capabilities.

3.2 RAMAC 350 Heads

Read/Write and Erase Heads:

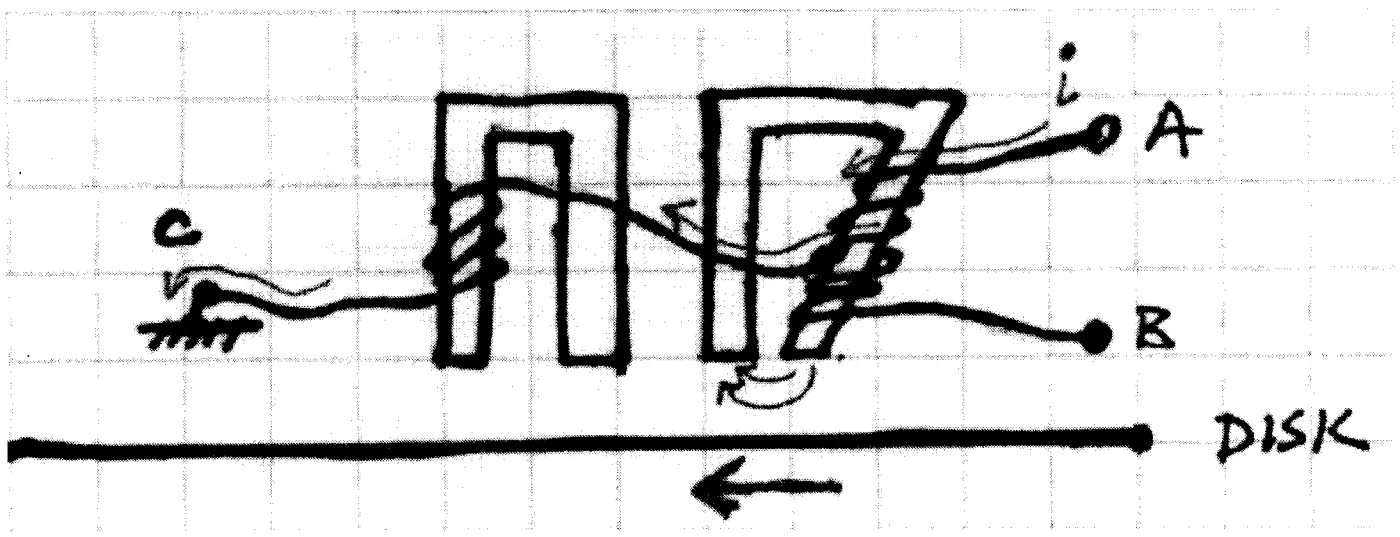
Since the RAMAC 350 disks are two sided, the control arm has two Hydrostatic air-bearing heads. One head to read the top of the disk, the other to read off the bottom of the disk. The head can support a maximum current of 200mA through it. There are three taps on the head. We shall call them arbitrarily taps A, B, and C. Taps A and B are used for sending current pulses through to tap C, which is always grounded. There is also a coil for each tap. Each coil has a resistance rating of 1.5 ohms according to the manual. However, we will be using the resistance of 2.5 ohms per coil that we have actually measured ourselves. This is likely due to contact resistance changes on the leads over time. Below is a simple circuit diagram.



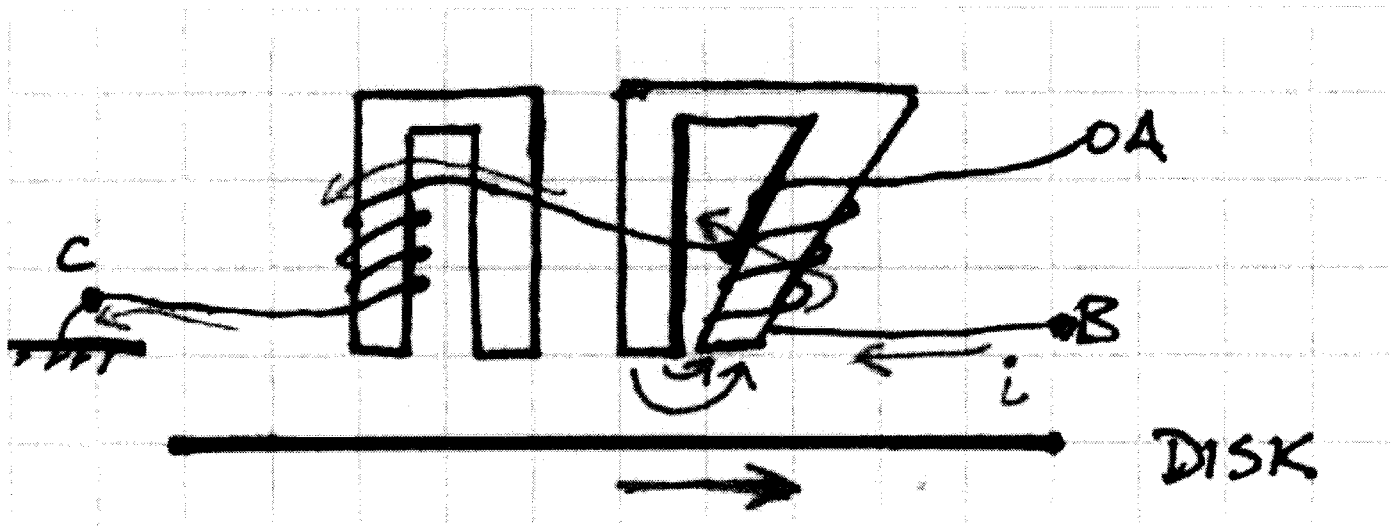
Taps A and B actually share one coil with each other, but there is a center tap on this coil that runs to tap C. Bifilar windings are used to achieve this. The head itself is actually a name for the entire unit. Contained within this head unit are a Read/Write head and an Erase head. The Read/Write head is recognizable since it looks like a pinched horseshoe. The Erase head is larger than the read/write head and is not pinched. Both have the same gap of approximately 1-2 mils. Coils A and B are wrapped around the Read/Write head while coil C is wrapped around the Erase head. Refer to Appendix A for more details.

Magnetization of Disk:

The head writes to a disk in the RAMAC via current two-level current wave forms longitudinally. The tap that we send current through dictates the direction of magnetization on the disk which we shall refer to as magnetization to the left and right. Let us assume that we send current through Tap A. Naturally, current flows from higher to lower potential, so it goes from tap A through the coil and through coil C to ground. Because of the right hand rule and the orientation of the turns on the Read/Write head from A to the center tap, a magnetic flux is induced in the left direction as shown below. Thus, the Read/Write head magnetizes the disk to the left as shown with the green arrow on the disk.



If instead, the current were sent through Tap B, a magnetic flux is again induced, however in the right direction instead of left. Therefore, the result is magnetization of the disk to the right.



The purpose of magnetizing left and right is to create flux on the medium for voltage pulses to be detected during read back. This section will be discussed later on in the code section where voltages are read back and converted.

Head Stabilizers:

Refer to Appendix B for diagram. The RAMAC head must be close enough to the disk that it can read and write to the magnetic disks. According to the IBM manual, the manufactured distance between head and disk is 1 mil. To achieve this, the RAMAC head has three air pressurized pistons that push back against the control arm and therefore bringing the head closer to the disk. What prevents the head from coming in contact with the disk in this process are the six air jets that are on the bottom of the head, facing the disk surface. As the pistons push the head closer, the air jets are there to push against the disk simultaneously to direct a force opposite to the piston so that the head is able to "fly" over the disk with out crashing the RAMAC hard disk drive. More detailed pictures and diagrams of the head can be found in Appendix A within the small bubble close up of the Hydrostatic air-bearing head.

Testing Available Heads:

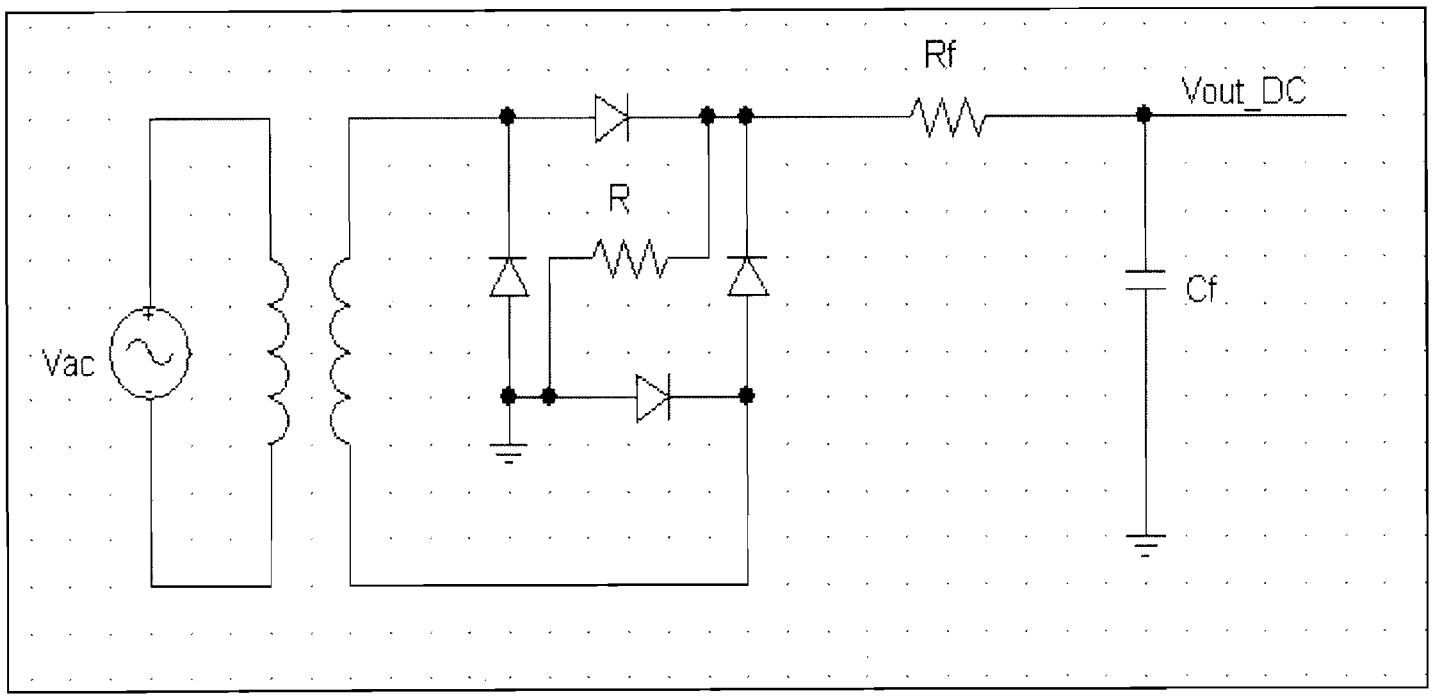
Originally, IBM had provided our design team with 6 RAMAC heads. We were told that these were one of the last existing RAMAC heads available and that locating more would be near impossible. If they were all to fail, our design team would be stuck at a dead end. With the insufficient time allowed before the deadline of the Senior Design Project, waiting for the arrival of replicated of the heads by a company would be impossible. After testing visually with the

naked eye, two of the six automatically failed since they were noticeably damaged from previously being smashed against a magnetic disk. Both had no air jets left from being smashed. The last four were carefully inspected thanks to the assistance of the Donald MacCubbins. He allowed us to use the power microscope in the SCU Mechanical Engineering Lab for this visual inspection. From this visual test via the microscope, our group was able to determine that only two heads were suitable to be used for our project. Fortunately, one is an upper surface head and the other a lower surface head. It should be noted that the erase head pre-erases the track before writing. Therefore, it must always be the first head a point on the disk sees as it rotates. The other two failed due to one being corroded and crumbling while the other was smashed shut so that no gap existed anymore. Refer to the microscope pictures of the four magnetic heads in Appendix B.

3.3 Circuit Design

3.3.1 AC to DC Circuit

In the AC to DC circuit below,



the Step-Down transformer is used to lower the output voltage to a usable value for the write circuit. Transformers require a varying flux to work so this is why they are used with AC voltage sources and not DC ones. This can be seen with Faraday's law which states that a changing magnetic flux will induce an EMF, which basically is a voltage, in a coil. If a coil has N turns, then the induced EMF is:

$$\varepsilon = -N \Delta\Phi / \Delta t$$

As a result, the changing flux creates a voltage in a coil.

Equation for the voltage in the primary coil: $V_p = -N_p \Delta\Phi / \Delta t$

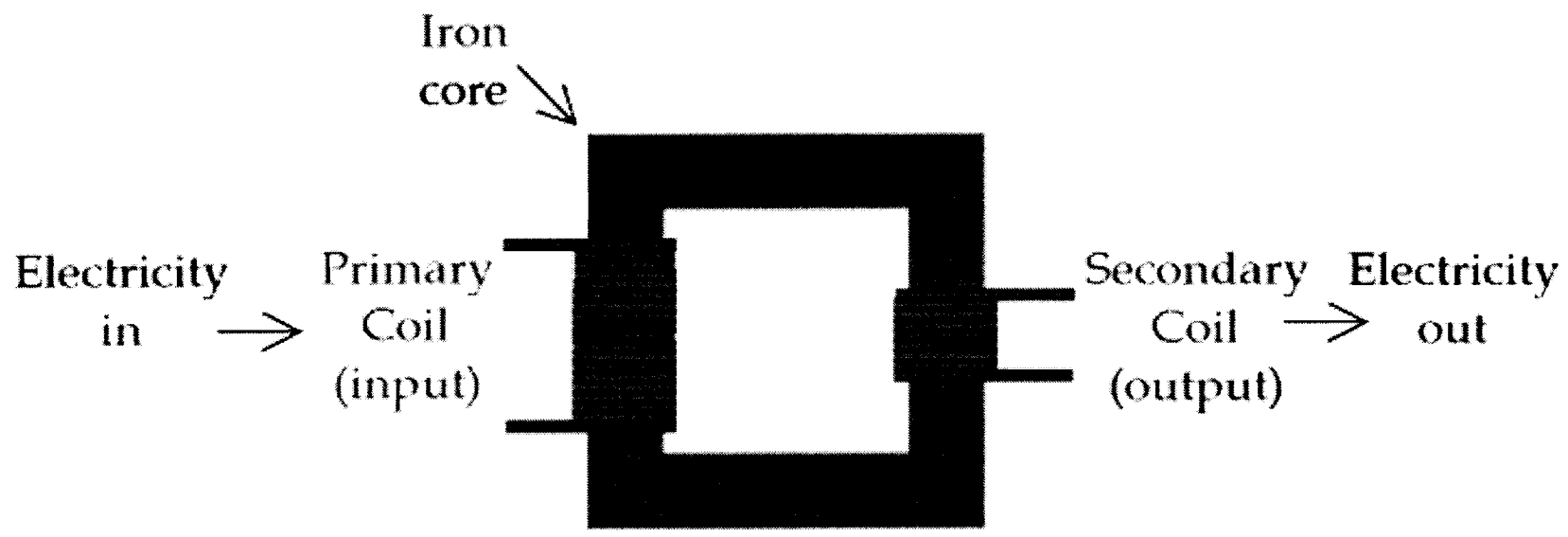
Equation for voltage on the secondary coil is: $V_s = -N_s \Delta\Phi / \Delta t$

Combining these two equations will give us a relationship between the primary and secondary coil.

$$V_s / V_p = N_s / N_p$$

The voltage source we are using is at a voltage too high for us to use normally. The input voltage is rated at about 400V and we need a voltage of about 20V. In order to lower the voltage to the 20V that we need, the coils on the secondary coil must have 20 times less turns of wire than the primary coil. This runs true because of the equation above.

The top image below helps to illustrate what a step-down transformer usually looks like and where the input and output voltages are taken at.

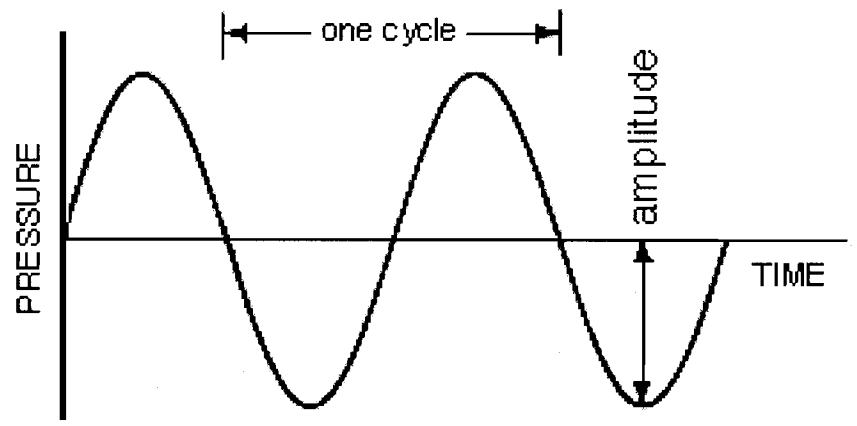


However, decreasing the voltage does not decrease the power consumption in the circuit since it follows the Conservation of Energy Law. Since P = IV, then the voltage, current, and turn ratios must stay equal ➔ same power consumption.

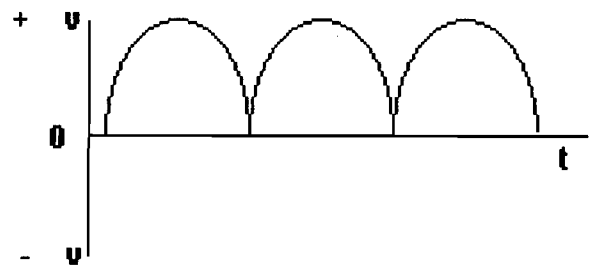
$$P = V_s I_s = V_p I_p$$

$$\text{So,} \quad V_s / V_p = N_s / N_p = I_p / I_s$$

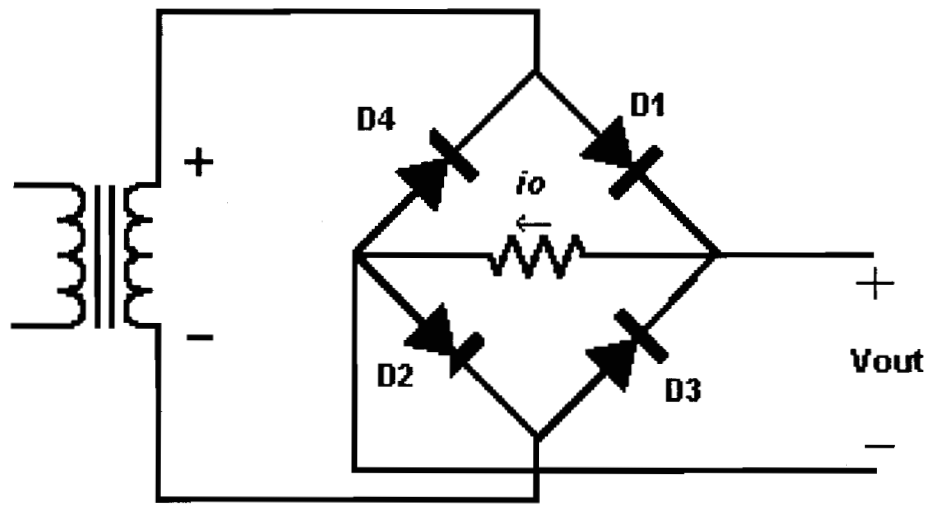
We have seen how the transformer works, but the bridge rectifier is needed to achieve full-wave rectification. Originally, a sine wave has an average of 0.



As seen from the wave image above, the amplitude of the negative and positive cycle are equal so taking the average of them would result in a zero value. By rectifying it, a full-wave is achieved. (*See image below*)



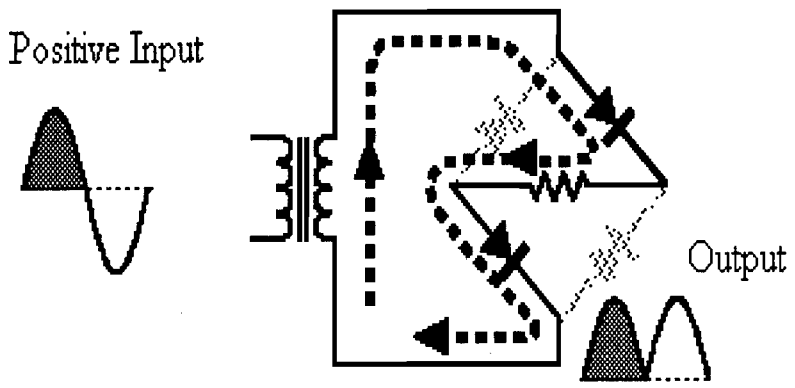
Now the average is a positive value that can be used to turn it into a DC power supply. The full-wave is accomplished by the diodes forcing the current to travel through the resistive load in the same direction on both the negative and positive phases of the cycle. As a result, the output voltage's polarity is always the same.

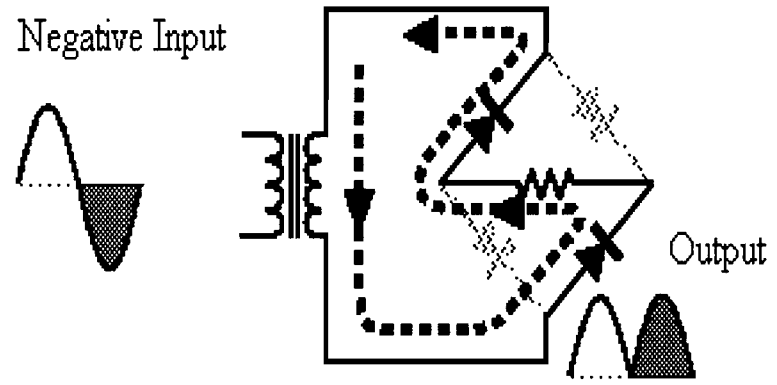


When the voltage wave is on the positive cycle, diode D1 is forward biased and D4 is reversed biased. The potential at the anode of D1 will be greater than the potential at its cathode. This will allow the current to flow through D1. The same potential goes for D2 also and this will allow the current to flow through D2 and the resulting output voltage will be positive.

When the voltage wave is on the negative cycle, diodes D3 and D4 will be forward biased and this will allow current to flow from the negative terminal of the input, up D3 and up D4, and then to the positive terminal of the input. However, the current that flows during the negative cycle is negative so this makes the output voltage positive even though it flows in the opposite direction.

The picture below on the left illustrates the direction of the current and the output during the positive cycle and the image on the right illustrates the same concept but during the negative cycle instead.

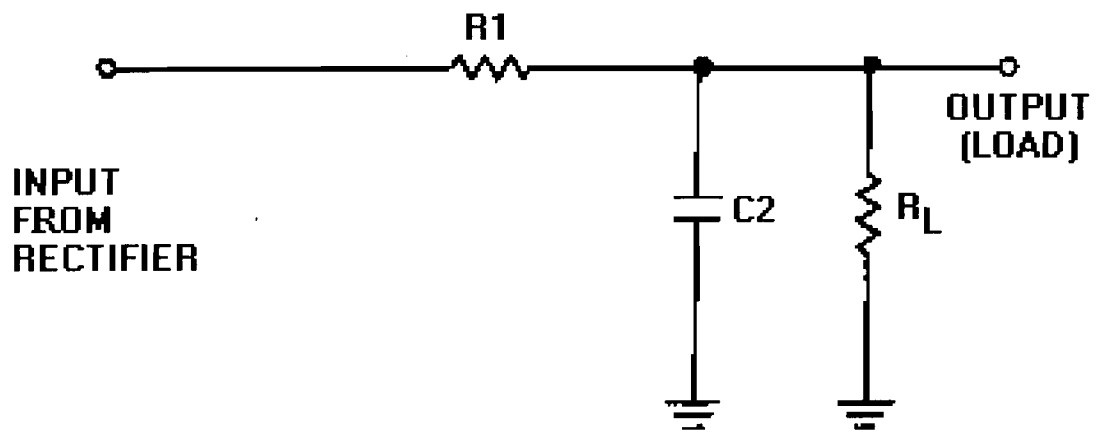




Since full wave rectification is achieved, only one more step is required to make it a DC voltage. The last step requires a RC low-pass filter (LPF). The RC LPF is good for our application because the load current is small and constant. Since we want a steady DC output, the capacitor must charge up as fast as possible but discharge as slow as possible. This requires the low-pass filter to have a large time constant in order to keep the capacitor from discharging rapidly. So we basically want a high average output voltage and low ripple voltage to have the best DC output.

*(**Er** is the ripple voltage and **Eavg** is the average output voltage)*

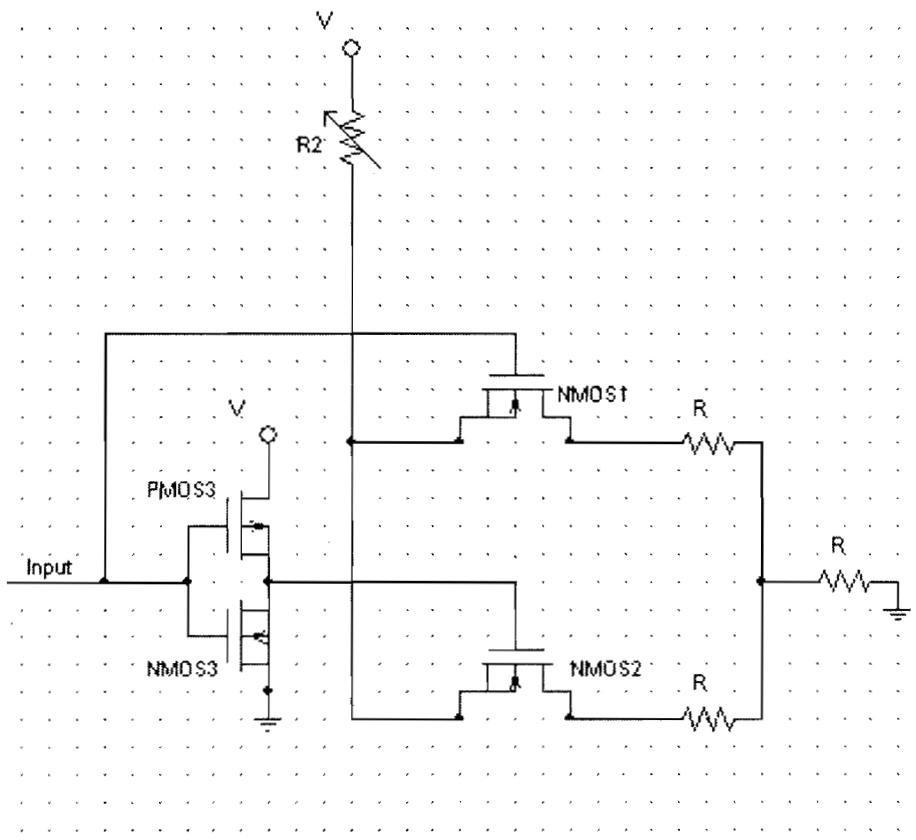
In the RC low-pass filter below,



the capacitor acts as an infinite impedance so the DC component of the output voltage is passed to the resistive load, which is the resistor in our switch circuit. The Eavg (average voltage) is then used as the bias point to create the need write current of 160-200 mA in the switch circuit.

3.3.2 CMOS Switch Circuit

The schematic below is our CMOS switch circuit. It is used to switch the write current through either the bottom or top resistor. The current will create the needed magnetic flux in the head to write either a 0 or 1. The reason for writing a 1 or 0 is because the user input will be converted into binary form for the simplicity of purpose.



Switch Circuit

MOS devices can only be used as switches only when it is in the linear region. This means that the device needs a voltage great enough to turn it on but not put it into saturation. In order for the device to turn ON: Vgs > Vt for a NMOS and Vgs< Vt for a PMOS. So to turn on a NMOS device a voltage of Vdd (+20V in our design) is applied to the gate of the device. To

turn a PMOS device on, a low potential is applied. This potential is usually ground (0V). Using the PMOS or NMOS by itself will limit the signal voltage range that can pass through. This is why our circuit utilizes CMOS transmission gates so that signal range will not be a problem.

PMOS3 and NMOS3 when used in series act as an inverter. The PMOS will be on the top and the NMOS will be on the bottom. Both the drains of the device must be connected together for the device to work properly. The reason why the PMOS must be on top is because it can reach all the way up to Vdd and the NMOS is on the bottom can reach all the way down the lowest potential.

Since this switch works with binary values, 1s and 0s, we must assign Vdd as 1 and ground as 0. This will allow the switches to work properly. W

Case 1) When the input is a 1, NMOS1 will turn *on* and PMOS2 will be *off*. When the 1 reaches the inverter, it will become a 0. This 0 will turn *on* PMOS1 and keep NMOS2 *off*.

Case 2) When the input is a 0, NMOS1 will turn *off* and PMOS2 will be *on*. When the 0 reaches the inverter, it will become a 1. This 1 will keep PMOS1 *off* and turn NMOS2 *on*.

In both of these case, a current of 160-200mA will flow through the top resistor if the binary input is a 1 and through the bottom one if the input is a 0.

3.4 System Specifications and Coding

3.4.1 Brief Summary of Specifications

The maximum capacity of the RAMAC 350 is 5 MB. This storage is divided among fifty disks. Each disk is twenty-four inches in diameter. For a constant data rate, the maximum capacity per disk surface is obtained when ID = ½ OD. The disks are made out of aluminum and the medium is an iron oxide particulate known as Fe_2O_3 or common iron rust. Each disk is magnetized on the top and bottom, allowing data to be written on both sides. On each side of the disk, there are one-hundred tracks or 500 sectors. In each of these sectors are 100 characters or bytes. Although the capacity of the RAMAC 350 is minute under today's standard, during its time, it was capable of storing 5 MB. Compared to the hard disk drives of today that run at speeds of up to fifteen thousand rotations per minute, the disks in the RAMAC 350 spin twelve and a half times slower at 1,200 RPM. Refer to chart on Appendix C.

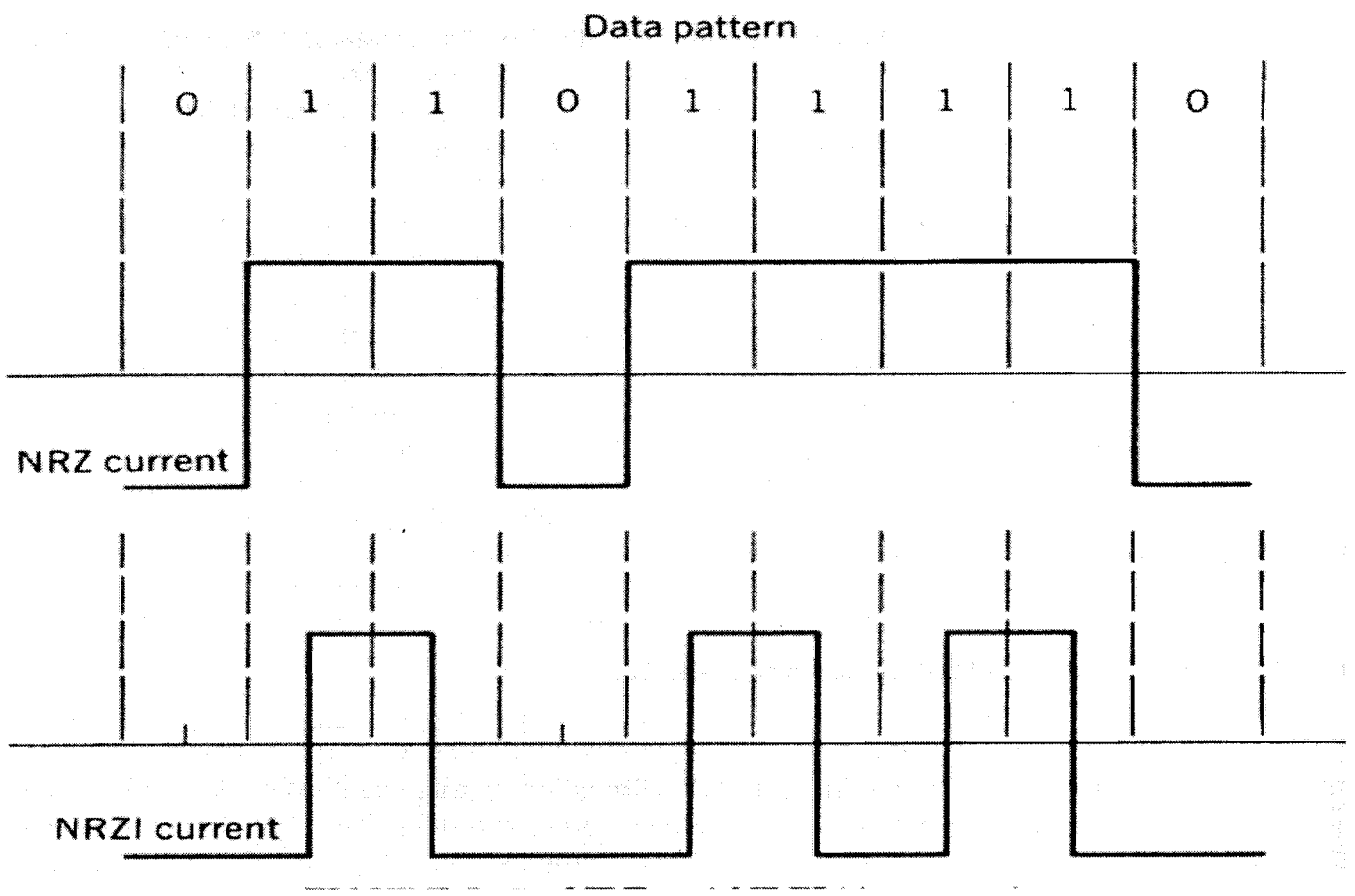
Because the design calls for the user to use a standard keyboard, the character coding needed to be altered from its original code. The RAMAC 350's character coding allocated eight bits to each character; six of which are actually used for the character itself. The two other bits in the string were used for the spacing bit and the error checking bit. The spacing bit, which came at the beginning of the 8-bit character string, was used as a reference in conjunction with a clock. This enabled the control system to determine when to start reading a character string and when to stop. The error checking bit that came at the end of the string basically switched high or low to make the 8-bit string have an odd number of 1 bits. If a character string with an even number of 1's were passed in the machine, it would output an error.

In contrast, our character coding will utilize a 10-bit string with two bits for spacing and error checking, and the rest for the character itself. The reason why eight alphanumeric bits were

assigned to the character instead of six was because eight bits allowed for more characters to be stored. In binary, two to the eighth power is two hundred fifty-six. This means that our code can hold two hundred fifty-six different characters from the ASCII table. Not only does this include numbers, upper case and lower case letters, characters, spaces, tabs, and returns, it can accommodate Spanish characters that use contains accents. The RAMAC 350's six bit coding allowed for sixty-four different characters. However, forty-eight of these sixty-four were only used; ten for the numbers one through nine, twenty-six for the upper case letters from A through Z, and twelve more for common punctuation such as a period, exclamation mark, or comma. The ASCII table for this type of character coding can be found in Appendix D.

3.4.2 NRZ vs. NRZI

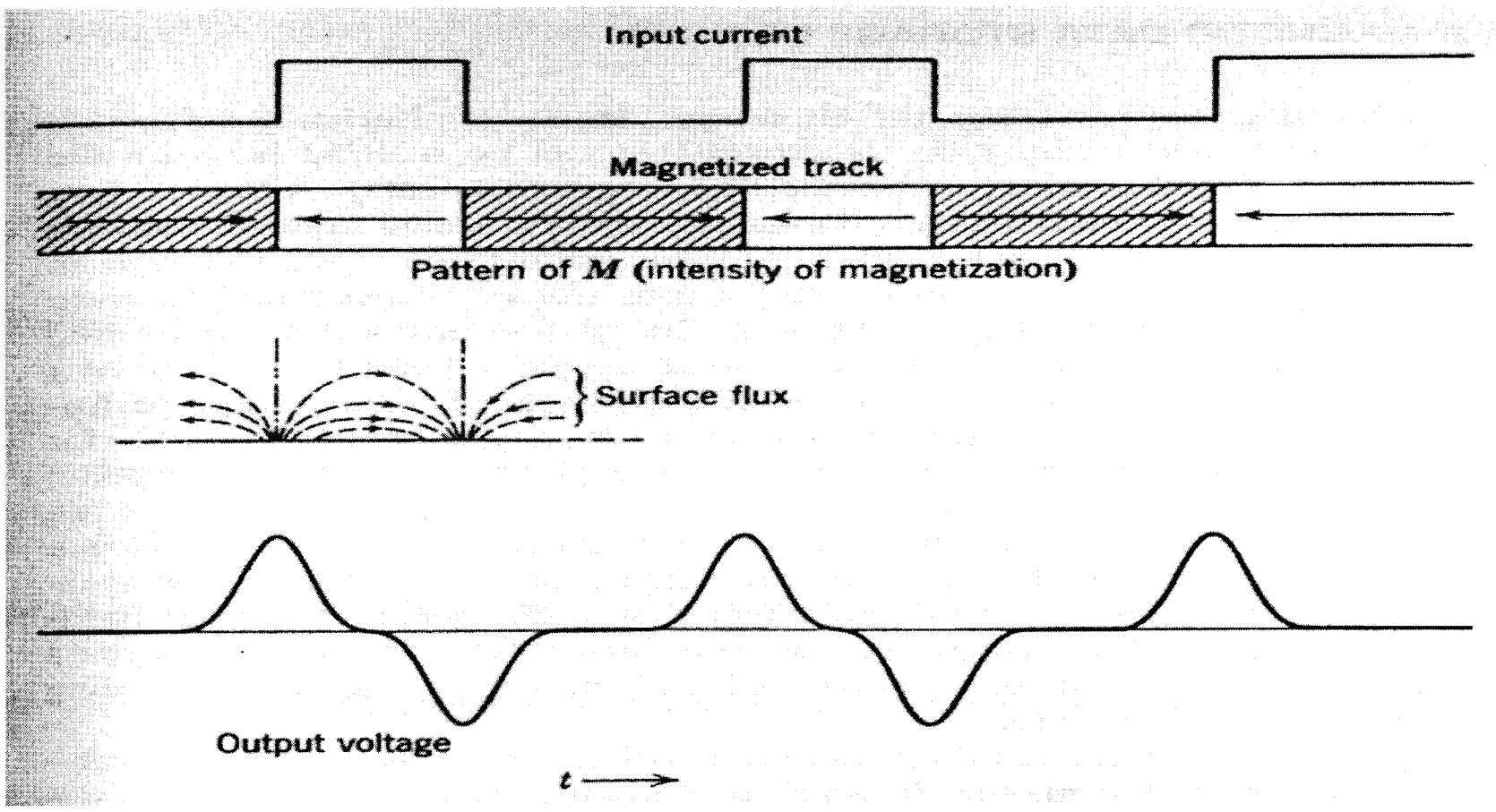
The two different methods that we looked to encode the write current to binary were NRZ and NRZI.



NRZ is the acronym for Non Return to Zero. In this type of coding, there is a transition in the write current whenever there is a difference in bit sequence, for example, 0 to 1 or vice

versa. The drawback of NRZ is that it has a problem reading a string with a consecutive number of 1's. When used with a clock, there is a difficulty with clock recovery, and the system may not know how many 1's are in the string. The alternative and the method chosen for the design is NRZI. This code, which stands for Non Return to Zero Inverted, differs from NRZ in that there is a transition in write current whenever there is a 1. If the machine reads a 0, then the write current stays at its previous state. The reason why NRZI will be implanted into the design is because unlike NRZ, it can be used to read a long string of consecutive 1's without clock recovery being a problem.

The binary sequence in the 10-bit string will affect four different elements. Using NRZI coding, the string will alter the write current. Whenever there is a 0, the write current will stay at its current state. Whenever a 1 is passed in the machine, the write current will make a transition. It is important to note that in NRZI, the current only transitions on the positive edge of the clock.



This current will create a magnetization on the medium of the disk as seen in the figure below. When the write current is low, it will orient a bar of magnetization in some defined direction. When the write current is high, it will do the reverse and orient a bar of magnetization in the

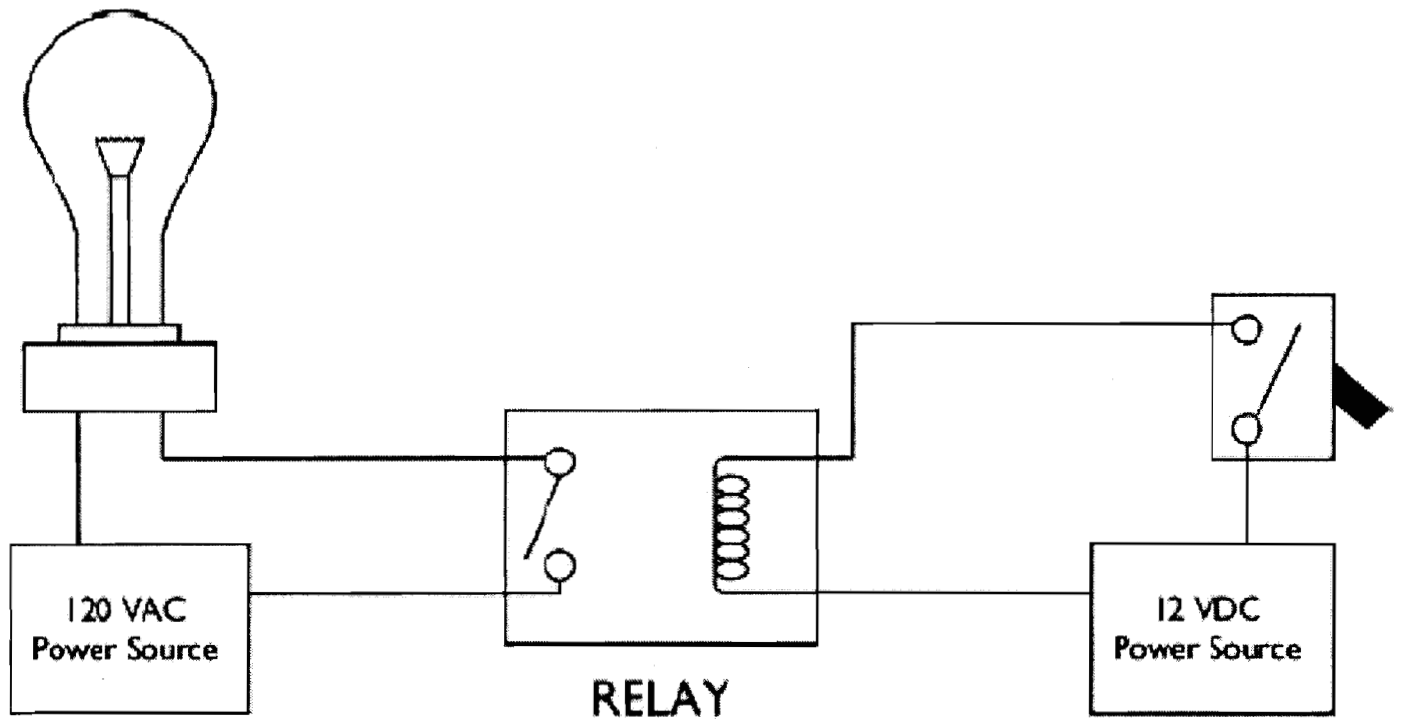
opposite direction. In turn, the magnetic flux on the medium will be affected. Whenever two north poles of magnetization are facing each other, the magnetic flux will flow out of the medium. The magnetic flux will flow into the medium whenever two south poles of magnetization are facing each other. Lastly, the write current will induce a voltage that follows the patterning of the magnetic flux. The voltage will be high when the magnetic flux flows out of the medium and low whenever the flux flows into the medium.

3.4.3 Changes in Plan for Coding (Winter Quarter Update)

After further speculation for the character to contain 10-bits, our group may have to reconsider switching back to the old machines coding of 8-bits per character. The main reason for keeping the system at 8-bits is because of the spacing of the sectors in relationship to the 5 equidistant sensors on top of the drum. Recall that in the original RAMAC, each sector contained 8 bits and there are five sectors in each track. If we were to increase the bit size to 10 bits, it would complicate the timing with the sensors on the top of the drum since those devices determine when the system reads and writes. Furthermore, a 10-bit coding scheme would mean a decrease in the total amount of characters that can be stored onto the RAMAC. By increasing the bit size to 10 bits per character, each sector could only store 80 characters as opposed to the 8-bit coding which would allow for 100. However, by limiting the code to 8-bits, the system will only be able to read a total of 64 distinct characters instead of the 256 that we would have like to have implemented using the 10-bit code scheme.

An optional write circuit would include relays to replace the power transistors that act as switches in our original design. The relays reacts to a certain threshold current or voltage. In our

circuit, once this threshold has been passed through the relay, it generates and magnetic force that actuates the switch mechanism. An example of how the relay works is pictured below.



For our design, we may want to use solid state relays that act when one part of the device reacts to sensing the light of another part of the device. When this occurs, the switch is essentially turned on. These relays are used when the circuit is introduced to electrical noise, therefore eliminating electrical noise. In addition to this, solid state relays have low electromagnetic and radio frequency interference, and even have fast response times. But, before we construct another write circuit using relays as switches, the group has agreed to first priority is to test the performance of the power transistor design before any other design is made.

4.0 SYSTEM RESULTS . . .

4.1 Test Plan – Fall Quarter

4.2 Revised Test Plan – Winter Quarter

4.1 Test Plan – *Fall Quarter*

Before the design can move onto the next phase, which is developing a read circuit for the device, the write circuit must be tested for its performance. Magnetic viewing film and magnetic particles have been purchased for the sole purpose of testing to see if the heads still produce the magnetic flux required.

The experiment will be done as follows: To represent the one mil gap between the head and the magnetic disk, Mylar film less than 1 mil in thickness will be placed over the magnetic particles. Then, the head will be connected to the write circuit and placed above the Mylar film. Short bursts of 160-200mA of current will be passed through the heads which should create some type of magnetization. Finally, the magnetic viewer film will be laid onto the surface to detect if there are any magnetic patterns formed. From this test, we can determine if our write circuit is suitable and regulate the current for the sufficiency of the design.

Another test to be performed is more of an end of the year goal. The user interface, either a desktop PC or laptop, will be used to test if the restored RAMAC 350 can properly read and write different characters. For the test, a user must be able to write a word or a phrase onto one of the disks then perform either a read and write on another disk. Finally the user will come back to the disk that he or she had previously written on to see if the display on the computer or laptop outputs the correct word or phrase. Once this process is complete, an error checking code can be implemented into the design for instances when one or more bits are written or read incorrectly.

4.2 Revised Test Plan – *Winter Quarter*

After considering the amount of time our group has left, the test plan has been revised in the Winter Quarter in order for the group to meet deadlines that have changed for the entire RAMAC Project. Due to the recognition of the RAMAC by IEEE as a milestone in Magnetic Disk Recording and the early graduation of the RAMAC design team, the project's completion date has been moved forward to the end of March.

As stated in the Fall Quarter, the first step in our test plan will be to test the write circuit for its performance. However, we will not be using a magnetic view at all, due to time constraints. Instead, we will connect the write circuit to a replica circuit representing the read/write heads. This will assure that the heads do not get damaged if the current applied to the circuit accidentally surpass the manual's suggested rating. This way, only inexpensive resistors will be blown due to instrumentation errors or calculation errors in the theoretical stage of the design were wrong. We will follow the specs found in the RAMAC manual and try to drive currents of 160mA - 180mA through the replica head circuit to see if the unit can handle it.

Following the success of this test, we shall then reconnect the heads back onto the RAMAC control arm and begin generating the 10ms pulses of current in an attempt to magnetize a disk track. To verify that the test is successful, we will expect to see voltage pulses between 100mV - 200mV read back from the disk track we just wrote. Because of the simplicity of reading back of pulses, the read circuit we had planned to design is no longer necessary.

The final test in our test plan, the full functionality of the RAMAC, will stay the same with no changes. It will just have to be completed earlier due to the upcoming milestone recognition by IEEE.

5.0 TEAM MANAGEMENT

5.1 Design Process
5.2 Major Deadlines
5.3 Work Distribution
5.4 Budget Summary

5.1 Design Process

On issue concerning the design process that we will be using for our Senior Design Project at Santa Clara University, there will be a slight modification of the entire engineering process. As of the FALL 2004 quarter, here are the current steps we have accomplished or are in the process of completing.

Customer Need

At the current time, there is no need for such a machine for business or consumer purposes. However, the customer we are thinking of is not in that category. We instead focus on the need of the product in the sense that it is a historic artifact that will further enrich the understanding of the history of this historic artifact and its impact on the City of San Jose as well as the impact on the hard disk drive storage technology that we have today.

Conceptual Design

Our conceptual design was completed in the fifth week of this fall quarter. It was in our problem statement with a basic block diagram to give an idea of where we intend to go and what possibilities there are to consider. Our circuits are still conceptual and have yet to be actually built and tested if parts are not available.

Detail Design

Our detailed design is overall complete and is fully discussed within the design sections in this Fall Quarter report. Not all is fully detailed yet but we are about 60% complete on figuring out the numbers and steps we will need for our design in circuitry and software.

Fabrication

Again, if all goes well this step may be bypassed since parts are readily available and our last remaining RAMAC heads are still functional to an acceptable level.

Integration

This step is planned for in our Ghent Chart for next quarter. Refer to Appendix.

Test/Verification + Operation

To test our parts and the entire project, we will be following the guidelines we set for ourselves in the Test Plan section. Our verification will be accomplished by our own team prior to the deadline for our Senior Design Project. We will also verify again during the presentations in May by letting students, reviewers, professors, and other guests operate it. The verification is the operation.

5.2 Major Deadlines

*** NOTE: This is just a brief highlight of the deadlines for our project. Please refer to the Ghent Chart in Appendix E for a more detailed description.

Fall Quarter

- Fall Design Review
- Senior Design Quarter Report(Senior Thesis)

Winter Quarter

- Write Circuit Testing
- Design Report
- Winter Design Review
- RAMAC ONLINE AND OPERATIONAL
- Begin preparations for Senior Conference
- Continue working on Senior Thesis

Spring Quarter

- Error/Efficiency Checking
- Finalizing all tests
- Design Conference
- Completion of Senior Thesis

5.3 Work Distribution

The design for the read and write function is split into two parts, the circuitry and the coding. Each individual member is going to be responsible for some aspect of the design in both divisions. However, everyone will have a different emphasis. Viet's main role will be to design the circuits for the read and write functions. Other circuits, like the switch circuit to regulate current to either the top or the bottom head, will also be constructed with the help of the other group members. Jordan will responsible for experimenting with the design and testing for efficiency and error. David will do the coding for the group using the Basic X software and work with building the circuit on the breadboard. Both Jordan and David will work together to get the digital and analog aspects to work together. The entire group will then work together to do the character code using NRZI. This will be done by using the 256-character coding in binary using the ASCII Table found online. If any assignment comes up during the course of the design, the group will work together to divide the work so that it is evenly distributed with regard to each individual's experience on the matter.

5.4 Budget Summary

The funding available to date is a total balance of $1350.00 plus support from the Santa Clara University Electrical Engineering Department. The only major spending we have planned for this entire project will be for equipment used for testing.

6.0 CONCLUSION . . .

6.1 Engineering Issues

6.2 Summary

6.1 Issues in Engineering Profession

Social

The creation of the RAMAC 350 has impacted society greatly. It has made storing information more efficient because the material used was nonvolatile and reusable. This meant that it was sustainable because it did not deplete the resources it needed to function properly. Instead of having to deal with magnetic tapes that take up huge amounts of storage space, we can just set it aside in a corner somewhere in a room. Because of its creation, we are now able to have the tiny 40GB hard drives that we can fit in our pockets. It has set the building block for the developments in massive storage devices. This is why the restoration of the RAMAC is important; it is to show how far we have gone from the days of the 1950s to the 21st century to get the technology that we have now.

Economical

The cost of building the RAMC 305 was extremely high compared to the cost of building a hard drive nowadays. They were so expensive that it was cheaper for businesses to lease rather than buy it. As a result of $137/month/MB lease of drive, there was no market other than the market for businesses for them.

Safety and Health

There were not many health or safety issues since the RAMAC 350 did not require any major hazardous material in manufacturing. For safety issues relating to hard drive heads crashing on the disk, the arm has interlocks that are controlled by pressurized heads to prevent arm movement while it is probing the disks. Only when the arm is fully retracted can it move

up and down. The spinning disks were not a safety issue for the reason that the RAMAC 350 was placed behind a protective cover. Therefore the risk of dismemberment by moving parts is not an issue.

Manufacturability

The RAMAC 350, with the thousands of components of which it is comprised, may prove to have been very difficult to manufacture during the 1950s. During the time of its existence, approximately one thousand units were made. This shows that even though it was difficult to produce, it could be built in mass quantity. Not only did the 350 contain electrical components, it also included mechanical parts. The integration of both circuitry and robotic parts is seen in the engineering and craftsmanship of the machine. The process of constructing this machine by hand would be rather difficult and testing for performance and efficiency merely adds to the time it takes to make a fully functional unit. This is apparent through the timeline of the RAMAC 350. By then, over 1,000 RAMACS had been produced.

Usability

The RAMAC 350's integration into the 305 made it popular because of its user-friendly interface. The machine's ability to read, alter, and replace any of the file records in any random sequence was invaluable since it helped with the smoother and better customer service. The person who controlled the inputs at the RAMAC only had to sit in front of typewriter and type in the needed information. Comparing the old RAMAC's usability with the one we are integrating with the PC makes ours look much simpler. The reason why ours is easier to use is because of the PCs point and click interface. After entering the Basic X program, the program asks the user

which disk and track he or she would like to write to. After the arm goes to the desired disk and track, the user will just have to input the information he or she wants to write. The user can then, after writing, have the unit go back and see if the information that was written is still present on the disk.

6.2 Summary

The success of the fall quarter presentation showed that our progress on the design is moving along quite well. Our group was able to meet important deadlines and move out of the conceptual phase for one of the designs. We were successful in coming up with the write circuit and it is only a matter of time in getting the appropriate supplies and materials to be able to test its effectiveness. However, there are a number of goals that still need to be reached. Although we had not scheduled them to be completed by the end of the fall quarter, they must be done before we can move on to other areas of the design. One of these goals is the design of the read circuit. The group has a basic understanding of how the read circuit should function but we are still in the process actually designing the circuitry. Another goal that will be pushed over to the winter quarter is the character coding. While we already know what our character code and coding method will be (256-character ASCII and NRZI, respectively), we have not yet written the code in Basic X. Since we are electrical engineers, we must first learn, essentially, the basics of Basic X. If this learning is done over the winter break, then the program for the read and write circuit should be expected to be completed by the middle of the winter quarter. Nevertheless, the group is satisfied with each other's output. We will be working tremendously hard next quarter to meet our winter quarter deadlines.

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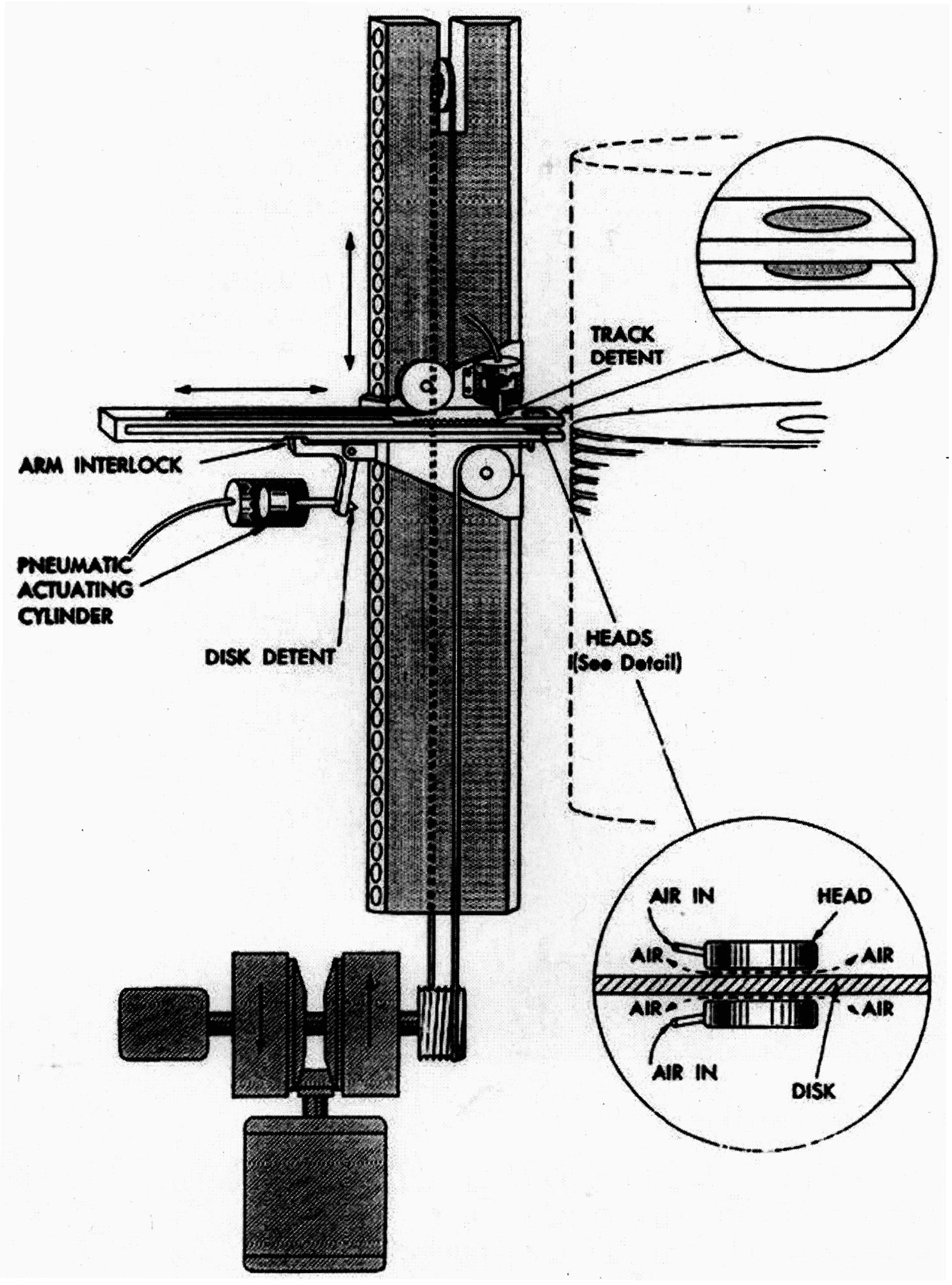
APPENDICES . . . . .

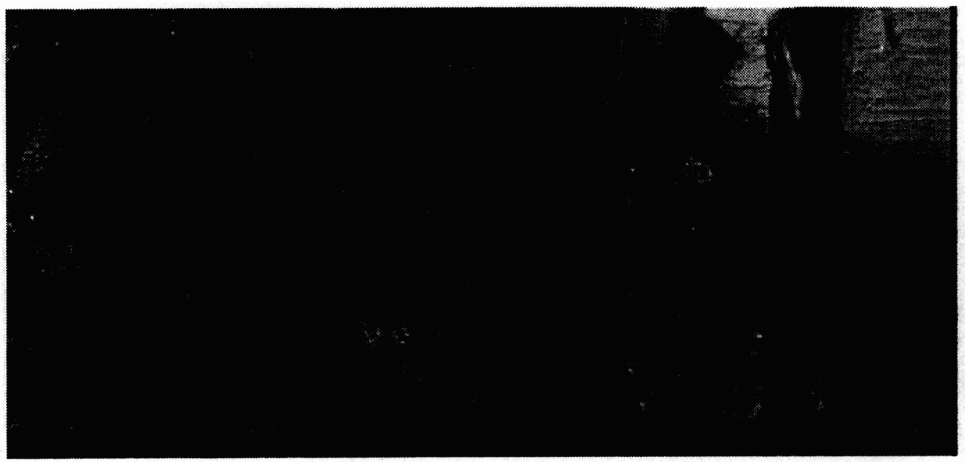
APPENDIX A: Head Diagrams
APPENDIX B: Photos of Heads
APPENDIX C: Spec. Chart
APPENDIX D: ASCII Table
APPENDIX E: Ghent Chart

APPENDIX A: Head Diagrams



APPENDIX B: Photos of Heads

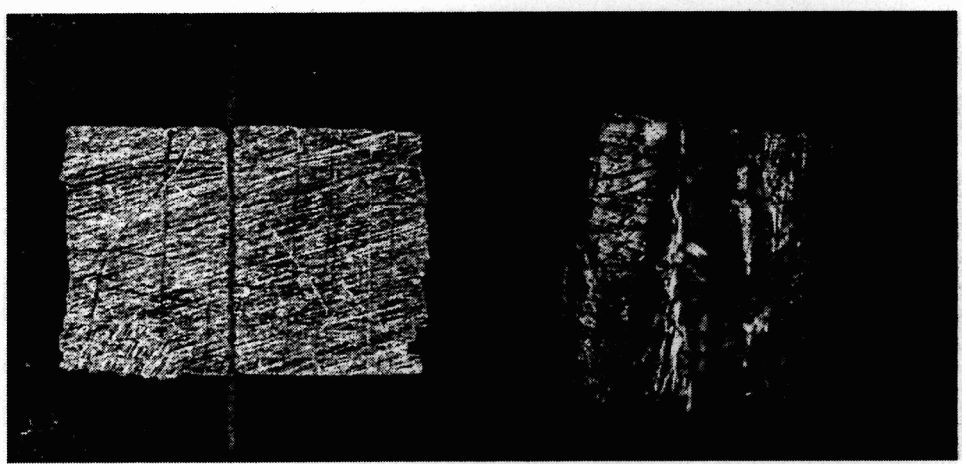
Head #1



ERASE READ/WRITE

Erase head was acceptable, but the R/W head was unfortunately corroded and crumbling.

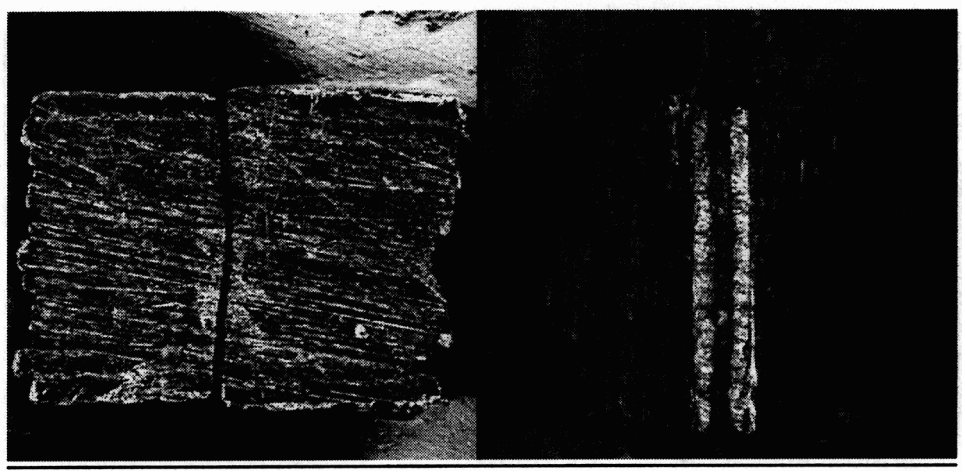
Head #2



ERASE READ/WRITE

Erase head was perfect, but the R/W head was smashed so that the gap no longer existed.

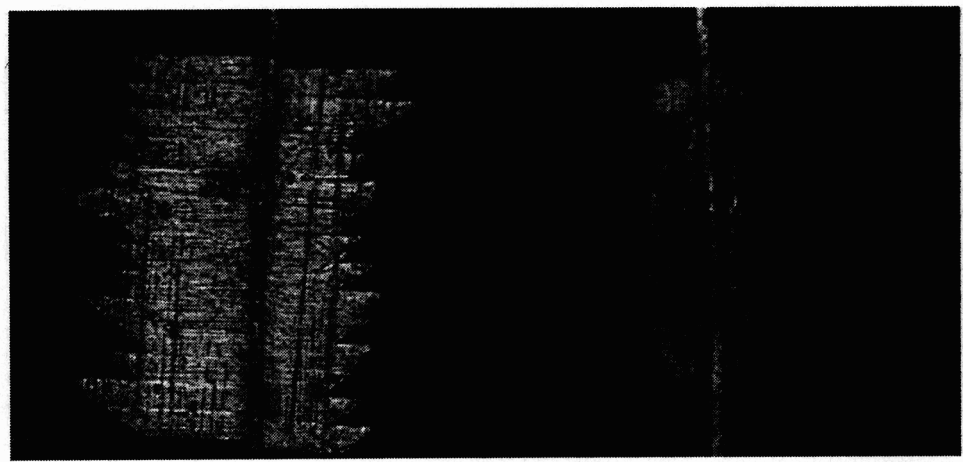
Head #C331



ERASE READ/WRITE

Erase head was in good condition and the R/W head was still near perfect. Metal was still luminous.

Head #L486



ERASE READ/WRITE

Erase head was perfect, and the R/W was in decent condition. Gaps still present.

APPENDIX C: Specification Chart

	RAMAC 350	IBM UltraStar
Disk Capacity	5 MB	300 GB
Diameter	24"	3.5"
# of Disks	50	3
# of tracks/disk	200	N/A
# of sectors/track	250	N/A
# of chars/sector	80	N/A
Total Char. Capacity	25 million	N/A
Avg. Seek Time	600 ms	4.3 ms
Rotations/minute	1200	10,025
Disk Substrate	Aluminum	N/A
Disk Particulate	Iron Oxide	N/A
Kbits/sec	170.4	1,100,800
Arm Assembly	Head Pair	Comb
Head to Disk Spacing	1 mil	3x10^-4 mil

APPENDIX D: ASCII TABLE

Dec	Hx	Oct	Char	Dec	Hx	Oct	Html	Chr	Dec	Hx	Oct	Html	Chr	Dec	Hx	Oct	Html	Chr
0	0	000	NUL (null)	32	20	040		Space	64	40	100	@	@	96	60	140	`	`
1	1	001	SOH (start of heading)	33	21	041	!	!	65	41	101	A	A	97	61	141	a	a
2	2	002	STX (start of text)	34	22	042	"	"	66	42	102	B	B	98	62	142	b	b
3	3	003	ETX (end of text)	35	23	043	#	#	67	43	103	C	C	99	63	143	c	c
4	4	004	EOT (end of transmission)	36	24	044	$	$	68	44	104	D	D	100	64	144	d	d
5	5	005	ENQ (enquiry)	37	25	045	%	%	69	45	105	E	E	101	65	145	e	e
6	6	006	ACK (acknowledge)	38	26	046	&	&	70	46	106	F	F	102	66	146	f	f
7	7	007	BEL (bell)	39	27	047	'	'	71	47	107	G	G	103	67	147	g	g
8	8	010	BS (backspace)	40	28	050	(	(	72	48	110	H	H	104	68	150	h	h
9	9	011	TAB (horizontal tab)	41	29	051	)	)	73	49	111	I	I	105	69	151	i	i
10	A	012	LF (NL line feed, new line)	42	2A	052	*	*	74	4A	112	J	J	106	6A	152	j	j
11	B	013	VT (vertical tab)	43	2B	053	+	+	75	4B	113	K	K	107	6B	153	k	k
12	C	014	FF (NP form feed, new page)	44	2C	054	,	,	76	4C	114	L	L	108	6C	154	l	l
13	D	015	CR (carriage return)	45	2D	055	-	-	77	4D	115	M	M	109	6D	155	m	m
14	E	016	SO (shift out)	46	2E	056	.	.	78	4E	116	N	N	110	6E	156	n	n
15	F	017	SI (shift in)	47	2F	057	/	/	79	4F	117	O	O	111	6F	157	o	o
16	10	020	DLE (data link escape)	48	30	060	0	0	80	50	120	P	P	112	70	160	p	p
17	11	021	DC1 (device control 1)	49	31	061	1	1	81	51	121	Q	Q	113	71	161	q	q
18	12	022	DC2 (device control 2)	50	32	062	2	2	82	52	122	R	R	114	72	162	r	r
19	13	023	DC3 (device control 3)	51	33	063	3	3	83	53	123	S	S	115	73	163	s	s
20	14	024	DC4 (device control 4)	52	34	064	4	4	84	54	124	T	T	116	74	164	t	t
21	15	025	NAK (negative acknowledge)	53	35	065	5	5	85	55	125	U	U	117	75	165	u	u
22	16	026	SYN (synchronous idle)	54	36	066	6	6	86	56	126	V	V	118	76	166	v	v
23	17	027	ETB (end of trans. block)	55	37	067	7	7	87	57	127	W	W	119	77	167	w	w
24	18	030	CAN (cancel)	56	38	070	8	8	88	58	130	X	X	120	78	170	x	x
25	19	031	EM (end of medium)	57	39	071	9	9	89	59	131	Y	Y	121	79	171	y	y
26	1A	032	SUB (substitute)	58	3A	072	:	:	90	5A	132	Z	Z	122	7A	172	z	z
27	1B	033	ESC (escape)	59	3B	073	;	;	91	5B	133	[	[	123	7B	173	{	{
28	1C	034	FS (file separator)	60	3C	074	<	<	92	5C	134	\	\	124	7C	174			|
29	1D	035	GS (group separator)	61	3D	075	=	=	93	5D	135	]	]	125	7D	175	}	}
30	1E	036	RS (record separator)	62	3E	076	>	>	94	5E	136	^	^	126	7E	176	~	~
31	1F	037	US (unit separator)	63	3F	077	?	?	95	5F	137	_	_	127	7F	177	&#127;	DEL

128	Ç	144	É	161	í	177	▒	193	┴	209	╤	225	ß	241	±
129	ü	145	æ	162	ó	178	▓	194	┬	210	╥	226	Γ	242	≥
130	é	146	Æ	163	ú	179	|	195	├	211	╙	227	π	243	≤
131	â	147	ô	164	ñ	180	┤	196	—	212	╘	228	Σ	244	⌠
132	ä	148	ö	165	Ñ	181	╡	197	┼	213	╒	229	σ	245	⌡
133	à	149	ò	166	ª	182	╢	198	╞	214	╓	230	µ	246	÷
134	å	150	û	167	º	183	╖	199	╟	215	╫	231	τ	247	≈
135	ç	151	ù	168	¿	184	╕	200	╚	216	╪	232	Φ	248	°
136	ê	152	ÿ	169	⌐	185	╣	201	╔	217	┘	233	Θ	249	∙
137	ë	153	Ö	170	¬	186	║	202	╩	218	┌	234	Ω	250	·
138	è	154	Ü	171	½	187	╗	203	╦	219	█	235	δ	251	√
139	ï	156	£	172	¼	188	╝	204	╠	220	▄	236	∞	252	ⁿ
140	î	157	¥	173	¡	189	╜	205	═	221	▌	237	φ	253	²
141	ì	158	₧	174	«	190	╛	206	╬	222	▐	238	ε	254	■
142	Ä	159	ƒ	175	»	191	┐	207	╧	223	▀	239	∩	255	
143	Å	160	á	176	░	192	└	208	╨	224	α	240	≡		

APPENDIX E: *FALL QUARTER - GHENT CHART*

	2004				2005					
Assignment	September	October	November	December	January	February	March	April	May	June
Overview of Project										
Review Electromagnetics										
Review Analog Circuits										
Write Circuit Design										
Character Coding										
Prepare Fall Presentation										
Fall Presentation										
Fall Report										
Testing Write Circuit										
Read Circuit Design										
Testing Read Circuit										
Basic X Coding										
Prepare Winter Presentation										
Winter Presentation										
Error Checking Code										
Testing Efficiency and Error										
RAMAC Online										
Prepare Final Presentation										
Design Conference										
Senior Thesis										

APPENDIX E CONTINUED: *WINTER QUARTER – REVISED GHENT CHART*

	2004				2005					
Assignment	September	October	November	December	January	February	March	April	May	June
Overview of Project										
Review Electromagnetics										
Review Analog Circuits										
Write Circuit Design										
Character Coding										
Prepare Fall Presentation										
Fall Presentation										
Fall Report										
Testing Write Circuit										
Winter Report - Report Revision										
Write/Read Test - Phase II										
Basic X Coding										
Prepare Winter Presentation										
Winter Presentation										
RAMAC Online										
Error Checking Code										
Testing Efficiency and Error										
RAMAC Online										
Prepare Final Presentation										
Design Conference										
Senior Thesis										