File Mechanics

Disk, Track and Record Arrangement

The arrangement of the disks in the file is shown in Figure 58. The file contains 52 disks, however, only 50 of these are used for data storage. The top and bottom disks are dummy disks, used to aid in the regulation of stray air currents within the file. The recording disks are numbered consecutively from top to bottom, 00 to 49. The whole disk array is rotated at a speed of 1200 RPM by a 1½ HP, 220 volt AC motor.

Data is stored on both the top and bottom of each recording disk. There is one read/write head for addressing the top side of the disk and one for the bottom. Both of these heads are mounted in one access arm (Figure 59) which may be positioned to straddle any of the 50 disks.

When the access arm is addressed to any particular disk, it may be moved inward or outward to place the read/write heads at various radial distances from the center. The arm may be detented at 102 different positions. When the arm is detented at any one of its 102 positions, a circular path on the surface of the disk moves past the read/write heads. These circular paths are called tracks. Each track includes the paths both on the top and on the bottom of the disk.

The innermost track and the outermost track on each disk are reserved for use by the Customer Engineer when servicing the file. The 100 remaining tracks, which are used for storage of accounting records, are numbered 00 to 99 from outside to inside.

With the disk rotating at 1200 RPM, each revolution requires 50 ms, which is 5 times as long as a drum revolution. Using a bit frequency in the file approximately equal to the bit frequency of the drum, two complete 100 character records can be stored in each 1/5 of the track circumference, one on the top side and one on the bottom side. Thus, a total of 10 records can be stored on each file track. Record positions 0, 1, 2, 3, and 4 are on the top side of each track; 5, 6, 7, 8, and 9 are on the bottom side.

Disk and Track Selection

In order to select a given track, the arm must be moved from its previous track location to the new track location. This involves one of three types of movement sequences:

1. To move to a numerically higher track address on the same disk, the access arm must move inward only.
2. To move the arm to a numerically lower track on the same disk, the arm must move outward only.
3. To move to an address on another disk; the arm must first be moved all the way out, then up or down to the new disk location, and inward to the selected track.

Since the third movement sequence includes the movements used in the other two, we shall use it as the example for an explanation of disk, track, and record selection.

Access Mechanism

In order to accomplish the necessary movement of the arm, an access mechanism is provided. This consists basically of the following components (Figure 60).

1. A carriage on which the arm is mounted for horizontal movement.
2. A way on which the carriage is mounted for vertical movement.
3. Two access cables, a capstan, two clutches, and a motor to provide movement to the arm and carriage.
4. A disk detent to keep the carriage fixed in place while the arm moves into the disk array.
5. A track detent to fix the arm's position at the correct track.

Carriage and Disk Detent

In order to allow the arm to move vertically, it is held in a carriage that is free to move vertically on a specially constructed way (Figure 60). The arm itself is free to move horizontally within special guides on the carriage. However, the carriage cannot move vertically at the same time that the arm is moving horizontally without damaging the disks. Therefore,

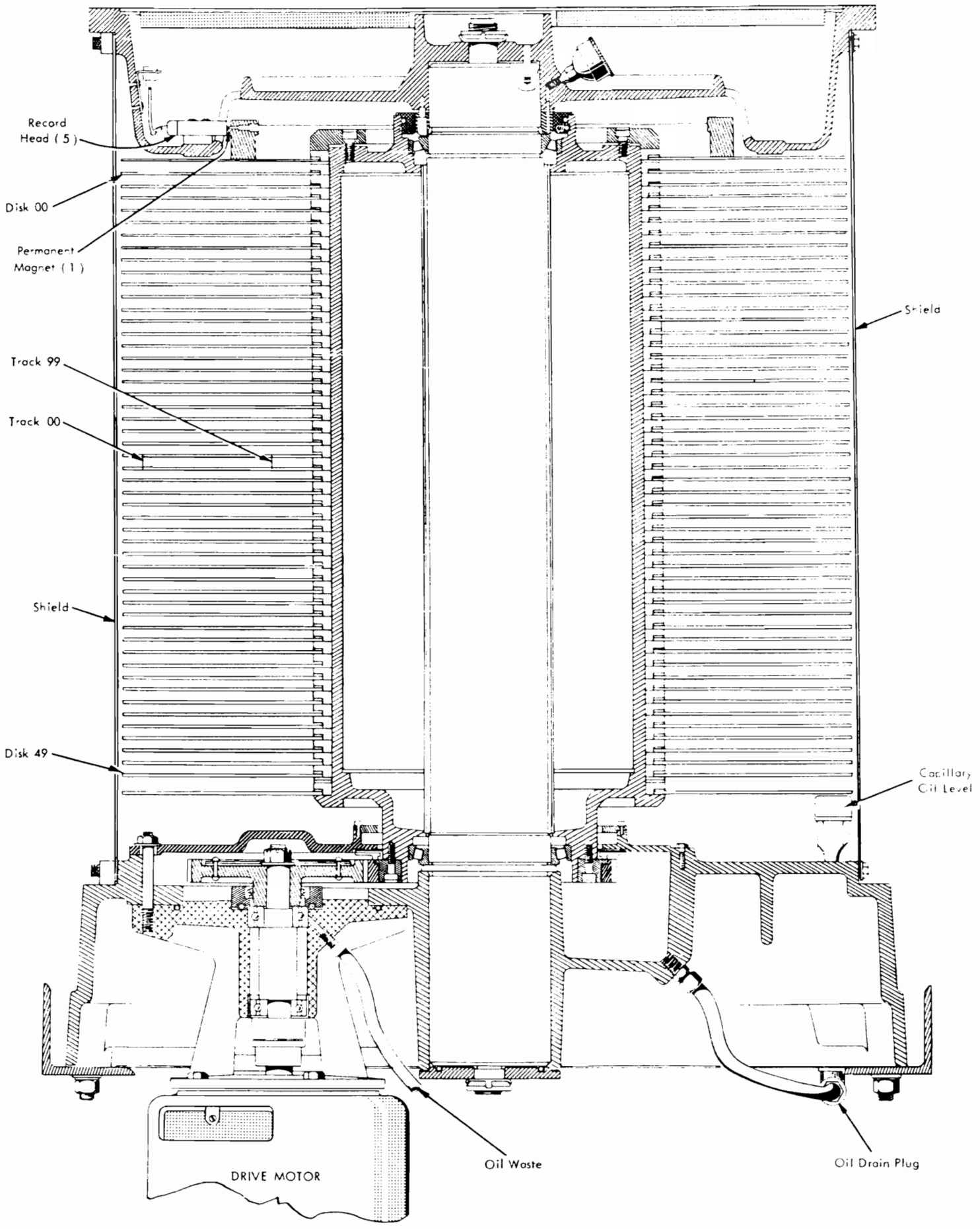


Figure 58. Disk Assembly

a detent is provided to lock the carriage to the way while the arm is extended or retracted. Another detent is provided to lock the arm all the way out, in the home position, while the carriage moves vertically. This disk detent (which locks the carriage to the way) and the fail safe bar (which locks the arm in the home position) are mechanically linked so that one or the other must be engaged at all times. This linkage (Figure 61) is called the fail safe interlock.

When the arm is retracted to the home position, out air pressure is applied to the disk detent piston to unlock the carriage so that it can move. When the correct disk has been located, in air pressure is applied to the disk detent piston to lock the carriage to the way and unlock the arm.

Capstan and Cables

The capstan and cables provide a method of applying power to move the arm and the carriage. The two cables are wrapped around the capstan in opposite directions (Figure 62). One of these cables goes up the far side of the way, over the tension adjusting

pulley, down and through a pulley on the carriage, and is fastened to the front end of the arm. The other cable goes up the near side of the way, through a pulley on the carriage, and is fastened to the rear end of the arm.

If the disk detent has locked the carriage to the way, rotating the capstan clockwise will cause the arm to move in; rotating it counterclockwise will cause the arm to move out.

If the arm is locked in the home position by retracting the disk detent, clockwise capstan movement will cause the carriage to move down; counterclockwise capstan movement will cause the carriage to move up.

Servo Clutches

The capstan may be caused to rotate in either direction by energizing one of two clutches attached to the capstan shaft. Figure 63 shows an exploded view of one of these clutches. The rotor is fastened to the capstan shaft, and the clutch housing is free to move about the shaft. The two clutch housings making up the pair of servo clutches are each driven in the opposite direction by a pinion assembly on the shaft of a 1/3 HP access drive motor. This pinion is shown in Figure 64, along with its clutches. One of these clutches is shown in cross section.

The space between the rotor and the housing is filled with powdered iron and graphite. The application of a direct current to the magnet coil will cause the powdered iron particles to align themselves and form a magnetic bond between the continuously running housing and the rotor.

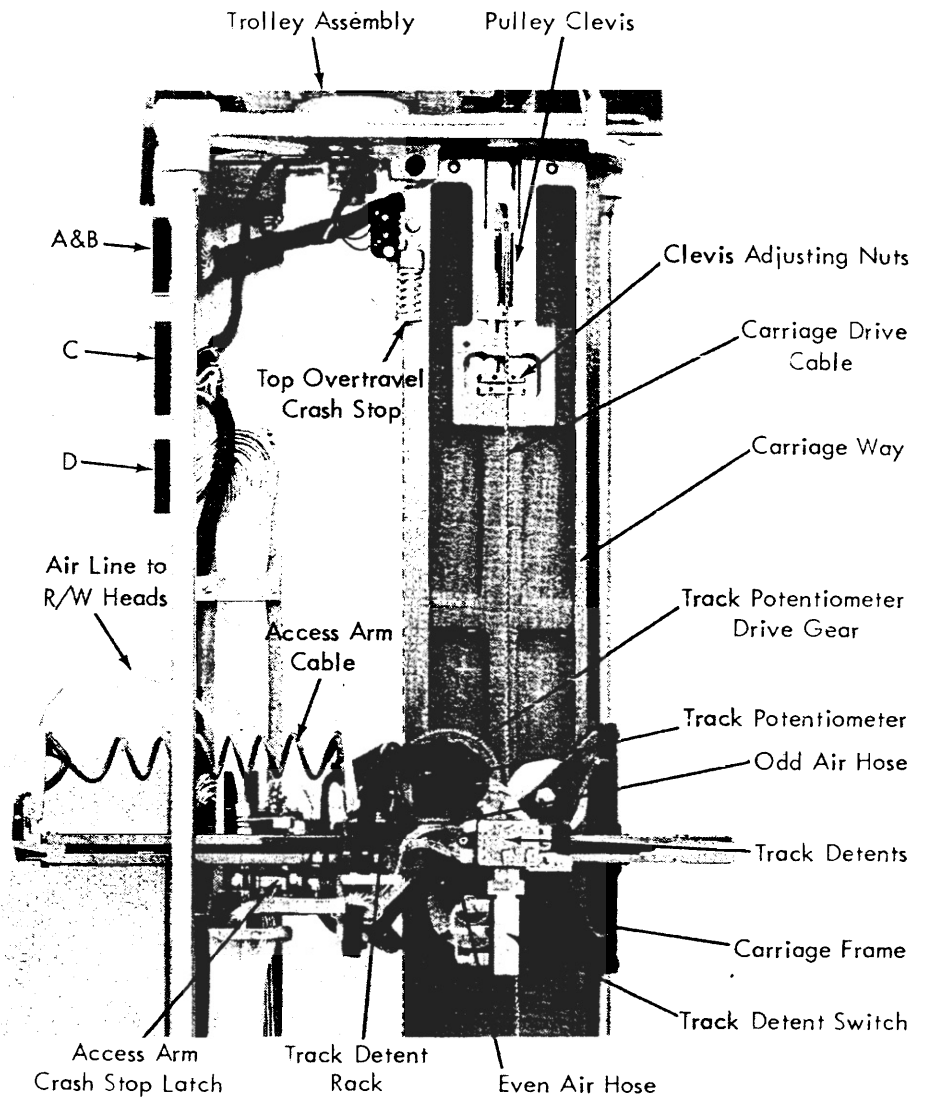


Figure 60. Carriage and Arm Assembly

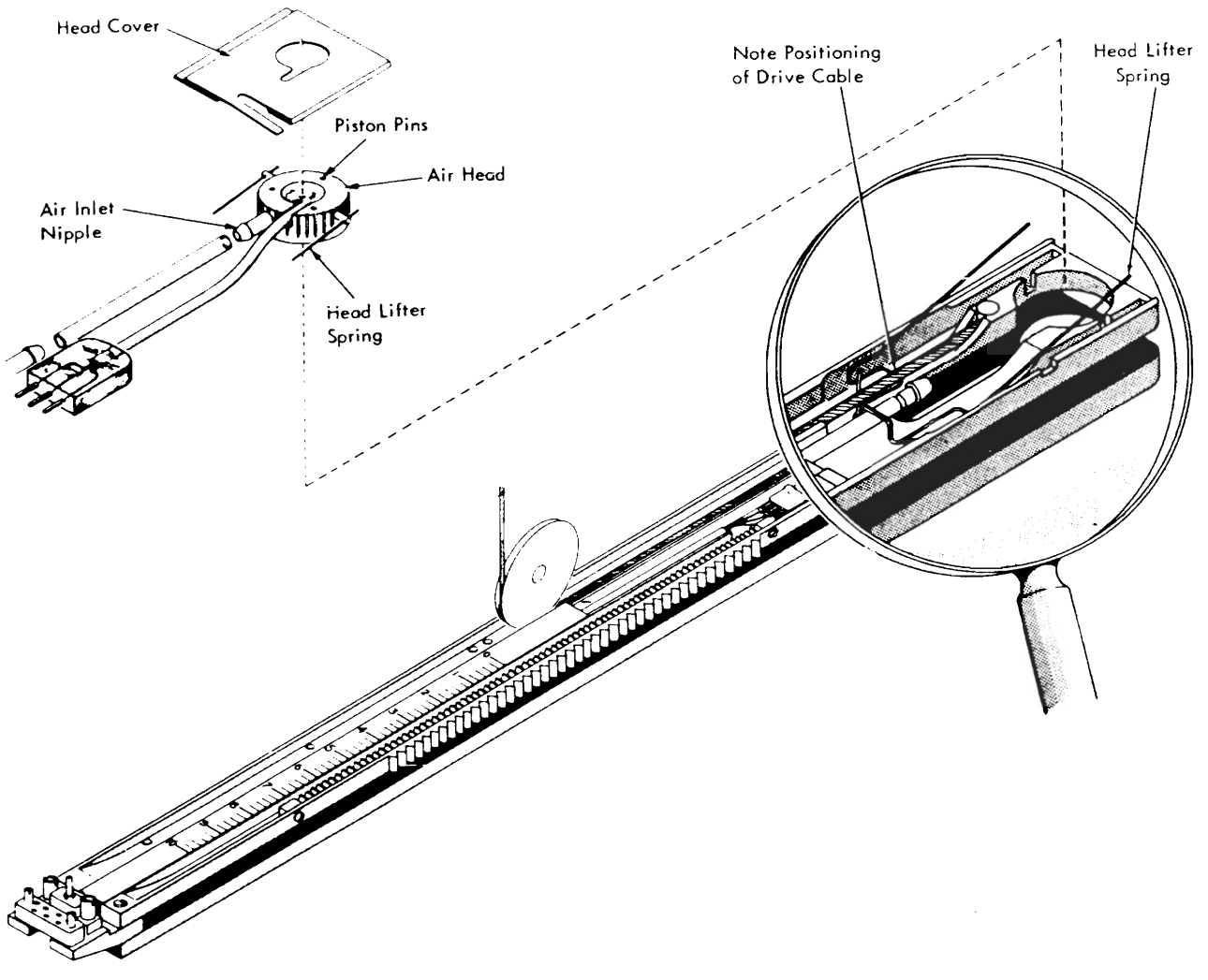


Figure 59. Access Arm

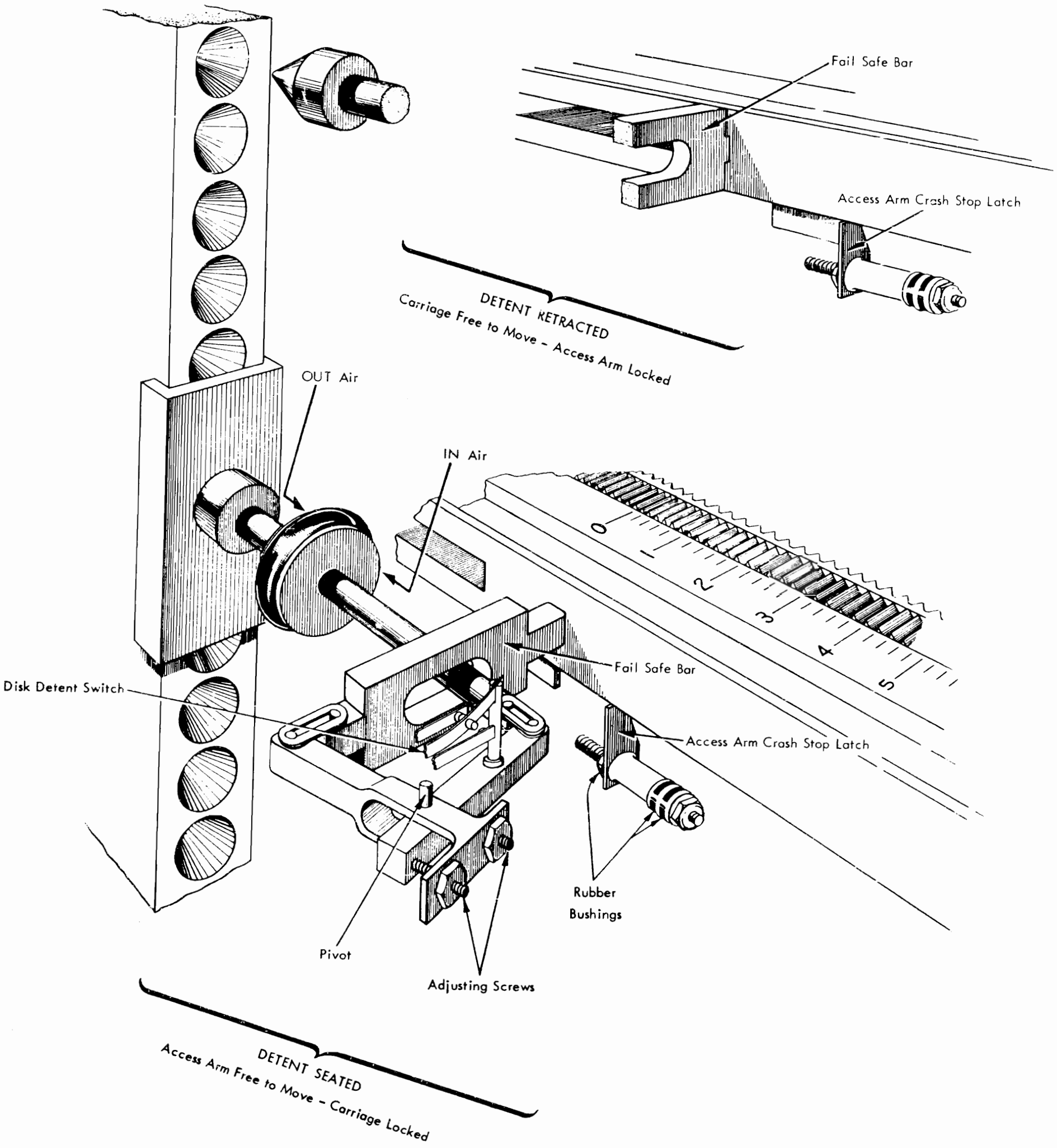


Figure 61. Disk Detent Operation

The servo control circuits are designed so that only one clutch is energized at a time. If one of these clutches is energized to produce the desired movement of the arm or carriage, the other will be energized as the addressed position is reached to cause dynamic braking.

Track Detent

Once the arm has been moved into the correct track, a track detent is driven by air pressure into a land in the rack on the side of the arm (Figure 65). In order to allow the rack to have teeth large enough to effectively hold the arm in place, two detents are

provided, one for even track addresses, and the other for odd addresses. Thus, one arm rack tooth is used to hold the arm for two tracks, depending on which detent is used. Both detents are air operated and spring returned.

Record Selection

When the access arm is detented so that its read/write heads are scanning a particular track, further selection is necessary to obtain one specific record.

The selection between the records on the top side of the disk and those on the bottom is accomplished by the side relay. When normal, this relay connects the read/write circuits to the top head, when transferred, to the bottom head.

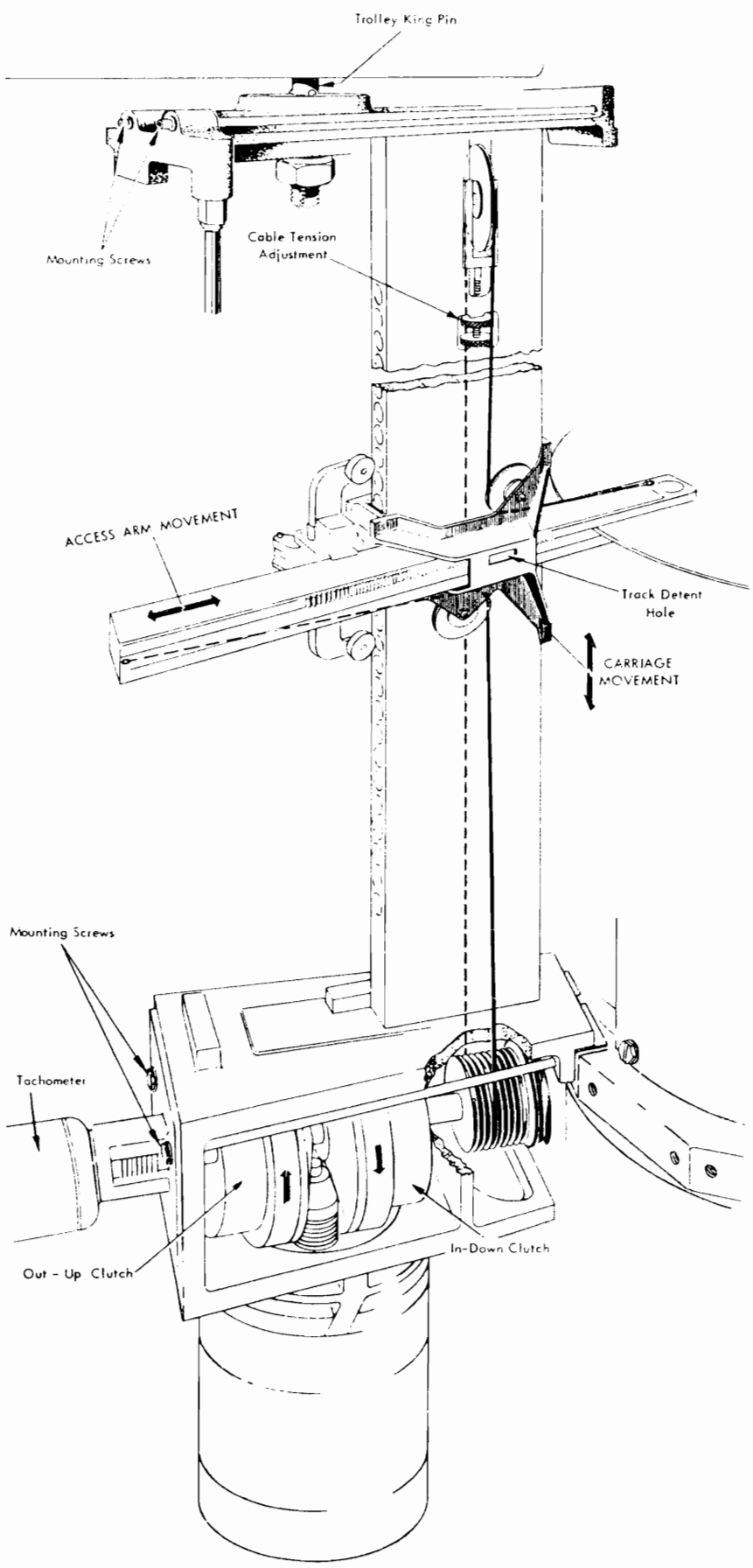


Figure 62. Access Mechanism

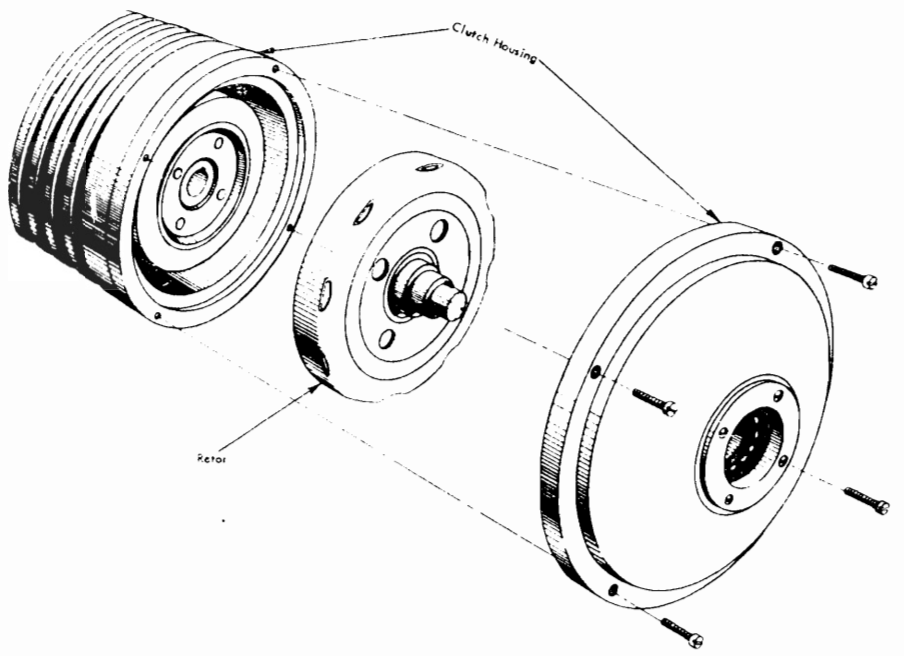


Figure 63. Exploded View of Magnetic Clutch

The selection of one of the five records on the selected side of the selected track is accomplished with the aid of the record heads. These heads are mounted on the top casting at intervals of 72°. A permanent magnet mounted on the top dummy disk moves past one record head every 10 ms. The relays which establish the record address connect the proper head into the record selection circuit to provide a record start pulse at the correct time. The same relays connect a second read head into the circuit to supply a record stop pulse 10 ms after record start. The record stop pulse serves as a safety feature.

Read/Write Heads

The actual reading and writing of a file record is done by the read/write heads. Figure 66 shows the physical arrangement of the coils used for reading or writing on the disk. The read/write coils have a core consisting of 8 laminations, while the erase coil core has 14 laminations. The erasing of a broader path than is used for writing and reading helps minimize extraneous "noise." The read/write head is cast in plastic and mounted in a larger mechanism called the air head (Figure 66).

Figure 59 shows the air heads as they are mounted in the access arm. The purpose of the air heads is to position the read/write head in relation to the disk. When the access arm is advanced from a position clear of a disk to a position straddling a disk, the read/write heads must be in a retracted position to avoid striking the edge of the disk. When the arm is detented at a track address, the read/write heads must be positioned close to the disk for reading and writing.

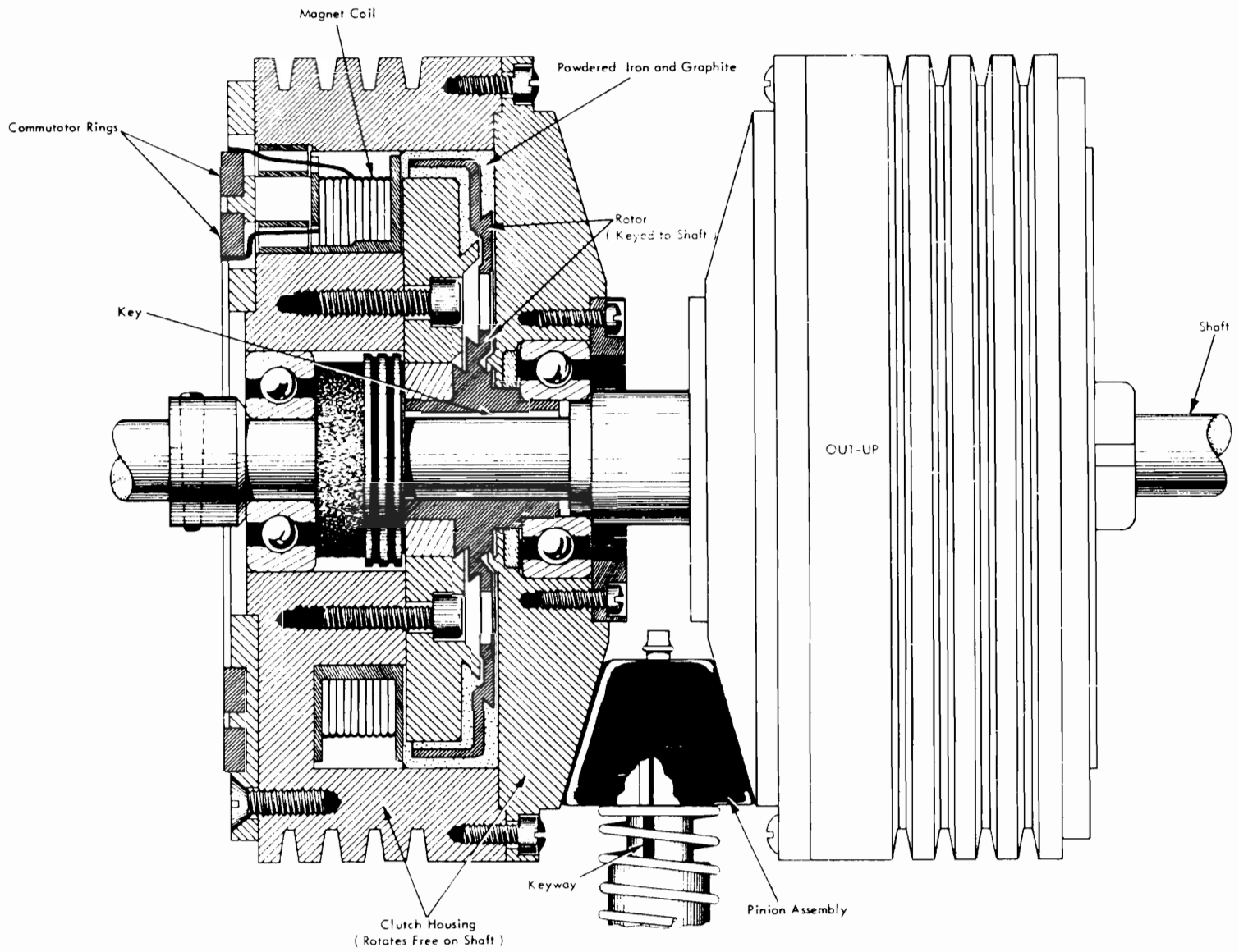


Figure 64. Magnetic Clutch Assembly

The positioning of the air head (and the read/write head which it contains) is controlled by the application or removal of air pressure. If no air pressure is applied to the head, the springs act against the gimbal pins to hold the head against the head cover. When air pressure is applied to the air head, the three pistons are forced to protrude from the head against the head cover. The stationary head cover limits the movement of the pistons, forcing the head away from the cover and toward the disk. To keep the head from scraping the disk, air is expelled against the disk from six small orifices in the head. The applied air pressure thus causes two distinct forces to impel the head in opposite directions. The point at which these forces balance allows the head to ride about .0003" from the surface of the disk. When air is applied, the heads are said to be down, even though the bottom head is moved upward to reach its active position.

Servo Control Mechanism Logic

The preceding material has explained the mechanisms required to move the read/write heads from one address to another. Since the various actions involved in a servo operation are controlled electronically, some means of translating the positions of the access arm and carriage into electrical signals and controlling their movement is required.

Track Potentiometer Logic

The track potentiometer provides a means of indicating electrically the distance and direction that the access arm must be moved to reach the addressed track. This potentiometer is mounted on the carriage as is shown in Figure 60. The wiper is geared to the access arm. As the access arm is moved from it's home position, the wiper moves from one end of the potentiometer resistor strip toward the other.

The upper part of Figure 67 shows the logic of the track potentiometer operation. A 150 volt floating power supply is connected across the extremes of the potentiometer. The position on the potentiometer resistor strip corresponding to the newly addressed track is grounded. However, since the track potentiometer is not physically large enough to permit a separate tap for each track position, taps are provided for track positions 00, 20, 40, 60, 80, and 100 only. Intermediate track positions are addressed by grounding a point on a voltage divider network connected between two adjacent taps. The selection of the grounding point is accomplished by the track ad-

dress relay tree (8.02.02). Ground potential is provided through the disk null relay N/O points which are transferred when the carriage is detented at the correct disk.

If the wiper receives a positive signal, as is the case in Figure 67, this voltage is taken through the home relay N/C points (the home relay is down when the carriage is detented) to the differentiating clutch amplifier. A positive voltage causes the in and down clutch to be energized. This moves the arm in.

A negative wiper signal follows the same path to the clutch amplifier, but energizes the out and up clutch.

A zero wiper signal causes neither clutch to be energized. However, it does cause an output from the track null detector, which is used to apply air to the correct track detent.

Disk Potentiometer Logic

The disk potentiometer provides a means of indicting electrically the direction and distance that the carriage must be moved to reach the addressed track. It operates on the same principle as the track potentiometer; however, the disk potentiometer resistor strip is actually mounted on the side of the way. The spacing of the disks is sufficient to allow a separate tap on the disk potentiometer strip for each disk position. The disk potentiometer wiper is mounted on the carriage.

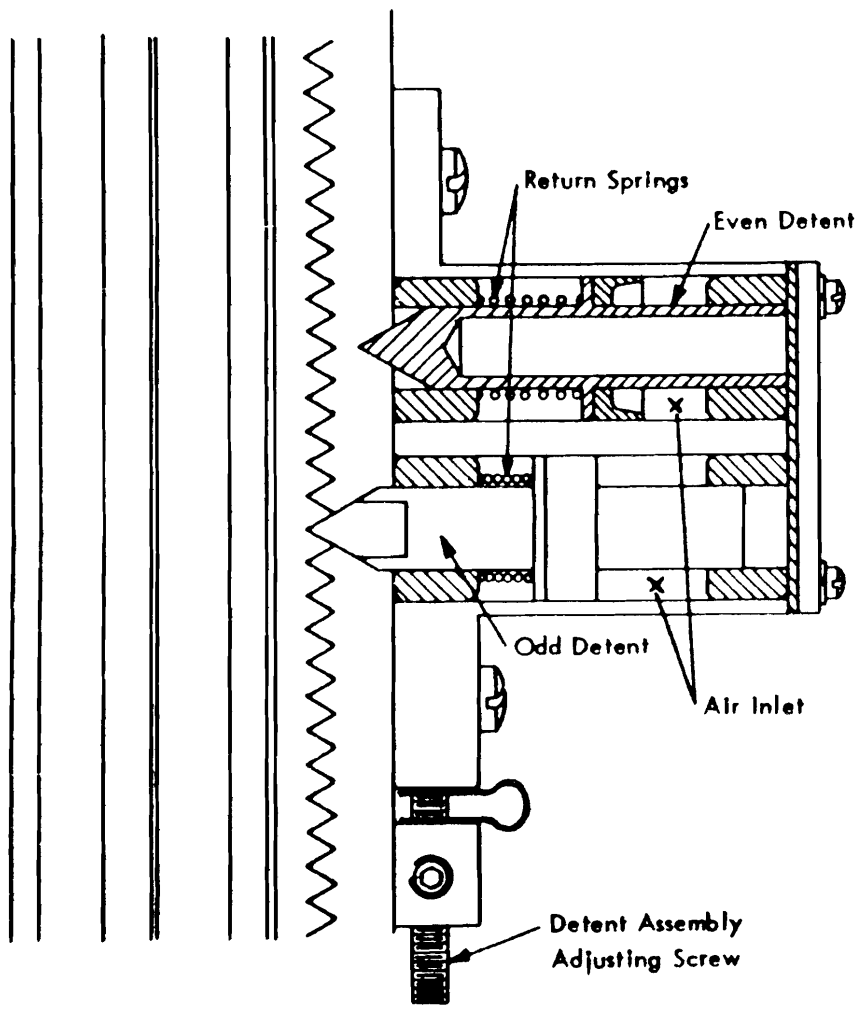


Figure 65. Track Detent

The output at the disk potentiometer wiper is fed to the disk null detector and a N/O point of the home relay. If the home relay is up (disk detent not engaged), this signal is fed to the clutch amplifier to control the movement of the carriage.

The output of the disk null detector controls the disk detent air and the disk null relay (top of Figure 67).

Disk Detent Switch

When the disk detent is disengaged, the disk detent switch is transferred to pick the home relay (8.04.03). Since disengaging the disk detent also frees the carriage to move, the control of the clutches is given to the disk potentiometer when the home relay is picked, as was seen in the discussion of the disk potentiometer.

Tachometer Logic

The tachometer provides a means for controlling the speed of movement and deceleration of the arm or carriage during a servo operation. It is essentially a DC generator, which is mounted on the clutch shaft.

As the clutch shaft gathers speed, the tachometer supplies a potential that builds up to a maximum of approximately 25 volts. The tachometer signal has the same polarity as the potentiomenter signal which has energized the active clutch, but the two signals oppose each other in the differential clutch amplifier. As the carriage or arm approaches the addressed position, the wiper signal becomes less than the tachometer signal. This causes the opposing clutch to be energized to provide dynamic breaking. With proper adjustment, the carriage or arm will decelerate to a smooth stop without oscillation or overshoot.

Air Valve Solenoids

The air valve solenoids are provided to control the air used to position the read/write heads and to operate the two track detents and the disk detent. These are located at the lower part of the access mechanism, on the side away from the disks. From top to bottom, these solenoids control the following: odd track detent, even track detent, head, disk detent in, disk detent out.

Air Compressor

Compressed air is supplied to the air valve solenoids from a piston type compressor currently located in its own cabinet. Previous models were located under the file. A schematic of the remote air compressor is shown in Figure 68. One or two compressors may be used depending on the requirements of the system. Air is delivered from the tank to the file through flexible hose. A solenoid operated vent valve will

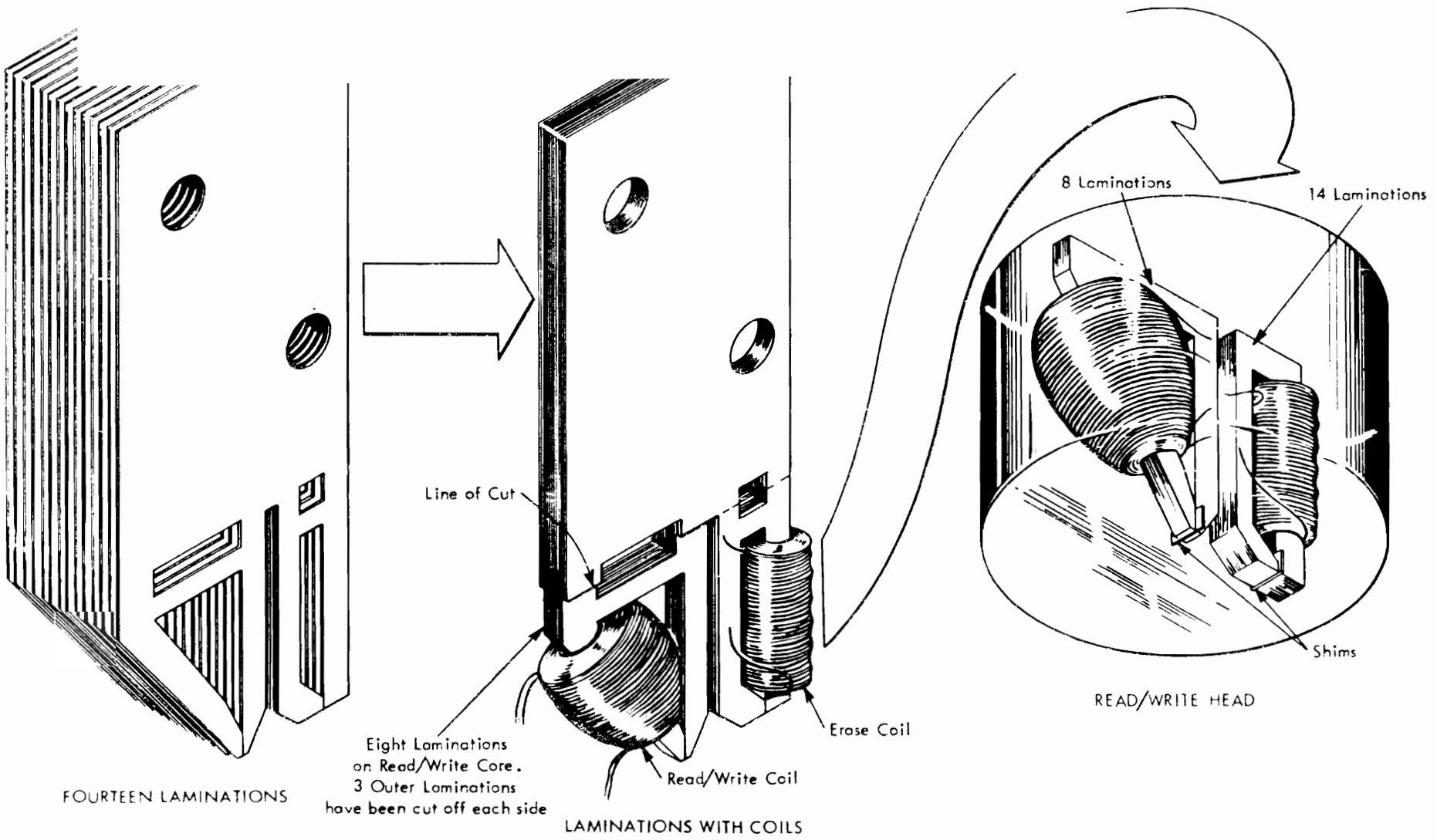


Figure 66. Read/Write Head and Air Head

open the file air lines to atmosphere if the file is taken off line. Water from the tank and lines accumulates in the automatic drain valve. From there it passes to trays to evaporate. A pressure switch will de-energize a dump valve solenoid if the line pressure exceeds 80 PSI. This will direct the compressor output to the atmosphere until the pressure in the tank is reduced to 60 PSI by file operation or bleeding.

Each of the two compressors has a three position control switch in the sequence control box. With the switch set to OFF, the unit under control of that switch is inoperative.

When set to LOCAL, the compressor can be controlled with the start and stop buttons on the control box. On 8.40.04, the compressor motor is excited through the motor control switch and the three points of switch C1 to the line. C1 coil is energized from L2, through the thermal points; then, through the remote-local switch terminal 33 (8.40.03) to the start switch on 8.40.04. When the control switch is set to REMOTE the motor control is through time delay point 7 (8.40.03). This point closes after the timer motor has been started by a signal from the 305.

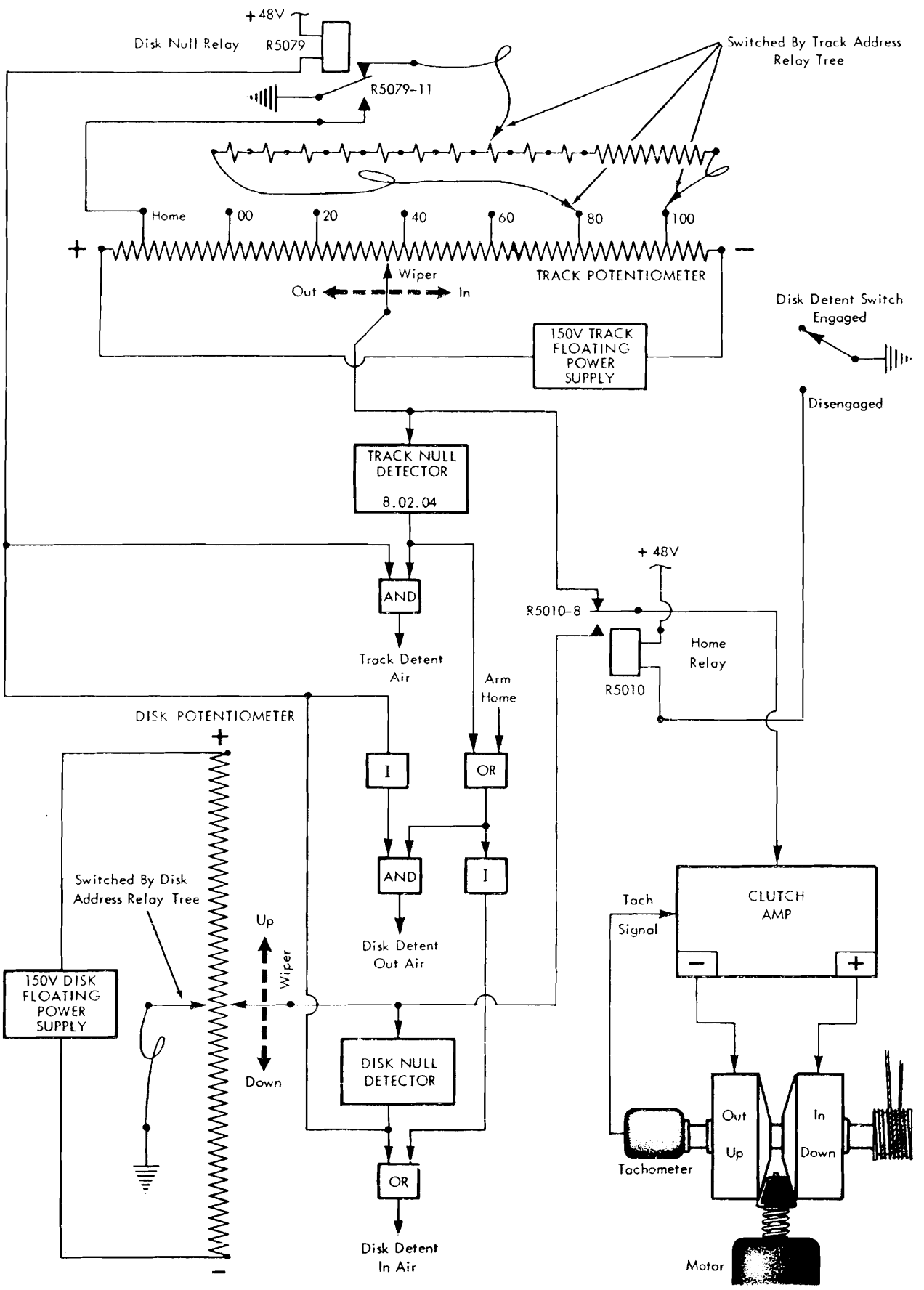


Figure 67. Logic of Access Servo System

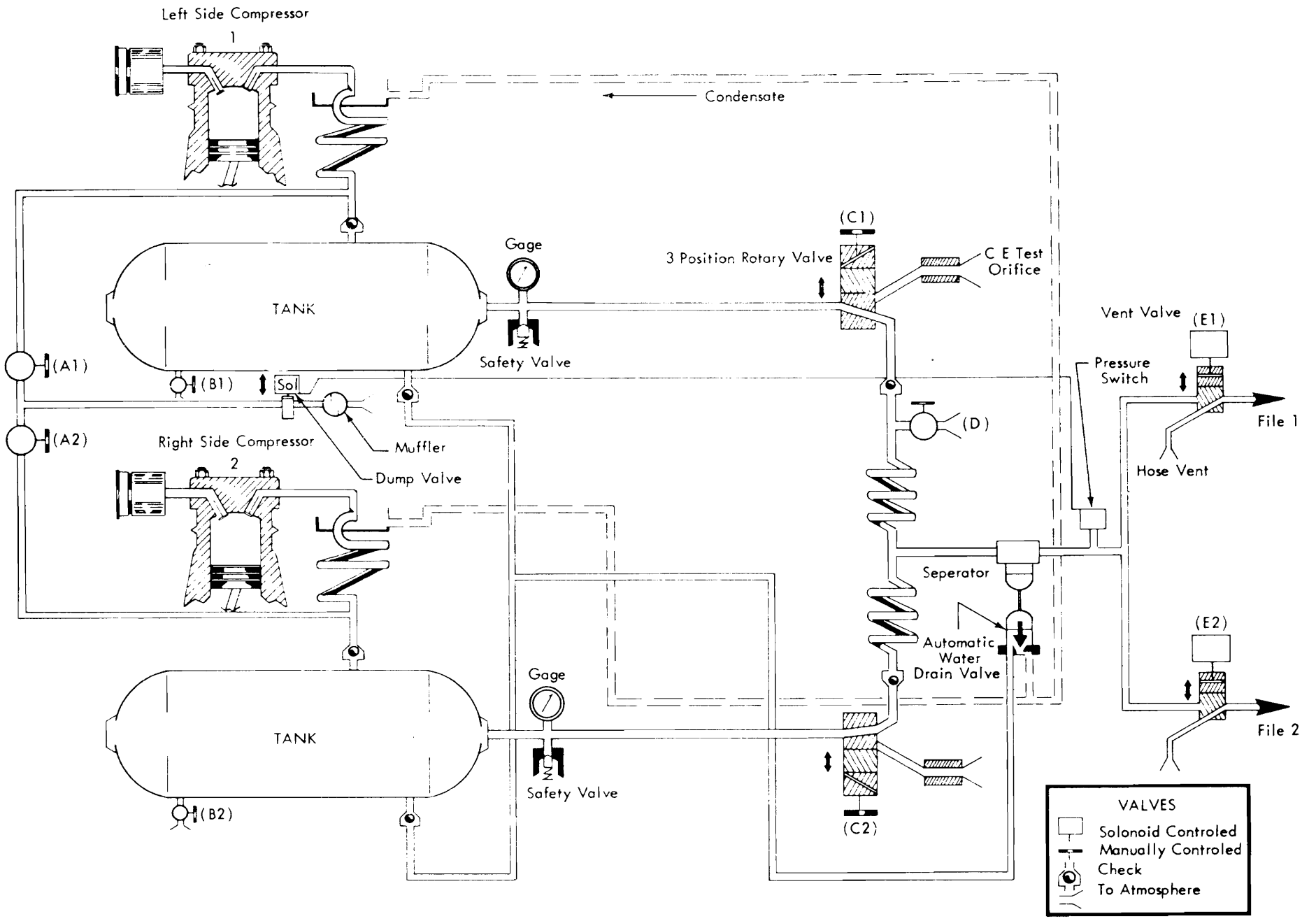


Figure 68. Remote Compressor

Basic File Servo Circuits

In order to follow the circuits involved in a complete $T_2 = J$ operation, it will first be necessary to consider the following basic servo circuits: safety circuits, null detectors, differential clutch amplifier.

Servo Safety Circuits

Great care has been taken in the design of the 350 circuits to protect the records that are stored in the file. A number of safety circuits must be properly conditioned before the file can be operated as a component of the RAMAC. Two safety relays are involved in these safety circuits, and both must be energized. These are the logic safety relay, and the bias safety relay.

Logic Safety Relay

The logic safety relay, R5116 (8.06.01), can be picked only by meeting the requirements of the interlock chain in series with the coil. Even if all of the interlocking conditions are fulfilled, R5116-2 N/O must be shunted in order to pick the relay initially. This shunt may be provided by either the safety reset switch (8.06.01), or by R160-1 (1.02.02). R160 is energized by the reset switch at the supervisory console (1.02.03).

If either reset switch is depressed, R5116 (8.06.01) will be energized, provided the following conditions exist:

1. The carriage is not at its extreme upper or lower limit of travel on the way. This permits the disk drive overtravel safety switches to be closed (8.06.01).

2. A number of critical relays must be in the machine. A normally open and a normally closed point of each of these relays are paralleled, so that any one may be either energized or not energized and still complete its portion of the interlock (8.06.01).

3. The pressure supplied by the air compressor must be greater than 45 PSI in order to close the air pressure switch (8.00.06).

Even though the logic safety relay is picked with the above conditions satisfied, the bias safety relay, R5007, must be picked to establish a hold circuit through the R5007-3 N/O points.

Bias Safety Relay

Figure 69 has the circuit for the pick of the bias safety relay, R5007 (8.06.02).

This relay is to be energized only if all of the following conditions and voltages are present:

1. Logic safety relay is energized.
2. +48v, +140v, −250v and −60v are present.
3. Regulated voltages −210v, +215v, +140v are present.
4. Pluggable unit B8b is present.
5. Track and disk ground fuses are intact.
6. Track and disk power fuses are intact.
7. Track and disk floating power supplies voltages are present.

Normally the left hand grid of the DE304 is at approximately ground potential causing the left hand section to conduct, picking R5007. If the disk or track ground fuses, the regulated 140v or regulated 215v power goes out, the left hand grid will be pulled down cutting this side of the tube off. If the −250v or regulated −210v were not present, the right hand grid would go plus, raising the common cathode potential and cutting off the left hand side again. The relay points of R5055 and R5056 in the plate circuit will be closed only if the two floating power supplies are operating correctly. The logic safety relay, R5116, must be up due to the fact that either the reset key or the safety reset key are depressed. R5116 has no hold until R5007 has been picked; therefore, the key must be held until 5007 picks.

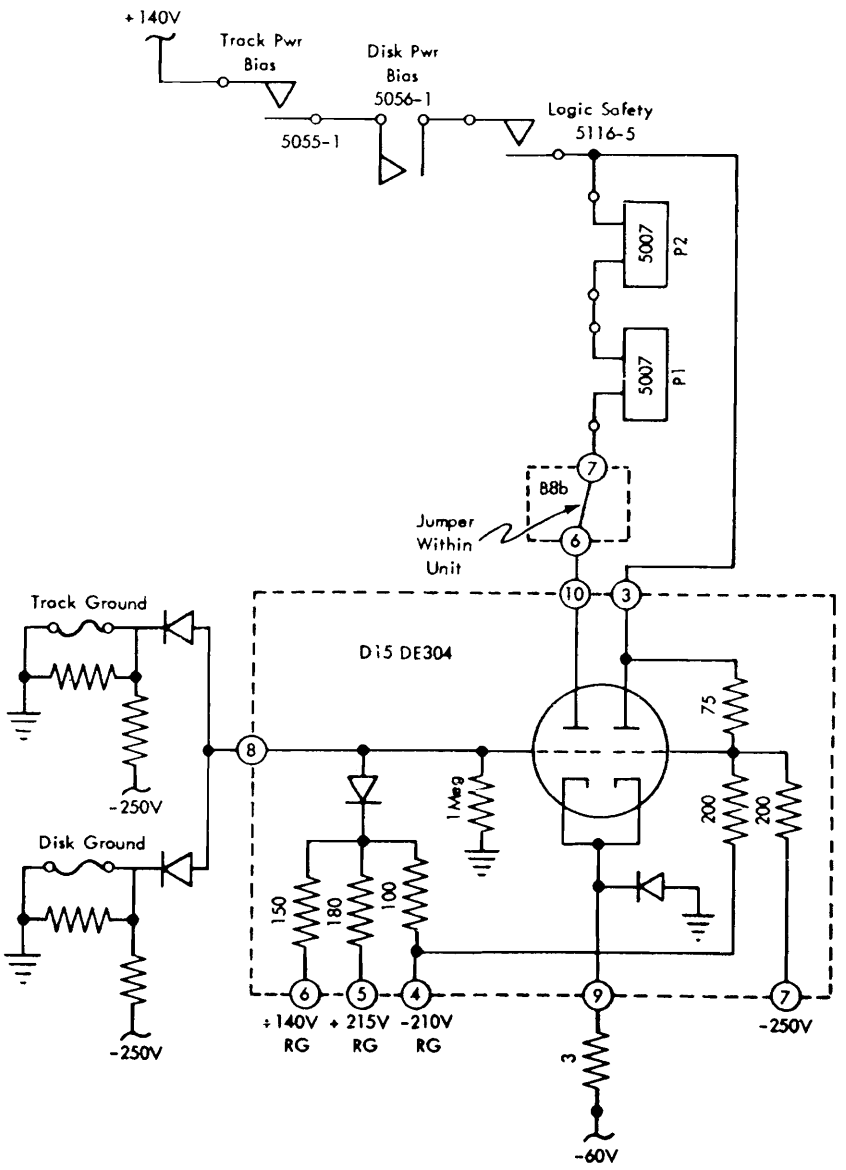


Figure 69. Bias Safety

Null Detectors

The disk and track null detectors are almost identical. We shall consider the disk null detector first, then the differences between the disk null detector and the track null detector.

Disk Null Detector

Figure 70 is a redrawing of the disk null detector (8.01.04) to include all the components within the pluggable units.

Servo logic requires that the disk null relay, R5079, be energized only when the carriage is located at the disk to which it is addressed. This relay is picked through the normally open points of MR3. MR3 is picked only when the disk wiper signal is within ½ volt of ground level.

The input to pin 4 of C10a must be high to allow this unit to draw current to energize MR3. This requires that both halves of A10 be cut off; that is, both grids must be about 10 volts negative with respect to their cathodes. As the left cathode and the right grid are both connected to ground, B11a must supply −10 volts from pin 6 and +10 volts from pin 3 to achieve a null. The circuit components are such that the required levels will be available if the input to D10 is within ½ volt of ground level.

If the input to D10 rises, the increased conduction through the left triode causes a lower level at the cathode of C11a. C11a draws more current to lower the grid of B11a. The input to the right cathode of A10 becomes negative, allowing current to flow through that triode, which lowers its plate output. C10a is thus blocked and MR3 is dropped.

A negative input to D10-5 causes the left triode to conduct less, raising the cathode of C11a. C11a draws less current to raise the grid of B11a, causing greater conduction. Pin 6 of B11a is thus raised, causing the left triode to A10 to conduct. This lowers the plate output of A10. As a result, C10a is blocked and MR3 is dropped.

The potentiometer in the cathode circuit of D10 controls the bias at the right grid. Since the voltage level of the common cathodes of D10 is determined by the total conduction of both triodes, the grid bias at the left triode is also controlled in part by the potentiometer adjustment. The sensitivity and balance of the disk null detector are therefore functions of this potentiometer adjustment.

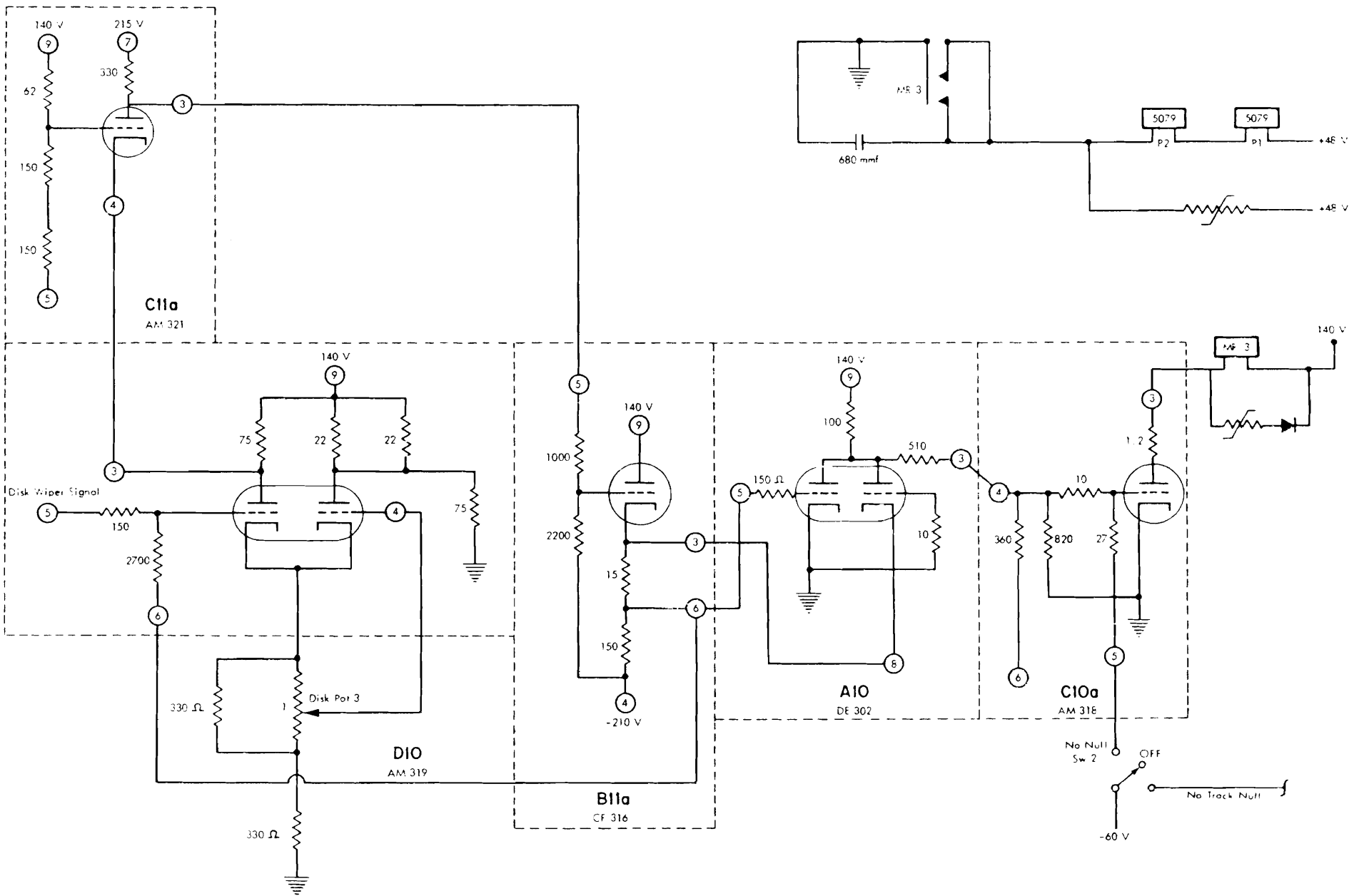


Figure 70. Disk Null Detector (8.01.04)

Track Null Detector

Servo logic requires that the track null relay (R5082 on 8.02.04) be energized only when the access arm is positioned at the track to which it is addressed, or when it is at home position if there is no disk null. R5082 is energized by the N/O points of MR2. With disk null relay (R5079) energized, MR2 is picked in a manner identical to the pick of MR3 by the disk null detector. This may be seen by comparing Figure 70 with Figure 78 (8.01.04 with 8.02.04). The operation of the track null detector when the arm is at the home position will be considered later.

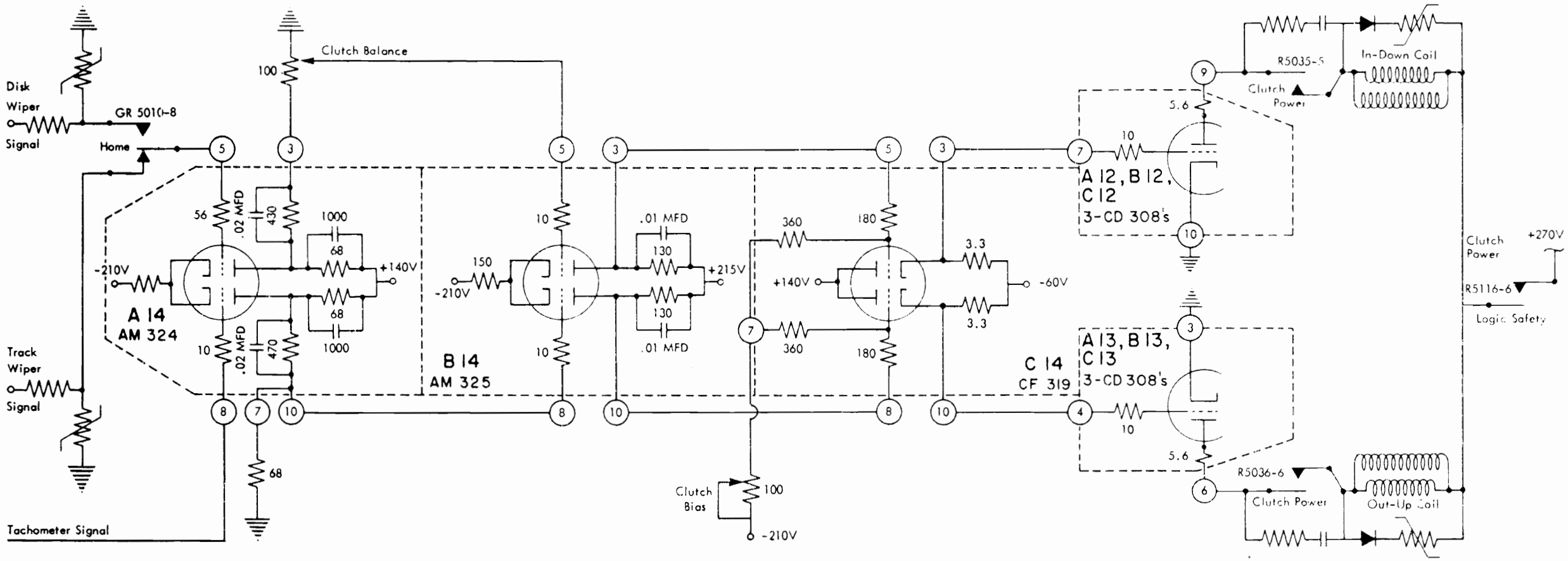
Clutch Power Amplifier

Figure 71 shows the differential clutch amplifier (8.05.01) with the components of all the pluggable units drawn in. The input to pin 5 of A14 is taken from either the track or disk potentiometer wiper, depending on the status of the home relay (GR5010). The input to pin 8 is the tachometer signal.

If a positive signal is applied to pin 5 of A14, the in and down clutch will be energized, assuming that R5116 and R5035 are energized. The positive signal to A14-5 increases conduction through the upper triode. This raises the cathode level, causing less current to flow through the lower triode. Thus, the level of A14-3 becomes more negative while A14-10 becomes more positive. These two levels applied to B14 cause less current to flow through B13's upper triode, and more current through the lower triode. Thus, B14-3 becomes more positive while B14-10 becomes less positive. The inputs to pin 5 and 8 of C14 cause the output from pin 3 to rise and that from pin 10 to fall. The halves of the CD 308's which drive the out and up clutch are cut off, while greatly increased current is drawn through the in and down clutch.

Similar analysis will show that a negative wiper signal causes the out and up clutch to be energized.

As the clutch shaft gains speed, a signal is supplied from the tachometer to pin 8 of A14. This signal has the same polarity as the wiper signal applied to pin 5, but its maximum value is about 25 volts. As the wiper signal becomes less than the tachometer signal, the differential amplifier becomes unbalanced in the other direction. This causes the opposite clutch to be energized to provide dynamic braking.



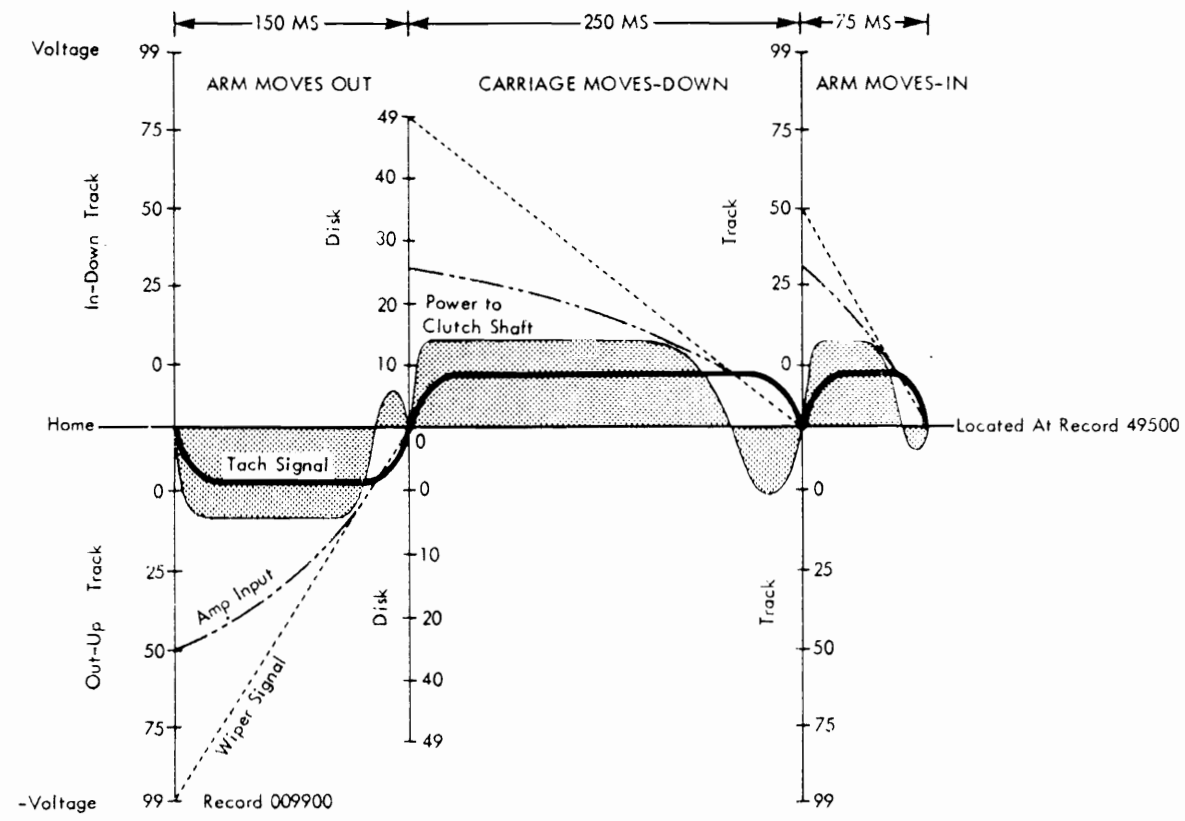


Figure 71. Clutch Power Amplifier (8.05.01, 8.05.02) with Theoretical Voltages and Waveforms

File Servo Circuit Operation

In order to facilitate the explanation of file circuits, we shall assume that a servo from address 01451 to address 49955 is being executed from the instruction W04J9905bb. Figure 72 is the data flow diagram.

OBJECTIVES:

1. Cause IRWDP cycle sequence.
2. Place new address in file address register relays.
3. Start mechanical servo operation.
   a. Retract air heads.
   b. Move arm out (track detent was released during R cycle).
   c. Retract disk detent, causing fail safe mechanism to lock arm all the way out.
   d. Move carriage down to new disk.
   e. Engage disk detent, causing fail safe mechanism to free arm.
   f. Move arm into new track.
   g. Engage track detent.
   h. Extend air heads.
4. Notify process unit servo is complete with track located gate.
5. Select addressed record for reading or writing.

IRWDP Sequence: The $T_2 = J$ line causes D cycle to follow W cycle. It also blocks I cycle ready trigger until P cycle end. On 2.01.06, $T_2 = J$ forces a program advance and a new program if P = blank. New program must be up to allow P cycle end to initiate an I cycle (1B2a – 1.03.04).

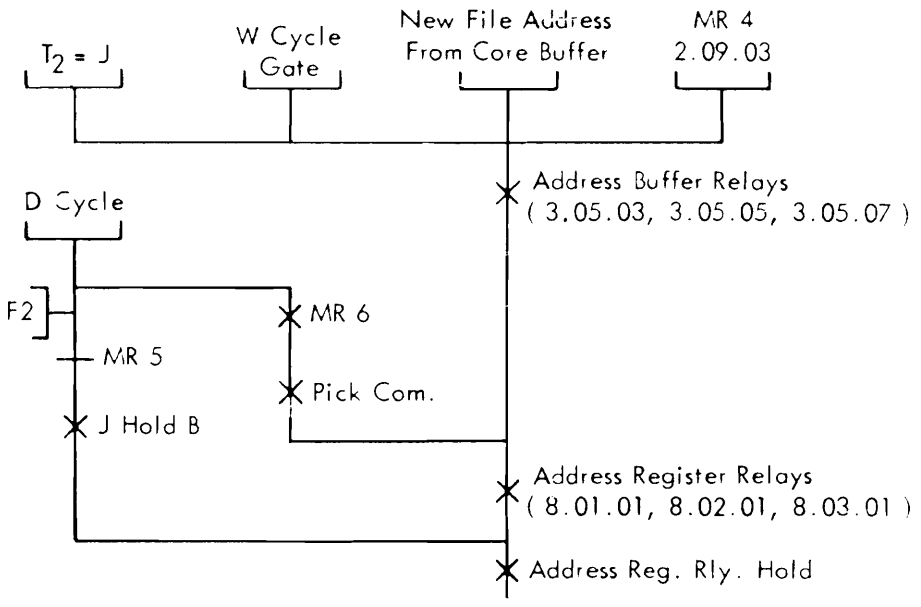


Figure 73. Pick and Hold Address Register Relays

Address Register Relays: The data flow chart for a servo operation (Figure 72) illustrates the path of the file address data. During R cycle the 5 specified characters are read into core buffer. On W cycle they are read out of cores as data to J and stored in the thyratron controlled address buffer relays. MR4 provides plate voltage for these thyratrons on a $T_2 = J$ operation. When MR6 makes, the address buffer relays are sampled to pick the address relays in the file. Just prior to reading the address out of cores, MR5 picks,

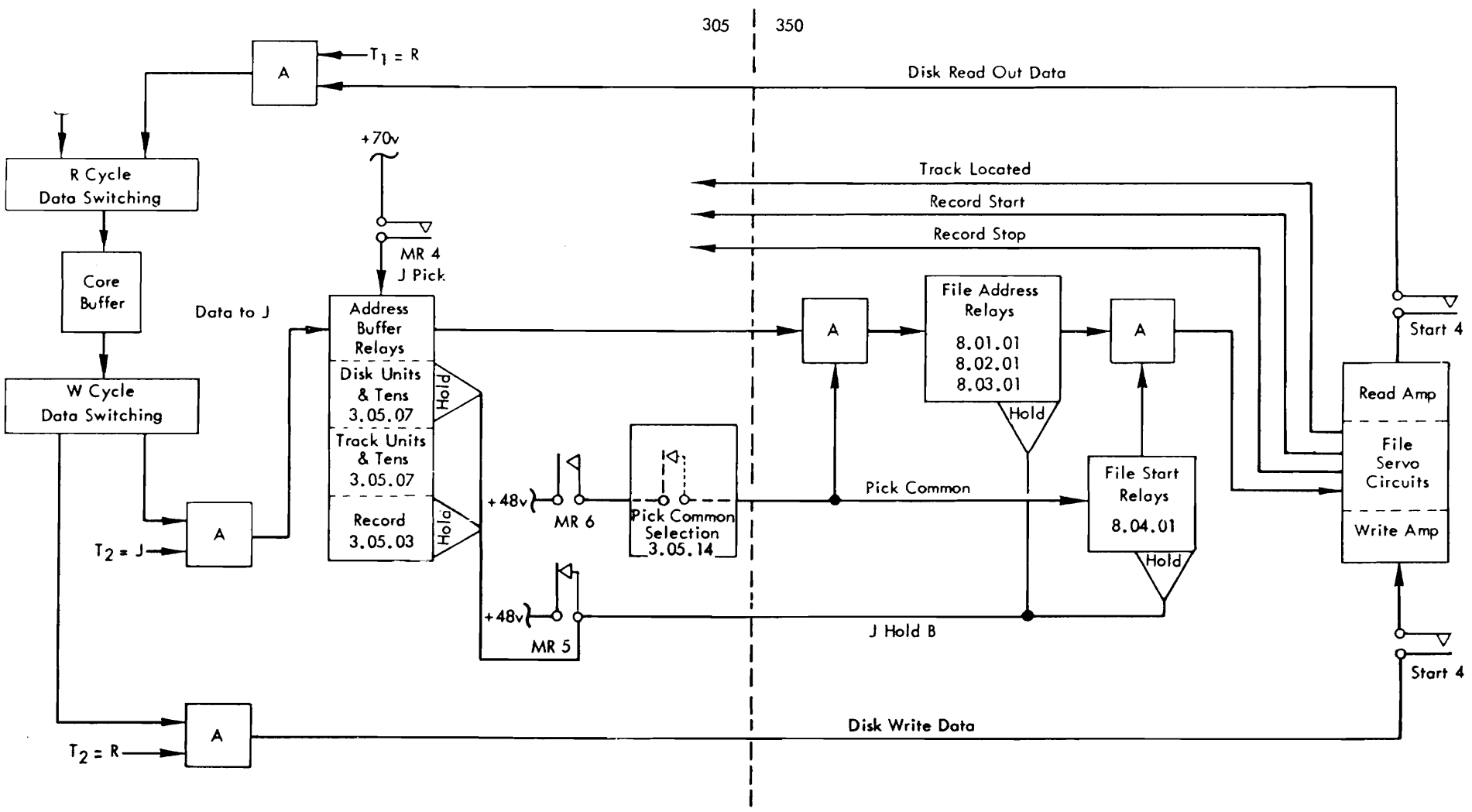


Figure 72. File Data Flow and Servo Control

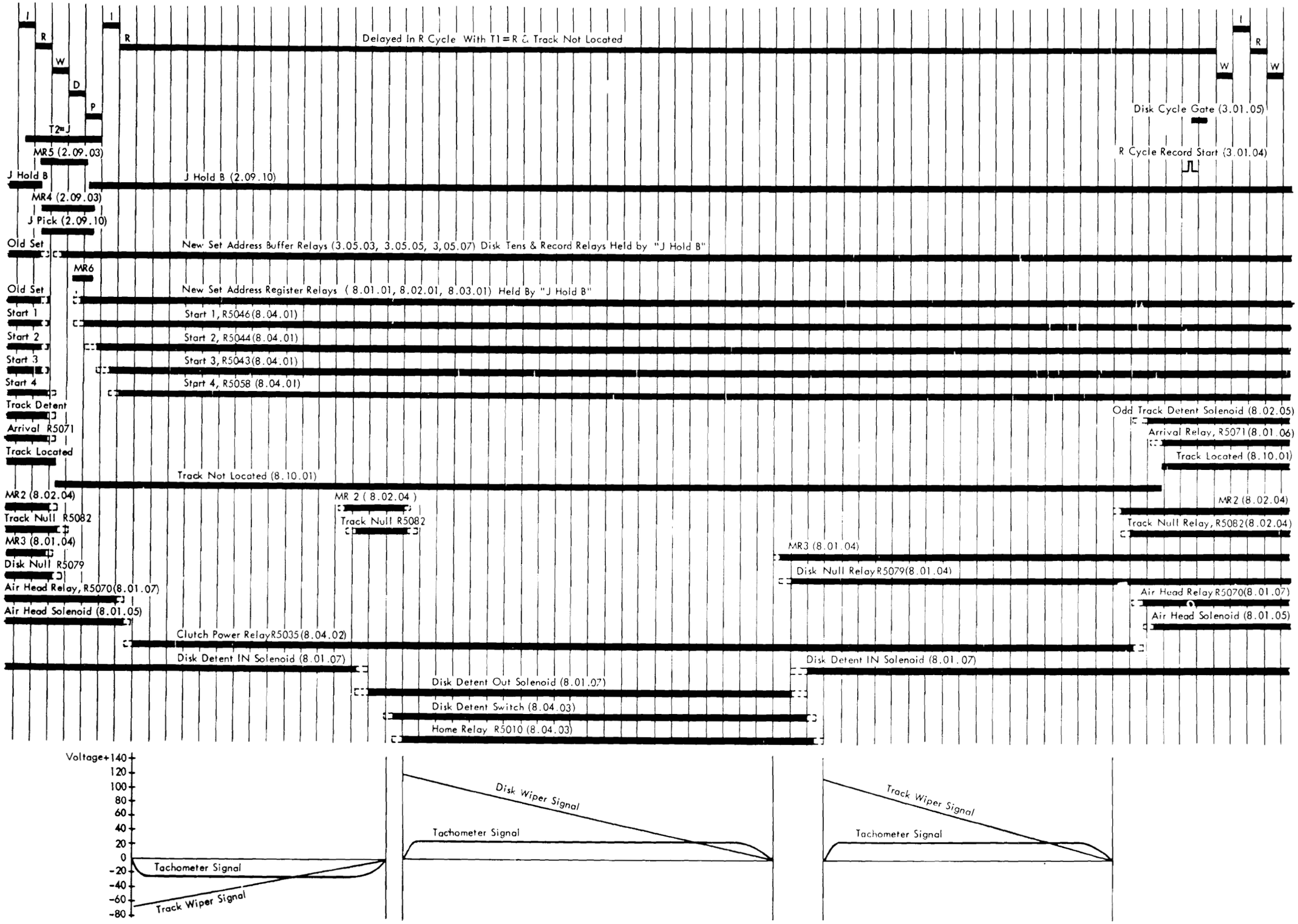


Figure 74. Sequence Chart of Servo Operation From Address 01451 to 49955 Followed by $T_1 = R$

dropping the hold on all file address relays, file start relays and some of the buffer relays. After the new relays have been picked MR5 will drop out establishing a hold until the next servo instruction. The only address buffer relays held are the record relays (for record advance purposes), and the disk tens relays (for dual file purposes).

The timings of these MR relays for a $T_2 = J$ operation are shown on System Diagram 0.09.05. MR5 will pick on 2.09.03 at the start of R cycle (3F3a), and drop out at F2 of second D cycle (same as D cycle). This lowers the J hold B line on 2.09.10, dropping the address buffer relays (3.05.03, 3.05.07). All file address relays (8.01.01, 8.02.01, 8.03.01) are dropped since their hold lines become J hold B on 3.05.11.

MR4 picks at the same time MR5 does on 2.09.03 but holds up longer, until D cycle end. This raises the J pick line on 2.09.10 to provide +70 volts to all the address buffer thyratrons (3.05.03, 3.05.05, 3.05.07). During W cycle the core data appears as data to J from C99 through C95 ($A_2B_2 = 99$ and MN = 05). On 3.05.01 this data is separated into 4 bit lines which feed the associated thyratrons of the address buffer relays. The units position of the core buffer appearing at C99 time is gated to the record address thyratrons (3.05.03). The next two characters, track units and track tens, are gated to the track address thyratrons (3.05.05). The disk address characters go to the disk address thyratrons (3.05.07).

To transfer the address from the process unit to the file address register, on 8.01.01, we must ground the proper pick line and place + 48v on the pick common line. The pick line grounding is accomplished on 3.05.12 and 3.05.3 by the points of the previously energized address buffer relays. The pick common line passes through 8.00.07 on one of eight common lines, depending upon the file configuration. For a single 5 million character file installation, pick common access 0/3 disk 00-49 would be used. This particular line is connected to + 48v through MR6 N/O points (3.05.14). MR6 will be up during D cycle (2.09.03). The pick common selection circuits on 3.05.14 will be more fully explained under "350 Optional Features."

During D cycle MR5 dropped out, establishing a hold on all file address relays. The points of these relays have now set up new ground points on the disk potentiometer (8.01.03) through the relay tree on 8.01.02, and on the track potentiometer (8.02.03) through the relay tree on 8.02.02.

The following table will aid in tracing the pick circuits for the address 49955:

	Address Register Relay		Address Buffer Relay Point	
Disk 40	R5137	(8.01.01)	R355-5	(3.05.13)
Disk 8	R5121	(8.01.01)	R347-2	(3.05.12)
Disk 1	R5130	(8.01.01)	R342-2	(3.05.12)
Track 80	R5166	(8.02.01)	R339-2	(3.05.12)
Track 10	R5152	(8.02.01)	R335-2	(3.05.12)
Track 4	R5156	(8.02.01)	R330-2	(3.05.12)
Track 1	R5134	(8.02.01)	R327-2	(3.05.12)
Record 4	R5163	(8.03.01)	R308-3	(3.05.12)
Record 1	R5157	(8.03.01)	R305-3	(3.05.12)

Start Servo Operation

The initiation of the servo operation is controlled by the start relays on 8.04.01. These relays are picked and held along with the file address relays with MR6 and MR5 (de-energized) respectively. The start hold access line becomes J hold B on 3.05.11, while the pick common line goes to MR6.

Retract Air Heads: The air head solenoid on 8.01.05 is de-energized as soon as the head relay (R5070) drops. This is only necessary if the disk address has been changed, so on 8.01.07, R5070 is dropped only if the disk null points (5079-5) are open after the start relays repick. For our example, the disk null relay (R5079) on 8.01.04 will be down. A positive disk null signal is applied to the null detector from the disk potentiometer through the start relay points, G5046-7 N/O on 8.01.03. The disk wiper is located at disk 01 while the new ground point is at disk 49, through the address relay tree on 8.01.02.

While the start relays are de-energized, and the new address is being transferred to the file, the disk null relay was dropped by applying —60v to the null detector through G5046-7 N/C points on 8.01.03. The head relay (R5070) on 8.01.07 is held at this time by the normally closed start relay points.

Move Arm Out: To accomplish this objective the carriage must still be detented, the track detent must be released and the out-up clutch energized. The track

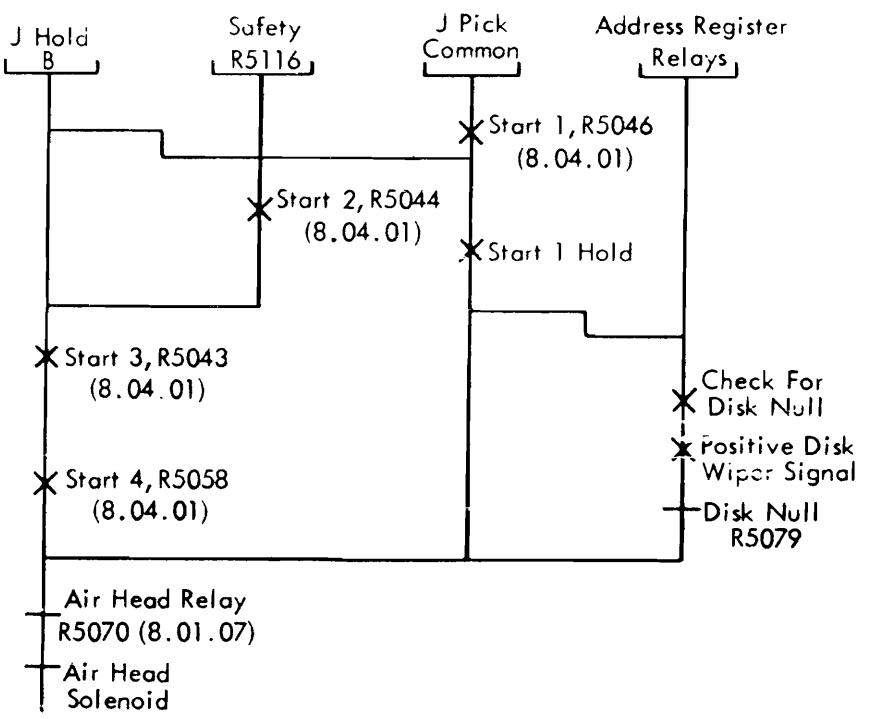


Figure 75. Retract Air Heads

detent solenoid (8.02.05) was de-energized when the start relay (R5046) dropped during R cycle. The disk detent in solenoid (8.01.07) is still energized through the home relays points (R5010-1 N/C) and track null points (R5082-2 N/C).

The out-up clutch is energized by applying a negative track signal (clutch) to the clutch amplifier on 8.05.01 and closing the clutch power relay points (R5035) on 8.05.02. The negative track signal from the track potentiometer on 8.02.03 is provided by grounding the home position. The de-energized disk null relay indicates the arm must be completely retracted to facilitate a shift to a new disk, so a disk null point (G5079-11 N/C) places ground potential at the track potentiometer plus end, beyond track address 00.

The clutch is actually energized when R5035 on 8.04.02 is picked. With no disk null (R5079 normal), R5035 picks when the air head begins retracting (R5070 normal) and the track detent is out. The CD cathode is grounded through the track detent switch on 8.01.06. If the read/write heads are already near the edge of the disk due to a previous track address of less than 20, we must delay arm movement until the air heads are fully retracted. In this case the clutch delay relay (R5006) will be energized and holding. The R5006-1 N/O points place a negatively charged capacitor on the grid of the CD, which must discharge through the R5070-4 N/C points before the clutch power relay is picked.

Retract Disk Detent: When the arm is fully retracted, a track null is developed. The track null points (R5082-4 N/O on 8.01.07) close to energize the disk detent out solenoid. At the same time the disk detent in solenoid is de-energized with the opening of R5082-2 N/C. When the disk detent is disengaged the home relay (R5010) on 8.04.03 will be energized.

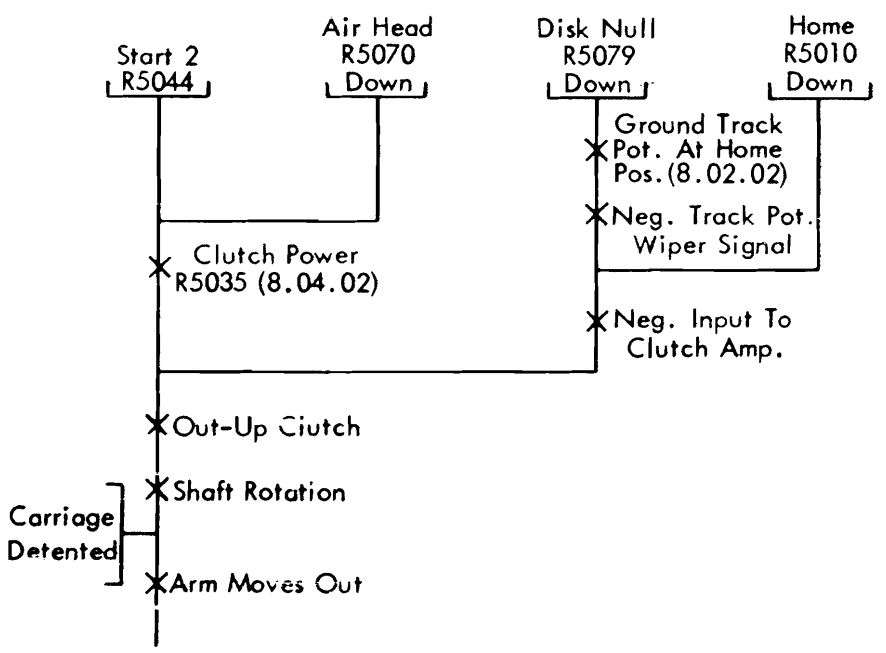


Figure 76. Move Arm Out

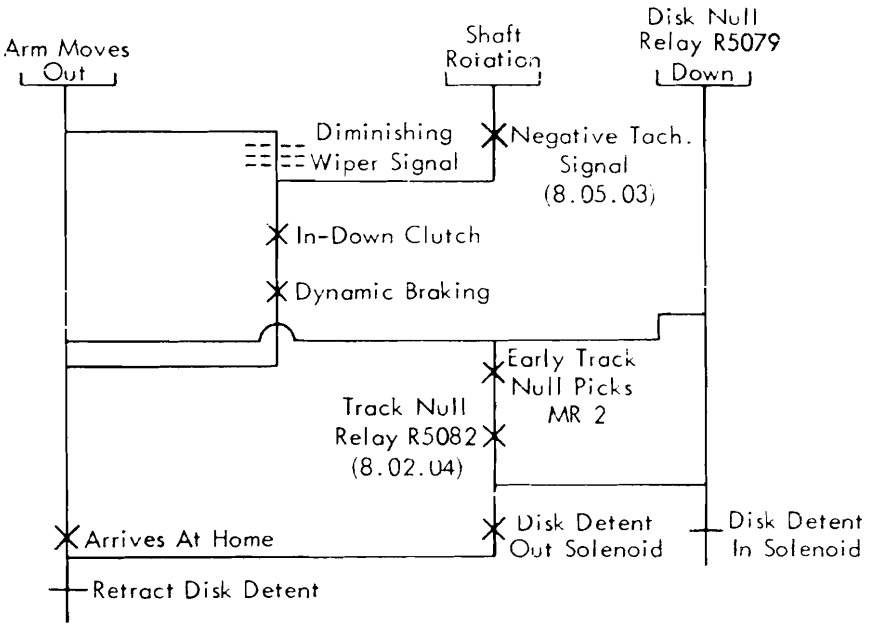


Figure 77. Retract Disk Detent

In order to save time when transferring from track drive to disk drive the track null circuits are designed to pick MR2 early (8.02.04) when moving to the home position. Figure 78 shows the disk null points in the grid circuit of the left hand section of A11b. When R5079-8 is normal the grid is tied to a more negative point on the cathode resistors of B11b. This cuts off the right hand section of A11a before the track signal actually reaches zero volts.

Move the Carriage Down: The fail-safe mechanism locked the arm in the home position when the disk detent was retracted. Energizing the in-down clutch on 8.05.02 will move the carriage down until a disk null is detected. A positive disk signal (clutch) is applied to the clutch power amplifier on 8.05.01 through the transferred home relay points (G5010-8). In our example the carriage is at location 01 (8.01.03) while the disk potentiometer is grounded at location 49 through the address relay points on 8.01.02.

Engage Disk Detent: When the disk null is detected the disk detent in solenoid is energized through the R5079-4 N/O points.

Move the Arm In: Energizing the in-down clutch will now move the arm in until a track null is detected at the addressed track. A positive track signal can be applied to the clutch power amplifier (8.05.01) when the home relay (G5010) drops. This occurs as soon as the disk detent is engaged on 8.04.03.

The track potentiometer (8.02.03) will be grounded at position 95 by placing the 10 one ohm resistors and then the ten ohm resistor on 8.02.02 in parallel with the markite strip from position 100 to position 80. This is done through the following N/O points on 8.02.02: from position 100, G5166-5 N/O, G5152-7 N/O, the ten one ohm resistors, G5152-6 N/O, the 10 ohm resistor, G5152-8 N/O, G5166-6 N/O to position 80. The fifth one ohm resistor down will be grounded through the units track address relay points.

Figure 78. Track Null Detector (8.02.04)

The full application of the postive track signal (clutch) to the power amplifier on 8.05.01 will be delayed following a carriage movement until the carriage settles down. Accerelator limiter points, R5004-1 N/C and R5005-1 N/C will open, sequentially, after the carraige reaches the addressed disk. On 8.04.03, R5004 picks when the disk detent switch transfers and R5005 picks shortly later when the 10 μfd condenser has charged.

Engage Odd Track Detent: When the wiper on the track potentiometer reaches the addressed position, the track signal decreases to zero volts. This picks the track null relay (R5082) on 8.02.04 which will energize the odd track detent solenoid on 8.02.05.

Extend the Air Heads: The air head relay (R5070) on 8.01.07 is picked through the track null relay points, R5082-2 N/O. This energizes the air head solenoid on 8.01.05.

Track Located Signal: This signal, developed on 8.10.01 by the closing of the arrival relay points (R5071-2 N/O), informs the 305 process- unit that the servo is complete. The arrival relay on 8.01.06 picks as soon as the track detent switch transfers if a track null exists and the air head relay is picked.

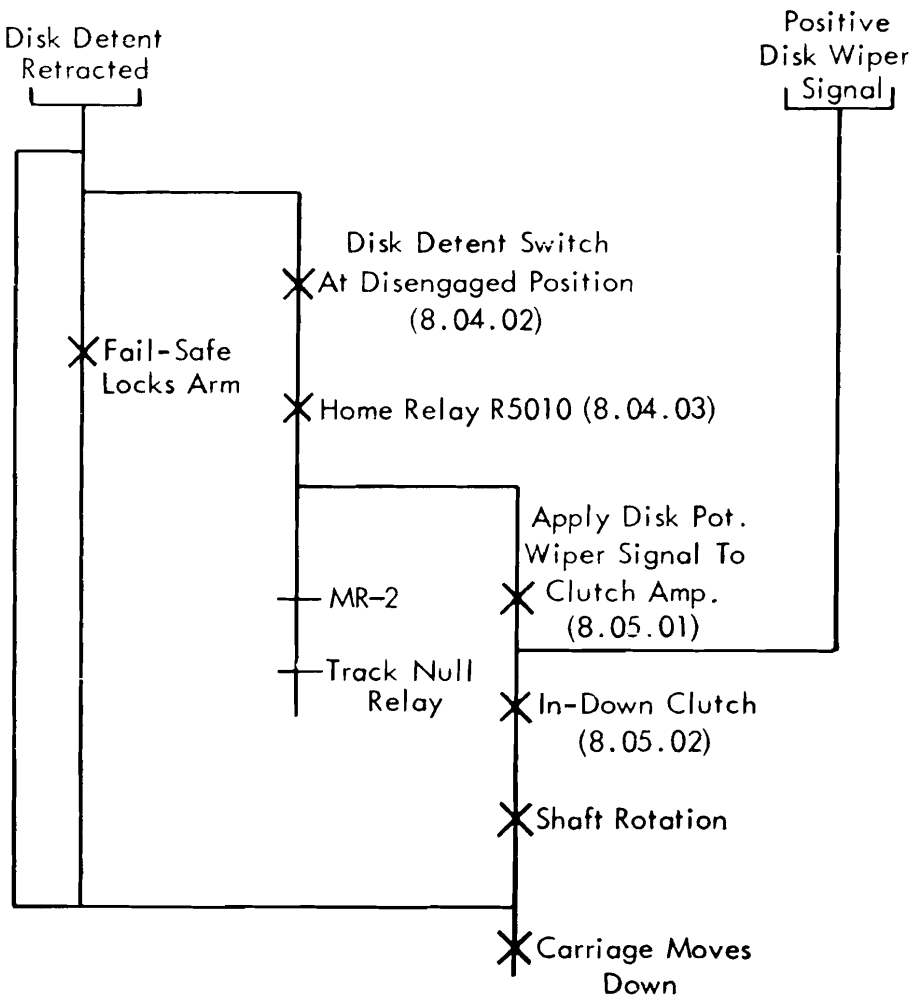


Figure 79. Move Carriage Down

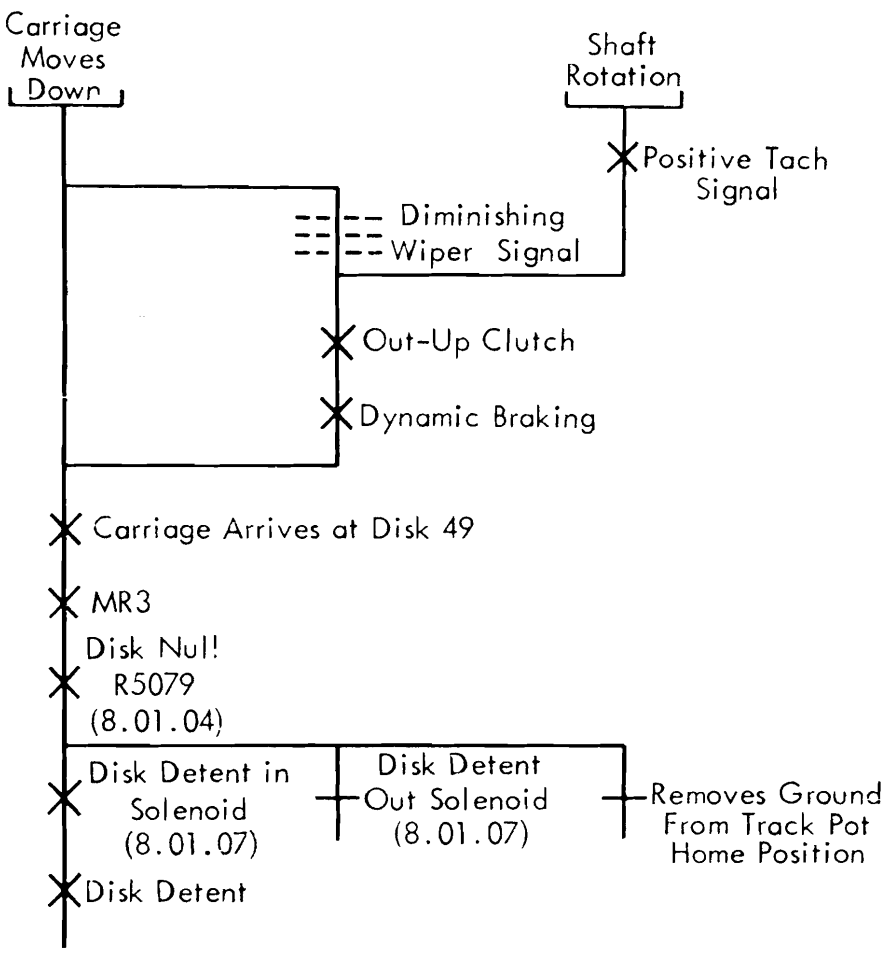


Figure 80. Engage Disk Detent at Disk 49

Record Selection: The record address relay points are used to select the correct record head through the network on 8.03.02. In our example, address 49955, record address relays 1 and 4 provide a record start pulse from the 0/5 head and a record stop pulse from the 1/6 record head. These pulses will tell the process unit when to start reading or writing record 5.

The bottom head on the access arm will be selected by energizing the side relay (MR1) on 8.10.03.

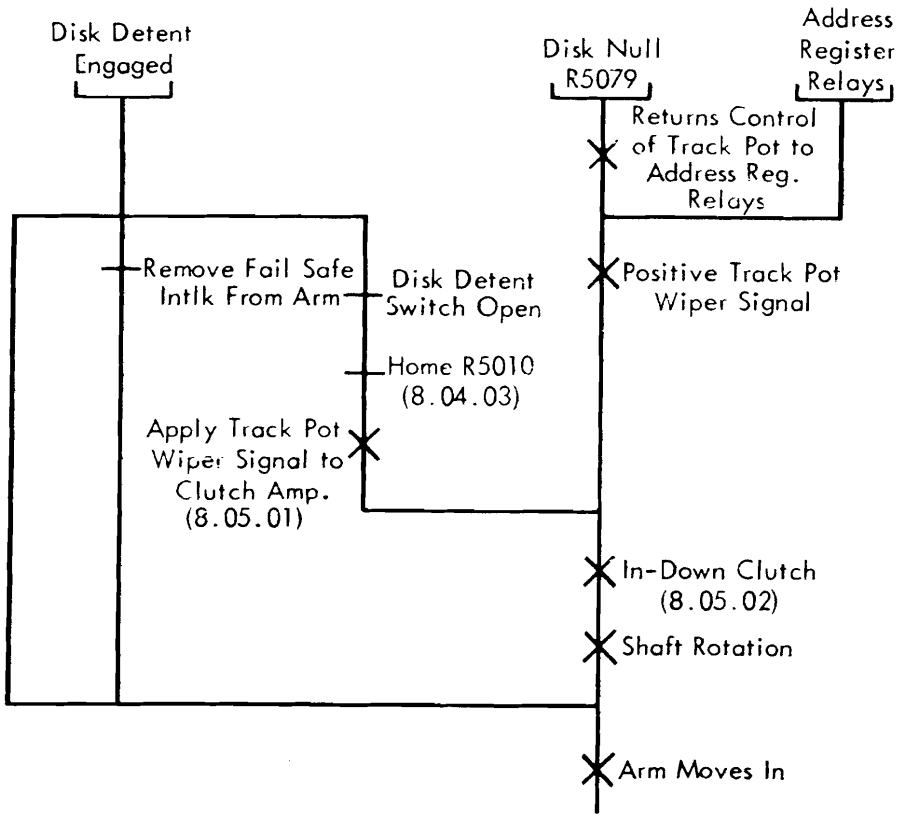


Figure 81. Move Arm In

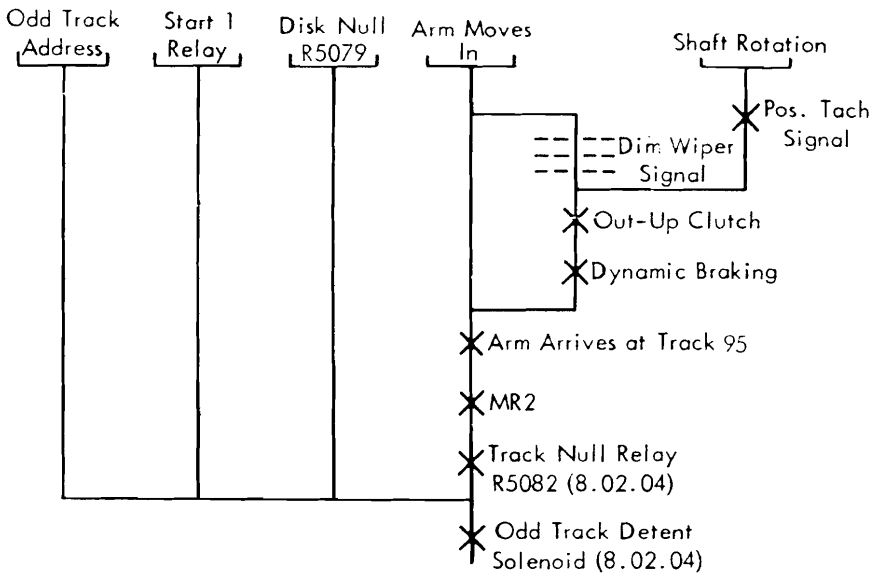


Figure 82. Engage Odd Track Detent at Track 95

Figure 74 is a sequence chart of the entire servo operation.

Customer Engineering Track Selection

One of the two customer engineering tracks (inner or outer) on an addressed disk is selected automatically when the test lock switch is ON and $T_2 = J$ operation is initiated. If the record address is an odd number, the outer track is selected. If the record address is even, the inner track is selected.

The test run relay, GR5119 (8.11.01) is energized when the test lock switch is ON (6.15.04). With GR5119 energized in addition to GR5079, control of the track address is exercised by GR5134-12 (8.02.02). The entry of an even track address will leave GR5134 down, and will apply ground to the 100 (inner CE track) tap of the track pot. The entry of an odd track address will cause GR5134 to be picked, and will apply ground to terminal "B", which is a point on a voltage divider connected between the 00 tap and the positive input to the track potentiometer. This will establish ground level at a point one track from the track 00 position.

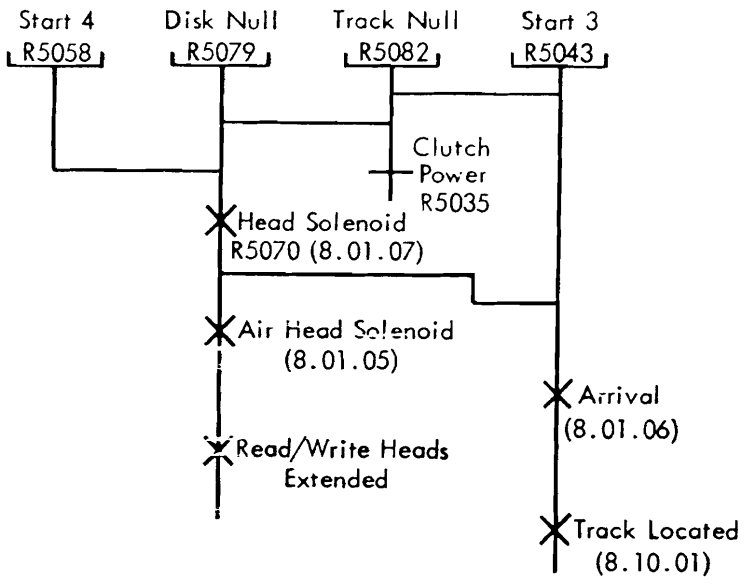


Figure 83. Extend Air Heads; Obtain Track Located Signal

File Read/Write

Basic Circuits

The method used to record information on the RAMAC file differs from that used on the process drum. On the drum one polarity of flux indicates a bit while the opposite polarity indicates no bit. On the disk an NRZI (non return zero IBM) system is used where a change in flux represents a bit while no change represents no bit (see Figure 86). One additional difference is the fact that all space bits (Bs) are inserted and written for each character. This is done only to stabilize the file read circuits.

The physical arrangement of the read/write coil and the erase coil are shown in Figure 84. The coil wiring is shown on System Diagram 8.10.02. Notice that the read/write coil is centertapped with the erase coil feeding the tap. One of the two heads (top or bottom) will always be selected by the points of the side relay, MR1. This is picked by analysis of the units position in the file address relays (8.10.03). When writing on the disk, the write relay 5057 will be energized and the arrival relay 5071 will be up. Electrons will flow from the head ground through the top head erase coil (assume MR1 is normal). At this point it will flow through either half of the read/write head, depending on which write amplifier (A or B) is conducting. One of the two will always be conducting during a file write operation and a bit of information coming in will cause the other to conduct. The resultant flux pattern laid down on the disk will change polarity only when a bit of information is written.

WRITE AMPLIFIER (8.10.05)

A detailed drawing of the write amplifier is shown in Figure 84. The three CD308's will conduct on either the left or the right side to pass write current one way or the other through the read/write head. The condition of trigger D8, determines which half of these CD's conducts. The two outputs of the trigger feed two inverters at B8a, and the output of the inverters goes to the grids of the CD308's.

The start 4 relay R5058 will be energized any time the arm is not in a servo operation. When a file write operation takes place the disk write data line will have ∅C data pulses from the core buffer, plus inserted Bs ∅C pulses on it. These pulses are inverted and

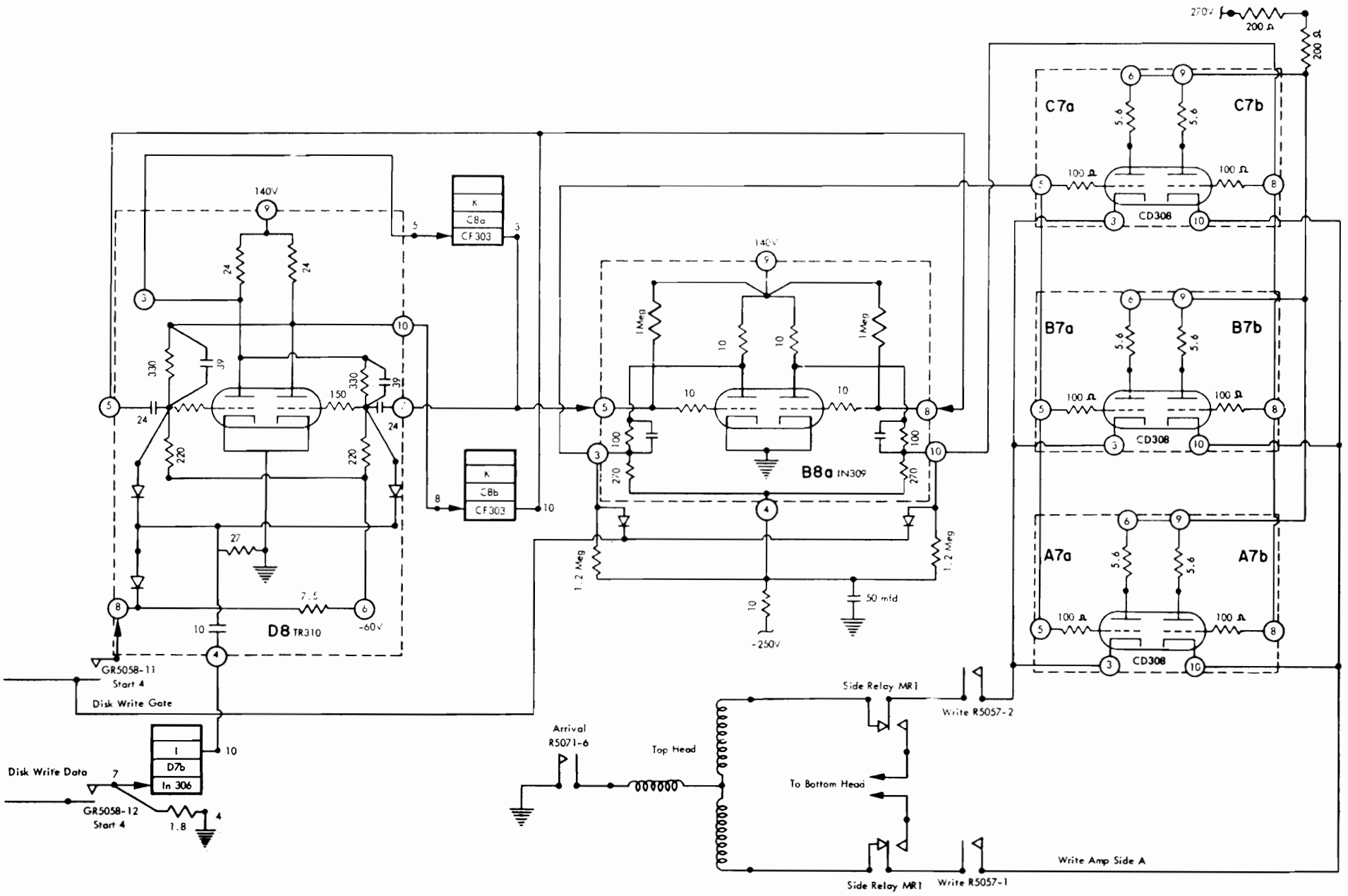


Figure 84. Write Amplifier (8.10.05)

fed to the trigger D8 through a binary input, each one flipping the trigger to the opposite condition. The CD308's will follow the trigger, one side conducting with the other side cut off, until the trigger changes its status.

Because the writing of the data must occur at a specific time in the revolution of the disk, there must be some way to prevent either side of the CD308's from conducting until ready. The disk write gate will be low until the desired sector on the disk is reached. This low on pin 8 of the TR310 keeps both halves of the trigger cut-off. The two outputs will be high and are inverted to lows on all grids of the CD308's. So we can say the disk write gate determines the starting and stopping time of current flow through the read/write head.

The erase coil, with current always flowing through it in the same direction, is necessary to eliminate any peripheral flux from the previous record. The width of its field is greater than that of the read/write head.

Read Amplifier (8.10.04)

Once the data has been stored on the disk in the form of flux reversals, the read/write head can be used to read these changes. The read amplifier is shown in Figure 85. When a change in flux passes the head, a small current will flow through the head coil. This places a pulse of one polarity on one grid of the AM306 (D4), and a pulse of the opposite polarity on the other grid. This 2 phase signal will be amplified through the four stage differential amplifier. One advantage of the push-pull amplifier is the elimination of noise picked up in the head leads. These noise pulses will generally appear on only one input to the amplifier and the degenerative feedback between the two halves of the amplifier will eliminate them.

The outputs of the amplifier A4, will have alternate positive and negative pulses representing data. The plus pulses from first one output and then the other are combined at the OR cathode follower A5, then shaped at the Schmitt trigger C5 to provide disk read out pulses.

Automatic Gain Control

Because of the difference in surface speed between the inside and the outside of the disk, signals from the inside track will vary from 11 to 14 millivolts while signals from an outside track will vary from 26

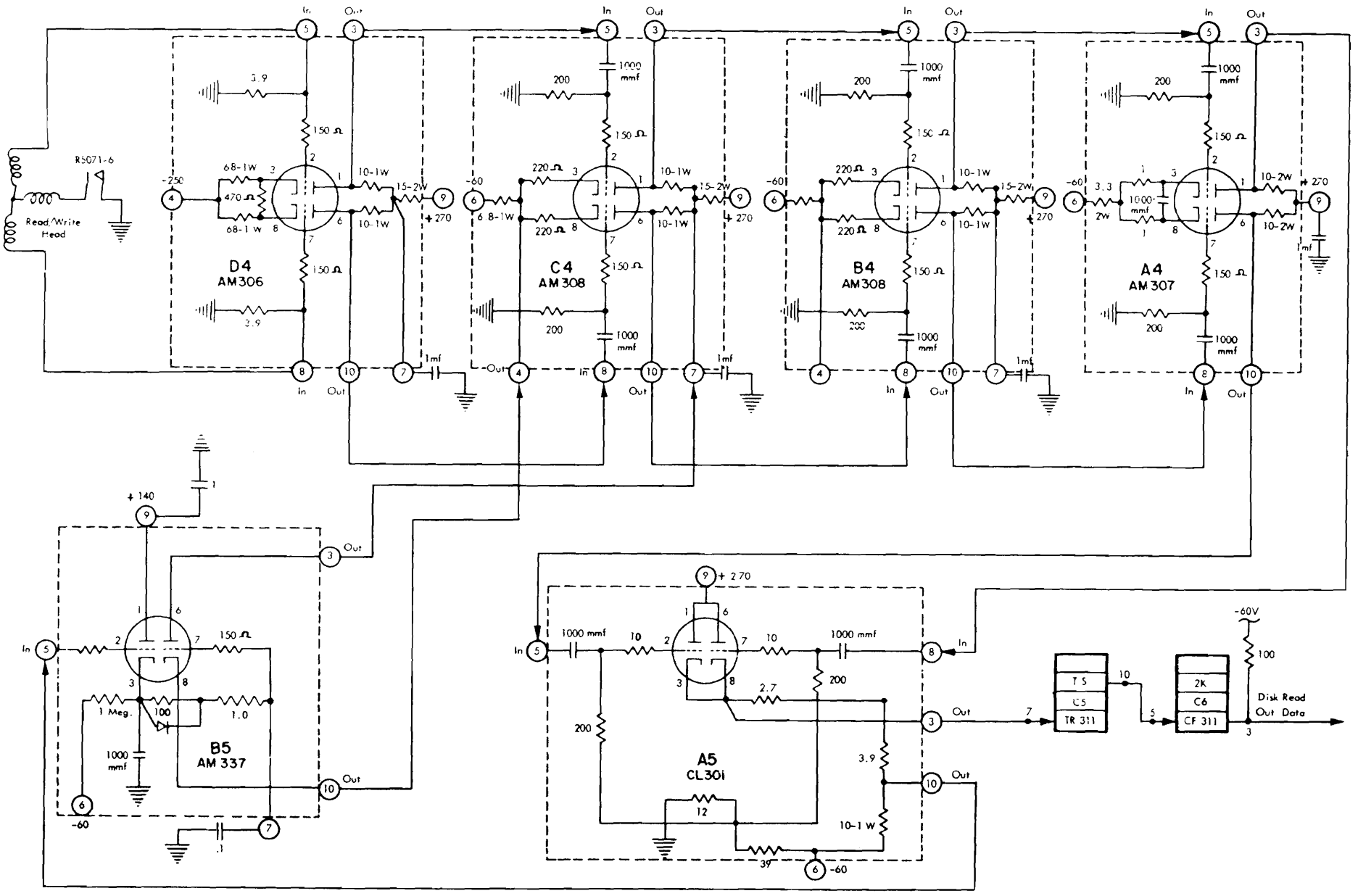


Figure 85. Read Amplifier (8.10.04)

to 40 millivolts. The read amplifier must be able to accommodate signals between these extremes. To accomplish this an automatic gain control circuit (B5-8.10.04) samples the output pulses and varies the amplification of the second stage at C4, accordingly. For example, if the output signals increase in strength it would be desirable to reduce the amplification of C4. This can be done by lowering the plate voltage and raising the cathode voltage. The signals are sampled at pin 10 of A5 and cause the left hand section of B5 to conduct more heavily, increasing the charge on the .1 μf capacitor between pin 7 and ground. This raises the voltage on pin 7 causing the right hand section of B5 to conduct more heavily. This in turn raises pin 10 and lowers pin 3, which has the desired effect on C4.

Prior to dual access and double density files, the first few bits of the record were (when reading) used to set the level of amplification. To prevent any possible distortion of the first few bits, a series of ∅C AGC pulses are now written ahead of the data portion of each record. These pulses are written each time the record is altered and are used when reading to establish the charge level of the .1 μf capacitor.

Disk Clock

The only pulses generated by the file itself are the five record start pulses for each revolution. These are developed by a permanent magnet, fixed to the top dummy disk,as it passes each of the five equally spaced record start heads fixed to the file housing (8.03.04).

The record start heads are numbered 0 to 4, or 5 to 9, depending upon whether the top read/write head or the bottom read/write head on the access arm is selected. Since the disk is revolving at 1200 RPM, a start pulse occurs every 10 milliseconds. These pulses tell the 350 file when to start writing (or reading) a record and when the record should have been finished.

Between two start impulses 100 characters must be written or read (with a gap before and after). This requires a clock to control the character rate and to identify each character and bit (or no bit). A clock track written on the disks would not be feasible because of the inability to predict the exact position of the read/write head from one servo to the next. On the drum, the heads are permanently fixed but not so in the file. For this reason the disk clock must be generated by an external oscillator during a write operation. On a read operation the data being read will control the clock.

When writing on the disk the spacing of the data bits is determined by the speed of advancement of the core buffer bit ring. On a track to track transfer, the core bit ring was driven by ∅A pulses from the process drum clock. On 3.02.02 it can be seen that the ∅A pulses to the cores come from the disk clock instead of the process drum clock when T = R (file read or write). These disk clock pulses are developed on 3.01.02 from three single shots. The rise of the disk clock, a square wave signal of approximately 12 μs in duration, triggers the ∅A single shot. The fall of the 2¼ μs ∅A pulse initiates the 2¼ μs ∅B pulse. The ∅C single shot will be triggered by the fall of ∅B or the fall of the disk clock, whichever occurs later.

The disk clock square wave is generated by an oscillator on 3.01.01. When writing into the file, one oscillator (consisting of pluggable units 2D6 and 2F6a) determines the frequency of the clock. It is adjusted to step through 100 characters plus a 1200 μs gap during the interval between two consecutive record starts. Because the records stored on the file must be retained permanently while the speed of the disks and the oscillator frequency may vary, some method is required to keep the disk clock frequency synchronized with the rate of the data bits being read from the file. To accomplish this there are two oscillators used when reading. The bits on the disk read out line switch one oscillator, then the other, to the disk clock line. This can be seen in Figure 82. Notice that when the oscillators are switched, the active oscillator always begins its sine wave at the midpoint and proceeds to the lower half of the oscillation. Raising pin 5 of the CF302 portion of the oscillator to ground level prevents it from oscillating.

When writing, the oscillator at 2D6 and 2F6a will conduct continuously in the following manner. Pin 5 of 2F6a drops below ground level because 2D7a is not conducting. This is due to the high at pin 10 of the clock switching trigger 2E7, which will be held 10 pin high. At the same time the low at pin 3 of this trigger is inverted, causing conduction at 2D7b, blocking the second oscillator at 2F6b. The clock switching trigger is held 10 pin high by raising the write clamp line (access 0/3).

When reading from the file the write clamp line will be down. The disk read out data pulses are inverted and binarilly fed to the trigger at 2E7, alternately switching it ON and then OFF. This alternates the oscillators through the two AK's, 2D7a and 2D7b. During both reading and writing the clock control trigger at 2B6 is 10 pin high and has no effect on the oscillator operation. When it is desirable to stop both oscillators, this trigger is turned 10 pin low by a negative shift on the clock set line. This causes both AK units to conduct, stopping the oscillators.

Figure 86 illustrates the operation of the oscillators, the clock and the phase generating circuits for reading and writing. To assure that the oscillators will switch

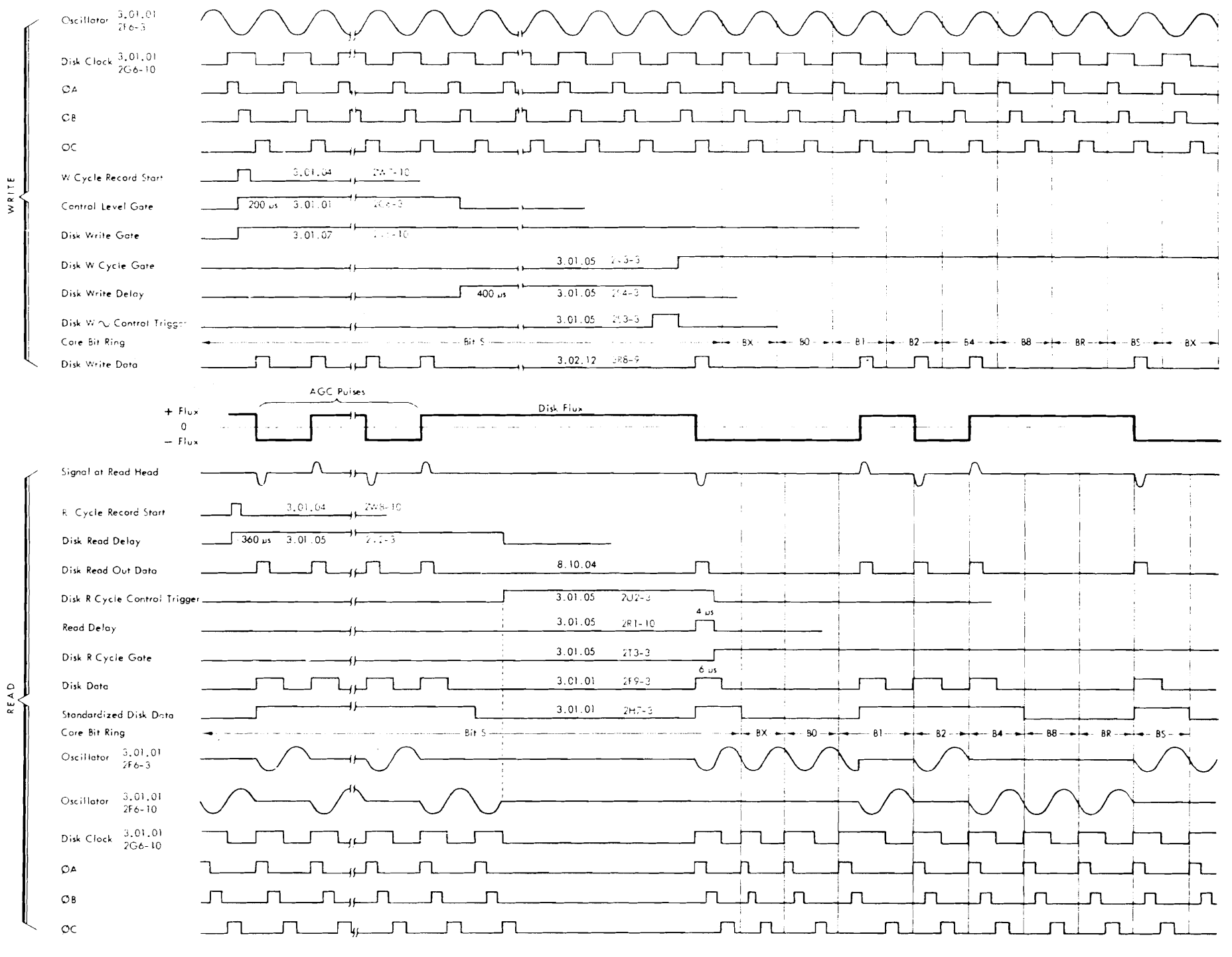


Figure 86. File Write and Read Waveforms

at least twice every character, the space bits are inserted. Notice in the diagram that one oscillator is tending to speed up on the read operation. This increases the duration of the B1 clock cycle. The ØA and ØB pulses have been advanced; however ØC, which is initiated by the fall of the clock pulses, is still in time with the disk data out. This is important since ØC's are used later on to sample the disk data.

File Write Operation ($T_2 = R$)

Two data flow charts in Figure 88 and a sequence chart Figure 87 are provided to supplement the write-up. The file write operation, for example X99R9900bb, can begin when the track has been located. This instruction will transfer X track (100 characters) to core buffer on R cycle. On W cycle the data in the core buffer is transferred to the file location specified by the address relays. As a check, a second RW cycle will follow the first W cycle. On the second W cycle the data just written will be read from the file and compared, character by character, to the data from X track which is placed in cores during the second R cycle. Any variation in the two records will stop the machine.

OBJECTIVES:

1. $T_2 = R$ causes an IRWRW sequence.
   a. Pick up the write relay R5057.
   b. Store check trigger differentiates first Wcycle from second.
2. During first W cycle data flows from core buffer to addressed record position in the file.
   a. Record start.
   b. Write AGC pulses (ØC) for 200 µs.
   c. Write core character 00, 600 µs after record start.
   d. Insert Bs for each character.
   e. The disk clock controls core ring advance and core starts.
   f. Stop file write after core character 99 is written.
   g. Check file speed and write speed.

3. On second R cycle re-read selected drum track into cores.
4. On second W cycle data flows from file record just written to comparing circuits and data from cores flows to comparing circuits.
   a. Record start.
   b. Block AGC pulses from data line.
   c. Develop standard disk data, ØA to ØA, to compare circuits.
   d. Disk clock advances cores and reads out of cores to compare circuits.
   e. Stop machine and turn on file check light if a comparing error occurs.
   f. Stop file read after core character 99 is compared.

IRWRW Cycle Sequence: A T_2 character of R will command the machine to begin a file write operation by picking R5057 on 8.10.01. This relay is energized by firing the thyratron (3A11) on 3.01.06 with I cycle end and $T_2 = R$. Notice that the file hubs on the 305 control panel must be jackplugged. The relay will remain energized until the thyratron is cut-off by firing a second thyratron at 3B11. This occurs at the end of the first W cycle.

The store check trigger (2T4) on 3.01.05 controls the special cycle sequence for $T_2 = R$. It also identifies the first W cycle and the second. Every I cycle it is turned ten pin high. The trigger remains ten pin high until the fall of the disk write delay (2S4). This occurs just prior to writing the record on the first W cycle. It will then remain 3 pin high throughout W cycle, the second R cycle and into the second W cycle. Then it is turned ten pin high by the fall of the disk read delay, 2V2, just prior to reading the record for comparing. The read delay is initiated by W cycle record start and store check switching at "and" inverter 2S5a. This can be seen in Figure 87.

On 1.03.05, R cycle ready trigger will be turned ON with W cycle end and store check for the second RW cycle. Both I and D cycle will be blocked at this time.

First W Cycle: The data flow during this cycle is shown on Figure 88. The core buffer contains 100

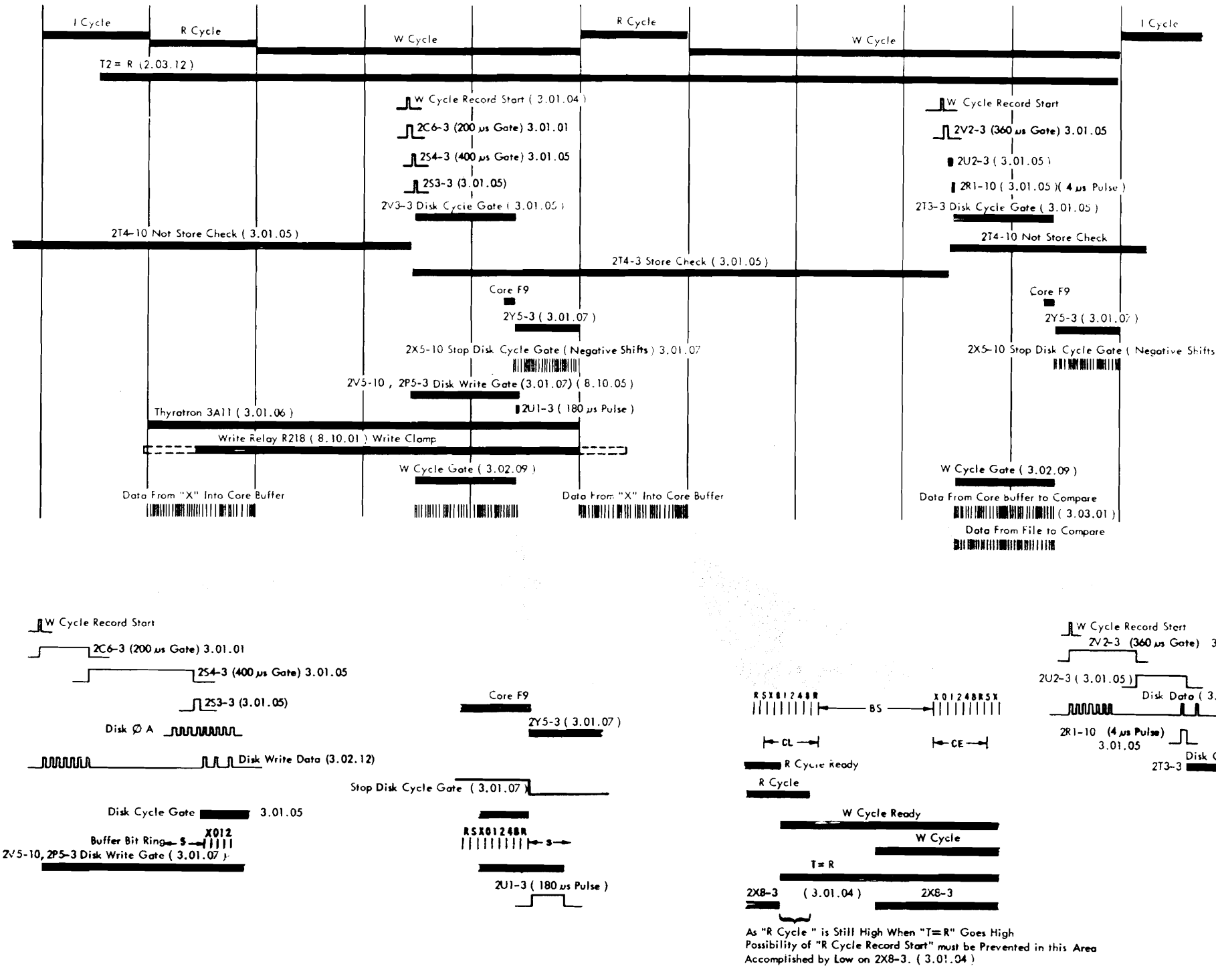


Figure 87. Store Data into File (X99R9900bb)

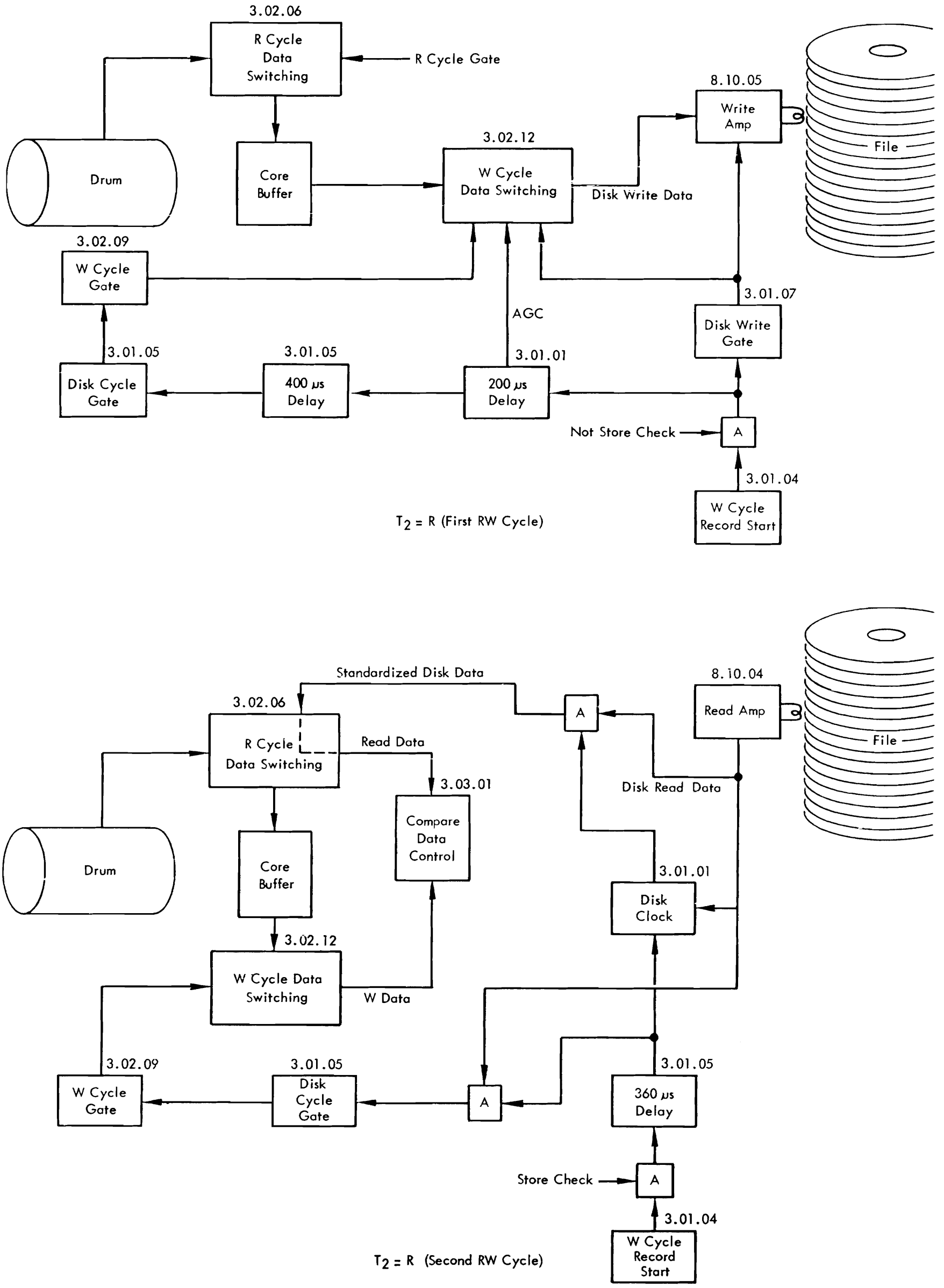


Figure 88. Data Flow and Controls, $T_2 = R$

characters to be written on the disk. Once W cycle begins, the machine will wait for the proper record start pulse; then, after a 600 μs delay, begin writing.

The record start pulse originates on System Diagram 8.03.04. For example, if the record address is 49995, the record start pulse selected will be from the 0/5 record head. As the permanent magnet passes the head a pulse is generated. On 8.03.02 this 0/5 pulse will be selected since the record 1 and record 4 address relays are up. After amplification and shaping on 8.03.03 the start pulse will become R cycle or W cycle record start on 3.01.04. The W cycle record start is conditioned by W cycle, T = R, and track located signal (2W7). T=R will be high while W cycle ready is high, if T_2 = R, as in our case. This means T = R will also be up while R cycle is still up (from CLB1 to CLBR). To block a possible R cycle record start at this time the "and" inverter at 2Y8b will be conducting.

During the first W cycle (not store check still high) the record start pulse is inverted at 2S5b on 3.01.05 and its leading edge triggers the 200 μs single shot, 2C6 on 3.01.01. The rise of the 200 μs gate from pin 3, labeled control level gate, is placed on pin 7 of the AI at 3R8 on 3.02.12. If disk write gate is high at this time we will place AGC pulses ($\varnothing$C) on the disk write data line. The disk write gate trigger (2V5 — 3.01.07) will be set 10 pin high by the leading edge of the 200 μs delay, labeled start record write delay. The disk write data on 3.02.12 is inverted on 8.10.05 and used to alternate conduction through the two halves of the read/write head.

The 400 μs disk write delay (2S4 — 3.01.05) is initiated by the fall of the disk W cycle delay gate, which is the 200 μs delay gate. During this 400 μs nothing is written on the disk, however the gap is being developed. At the fall of the 400 μs disk write delay the store check trigger, 2T4, and the disk W cycle control trigger, 2S3, are turned 3 pin high. The fall of the next $\varnothing$A sets the disk W cycle gate 3 pin high, raising the disk cycle gate line. This gate, 600 μs after record start, signals the machine to start reading out of core buffer to the disk write amplifier. On 3.02.08 it will drop the not W cycle gate, which inverted becomes the W cycle gate. On 3.02.02 we can now send phase pulses to the cores, each $\varnothing$A advancing the core bit ring, and every eighth bit time (Bit S) the $\varnothing$C will develop a core start on 4.11.00 at 4H7. This start reads out of the cores to the character register and 3 μs later advances the core units ring. Because the W cycle gate does not come up until the fall of $\varnothing$A, the bit ring is still at bit S when $\varnothing$C arrives. This reads out of core character 00 and advances the units ring to character 01.

The data from cores, $\varnothing$A to $\varnothing$A, is sampled on 3.02.12 with $\varnothing$C at 3R8. At the same time core space bits are being inserted for each character at 3S8. Since the core bit ring is reset to Bs, the first bit in any file record following the AGC pulses will be a space bit (Refer to Figure 86).

To stop writing after core character 99 has been written it is necessary to drop the disk cycle gate on 3.01.05 at 2V3. This blocks the core starts. The stop disk cycle gate line has a negative pulse at this time developed on 3.01.07. Two "and" inverters feed this line, one for W cycle and one for R cycle. During W cycle 2X5b will have Bs pulses on pin seven. Pin eight will go up when the write gate control trigger goes 3 pin high at the fall of core field 9. At the same time a 180 μs delay is initiated at 2U1 on 3.01.07. The fall of this delay gate will turn off the disk write gate 180 μs after the last character is written.

The record must be written within one sector on the disk. If the disk write gate remains "up" into the next sector, the AGC pulses for the next record will be erased. To detect this condition, the record stop pulse (record start for following record) samples the disk write gate trigger at 2V10b on 3.01.07. A write gate stop failure will turn on the file check trigger on 1.02.06. The fall of the record stop pulse, 40 μs later, is inverted at 2T5b on 3.01.07. It is capacitively coupled to the inverter at 2F10b, where it plate pulls the disk write gate 10 pin low.

When writing on the file a check will be made to ascertain that the file is up to speed. If the file is below speed, writing may be completed long before the end of the sector (record stop). On 3.01.08 the fall of the disk write gate will trigger the single shot at 4Y2. The negative single shot gate should appear at pin 5 of the AI at 4Y1a when the record stop pulse is on pin 6. In this case no file speed check will be detected. Notice that the check will be made only if a write operation has just been performed. The trigger at 4X2 will be pulled 10 pin low each file revolution with the record start. Only the fall of the disk write gate can raise pin 10 and allow the check. The duration of the single shot is adjusted after the file has reached full speed as outlined in the RAMAC Reference Manual.

Second RW Cycle: The store check line, being high at the end of the first W cycle, demands another RW cycle. The second R cycle will be accomplished in the normal manner, re-reading the selected drum track into the core buffer.

During the W cycle the 100 characters in the core buffer are entered into the compare circuits (3.03.01) as W data and the file record is entered into the compare circuits as read data. (Refer to the data flow on Figure 88.) The two sets of data flow must be syn-

chronized with the file clock. The file clock in turn will be controlled by the data coming from the disk.

A W cycle record start will be developed in the same manner on 3.01.04. ON 3.01.05 the disk read single shot 2V2 will be turned on, since store check is high. At the end of 360 μs pin 3 will go low, turning the disk R cycle control trigger 3 pin high and the store check trigger 10 pin high. The disk R cycle control scans the disk data line at the AI at 2U3b looking for the first bit written (after the AGC pulses). The first bit, a space bit, arrives and triggers a 4 μs read delay at 2R1. At the fall of pin 10 the disk cycle gate will be brought up by turning the trigger at 2T3, 3 pin high. The disk cycle gate will again become the W cycle gate on 3.02.09. This will provide core phase pulses to drive cores, and also develop W data on 3.02.12 at 3Q2b.

The disk clock on 3.01.01 was started with the first Bs on the disk read out data line by setting the clock control trigger at 2B6 10 pin high. This trigger had been previously set 10 pin low at the fall of the 360 μs disk read delay, appearing on the clock set line. It was previously explained how the clock control trigger kept both oscillators from operating when 10 pin low. Each data bit from the disk on 3.01.01 will flip the clock switching trigger, 2E7. The write clamp, which previously kept it 10 pin high, is down since the write relay 5057 on 8.01.01 dropped out at W cycle end of the first W cycle.

The disk read out data pulses are arriving at disk $\varnothing$A time since they are switching the clock. These pulses are developed into 6 μs pulses at the disk data single shot on 3.01.01 at 2F9. This is the disk data line which brings up the disk cycle gate on 3.01.05. This data is also fed to pin 8 of the standard data trigger 2H7, the plus shift turning this trigger 3 pin high. The next $\varnothing$A will flip 2H7 trigger 3 pin low resulting in a $\varnothing$A to $\varnothing$A standard data pulse. In the case of 2 consecutive data pulses, both $\varnothing$A's will be blocked at 2K7b resulting in a 24 μs data gate out. The standard disk data has the space bits removed on 3.02.06 at 3P4 (since there are no Bs in cores) and becomes read data.

W data and read data are now compared on 3.03.01. Two AK's at 3G7a and 3F4b are fed by both data lines. If both sets of data are identical neither one conducts. Any discrepancy causes one of them to conduct resulting in a $\varnothing$C pulse on the compare failure line to the file check trigger. This trigger raises the error lines and stops the machine in the same manner as a parity error, described in section 4, except the file check light will be on.

The reading and comparing operation will be stopped on 3.01.05 by dropping the disk cycle gate with a negative pulse on the stop disk cycle gate line at the first Bs after the fall of core field 9 (after character 99).

The file writing and reading operations are shown on the sequence chart in Figure 86. Notice how the two oscillators are out of phase during bit one time. $\varnothing$A and $\varnothing$B are early in relation to the data pulse but $\varnothing$C, initiated by the fall of the clock, is back in time.

Read Record From File ($T_1 = R$)

With the instruction, R99X9900, the RAMAC cycles through I, R, and W cycles, during which it transfers the record from the established file address into the core buffer on R cycle and to track X on W cycle. As the transfer from the core buffer to track X is a typical W cycle operation as covered in Section 4, we need to give attention only to the R cycle operation .

The earlier discussion of the second W cycle operation with $T_2 = R$ has developed all of the concepts necessary to understand how data may be read from the file. In the second W cycle operation with $T_2 = R$, the standardized disk data was passed through 3.02.06 to become read data which was entered into the compare circuits on 3.03.01. With $T_1 = R$ the read data is gated into the core buffer circuits by the R cycle gate (3.02.06). Refer to Figure 89.

The R cycle gate is provided by gating the disk cycle gate against R cycle at 3V3a (3.02.04). The disk cycle gate is developed in the same manner as was used to develop it for the second W cycle with $T_2 = R$, except that the single shot, 2V2, is triggered with the R cycle record start applied through 2W2a (3.01.05).

It will be recalled that on R cycles the core buffer waveform generator is not activated at any character time until BR$\varnothing$C, after all bits for that character have been entered into the character register. Because of this, the core units and tens rings do not advance until the end of each character time. When the rings advance from 99 to 00, the last character has been transferred and the disk cycle gate can be turned off immediately. The fall of core F9 is inverted into a positive shift at 2Y4a (3.01.07). This is gated by R cycle to cause a negative shift on the stop disk cycle gate which flips the trigger 2T3 (3.01.05) to lower the disk cycle gate.

Record Advance

There are certain types of ledger accounts which normally require the capacity of two records to store the required data. A RAMAC user may, for example, reserve two records for each of his customer accounts.

One of these records would normally contain such

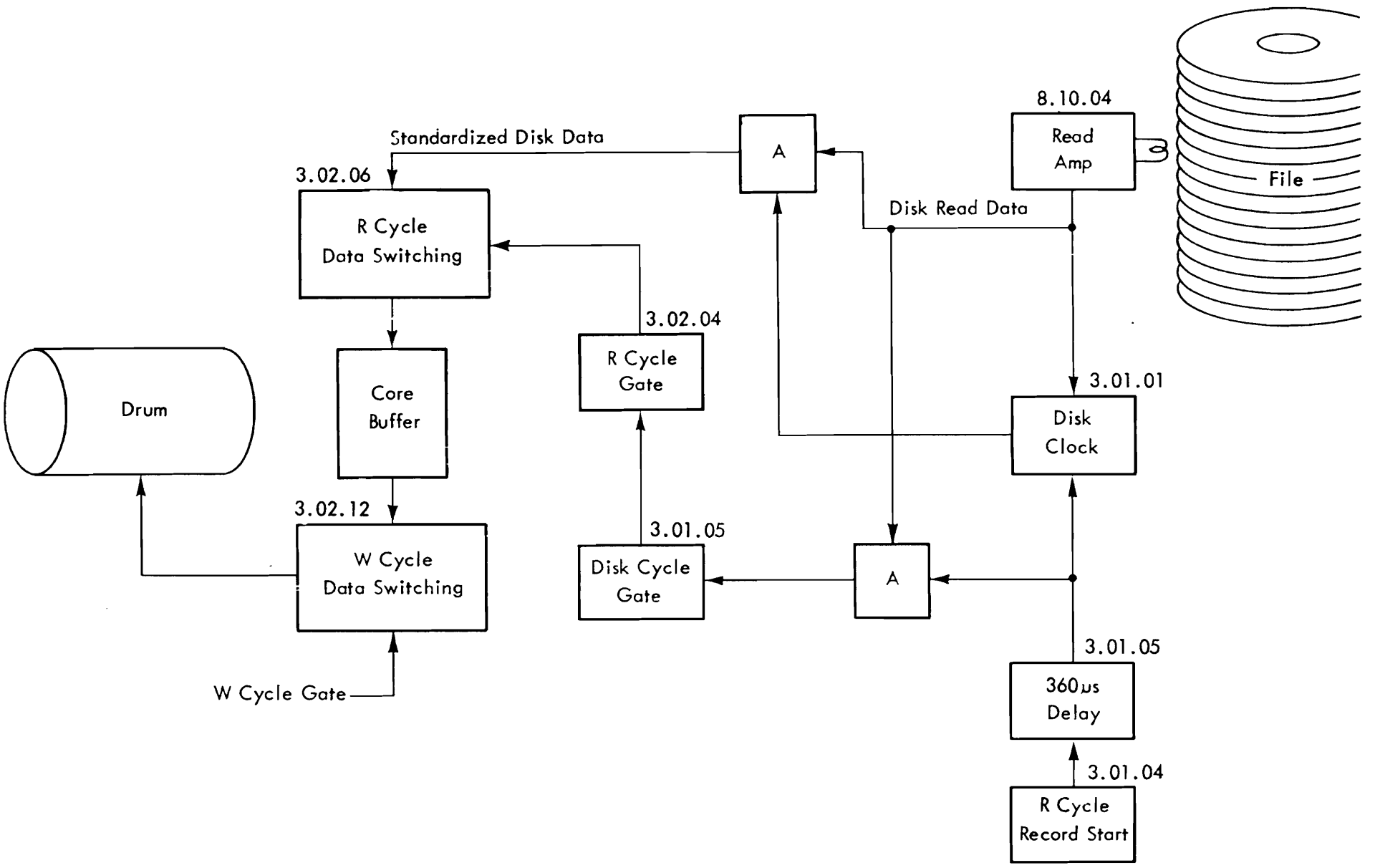


Figure 89. Data Flow and Controls, $T_1 = R$

information as name, address, and shipping instructions, whereas the second would contain the accounting data related to that customer. The two records required by ledger accounts of this type are normally stored in two consecutive file addresses. The record advance feature permits both of these records to be made availabe without requiring a second servo instruction.

For example, the ledger account of a particular customer is stored in file addresses 25242 and 25243. Record 25242 contains customer name, address and shipping instructions. Record 25243 contains the accounting data. When it is necessary to process a customer order, the following instructions transfer the customer's records to the processing track:

1. K05J9906 causes a servo to file address 25242.
2. R99W9900 &
   a. Transfers record containing customer name, address, and shipping instruction to track W.
   b. PROGRAM EXIT & is wired into RECORD ADVANCE IN. This causes the file address to advance from 25242 to 25243. RECORD ADVANCE OUT is wired to PROGRAM ADVANCE.
3. R99X9900 transfers record containing accounting data to track X.

Immediately prior to record advance the access mechanism is established at file address 25242. The address register relays are holding on the J hold B line. The record relay which holds is R5160, for record 2 (8.03.01). The disk tens relays and the record relays of the process unit address buffer are holding to J hold B. These relays are:

1.	R354	disk tens = 2	3.05.07
2.	R306	record = 2	3.05.03

OBJECTIVES:

1. Drop record 2 relays in address buffer and address register.
2. Pick record 3 relays in both groups.
3. Provide record advance out impulse during second P cycle. Drop old record relays.

Drop Old Record Relays: The program exit & hub emits an MR7 impulse during the first P cycle. This is wired to the record advance in hub on 3.05.02, picking R290 and R295 through the R306-2 N/O points. This will cause the 305 to go through an IRWDPDDP sequence. These relays hold through MR9 until character 48 of the second D cycle (2.09.02). The R290-4 points will open the hold to the record relays in the address buffer and address register by picking R311 on

3.05.01. The address buffer relays are on 3.05.03 and the address register relays are on 8.03.01. This occurs at F7 of the first D cycle following P cycle.

Pick New Record Relays: After dropping the record relays it is necessary to pick new relays, increasing by one the previous address. R295 has stored the information that the previous record address was 2. On 3.05.03 the address buffer relays 305 and 306 are picked through the 100 Ω resistor and the normally open points of R290 and R295 to ground. The other side of these relays goes to + 70 volts on the J pick line, through MR4 during the double D cycle. On 8.03.01, R5157 and R5160 (the record 1 and 2 relays) will pick through the normally open points of 305 and 306 on 3.05.12. The common side of the address register relays goes to + 48v on the pick common line. Normally this circuit is through MR6, which picks on servo operations. For record advance, however, we will place MR7 on the MR6 line. On 2.09.11 the circuit will be through the R289-3 N/O points to MR7 to +48 volts. R289 will pick on 3.05.02 through the 290-2 N/O points.

P, D, D, P cycle sequence will be required to complete the record advance routine. To continue the program a control panel impulse to the program advance hubs or the program entry hubs is required. This impulse will be available during the second P cycle from the record advance out hubs on 3.05.02. When the record address is advanced from 9 to 0 it may be desirable to change the track address. In this case the record advance overflow hub (3.05.02) emits instead of the record advance out hub.

Skip to Record

This feature operates very similar to record advance. A P flag wired to one of the 10 skip to record hubs (3.05.02) will change the record address, the track and disk addresses remaining unchanged. Any one of the 10 possible record addresses may be selected. A skip to record out hub provides an impulse to continue programming on the second P cycle.

For example, a P flag wired to SKIP TO RECORD 8 on 3.05.02 will pick relays 278 and 284. The 278-2 N/O points will pick R277 during the double D cycle. On 3.05.10, R311 will be energized through the 278-4 N/O points to drop both address buffer relays (3.05.03) and address register relays (8.03.01). Relay 309 on

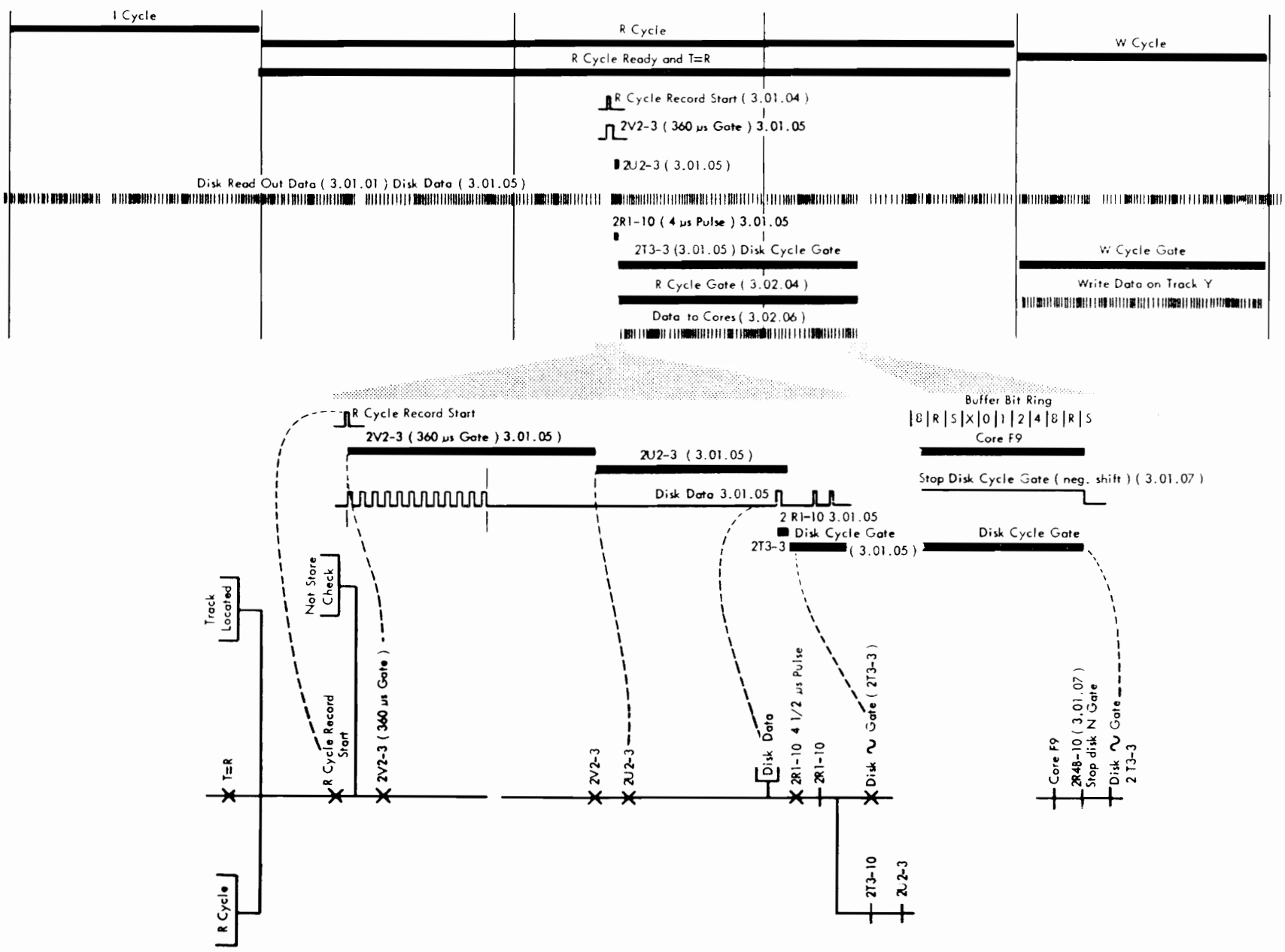


Figure 90. Read Record From File (R99Y9900bb)

3.05.03 will be picked through the 284-2 points to ground, when J pick (MR4) is made. On 3.05.12 record 8 pick line will be grounded through 309-3 N/O points. This will pick the record 8 relay R5164 on 8.03.01 because the pick common line is returned to + 48 volts by placing MR7 on the MR6 line. The skip to record out hub provides a control panel impulse on 3.05.02 through the 277-2 N/O points.

350 Optional Features

In this section the various combinations of files, process units and accesses will be discussed. This covers dual access, dual file, dual process and also the 10 million character file. Figure 93 illustrates the location of the various access arms available, the location of the shoe connectors, fuse boxes and relay gates. The M and S refer to MASTER and SLAVE 305's, the slave processing unit being the second 305 on a dual process system.

Access 0 is used on the standard single access machine and is connected to the 305 through shoe connector E (M). For dual access, 0 and 2 are used through SCE (M). For dual process, accesses 0 and 3 are used through SCE (M) *and* SCE (S) respectively. If dual access is included with dual process, all four accesses are used, 0 and 2 for the master 305 and 3 and 5 for the slave. A dual file system with single access uses access 0 for both files. The second file is connected to the 305 from its SCE (M) to the first file's SCH (M). Nearly all the SCH terminals are jumpered to the corresponding positions on the first file's SCE (M). This

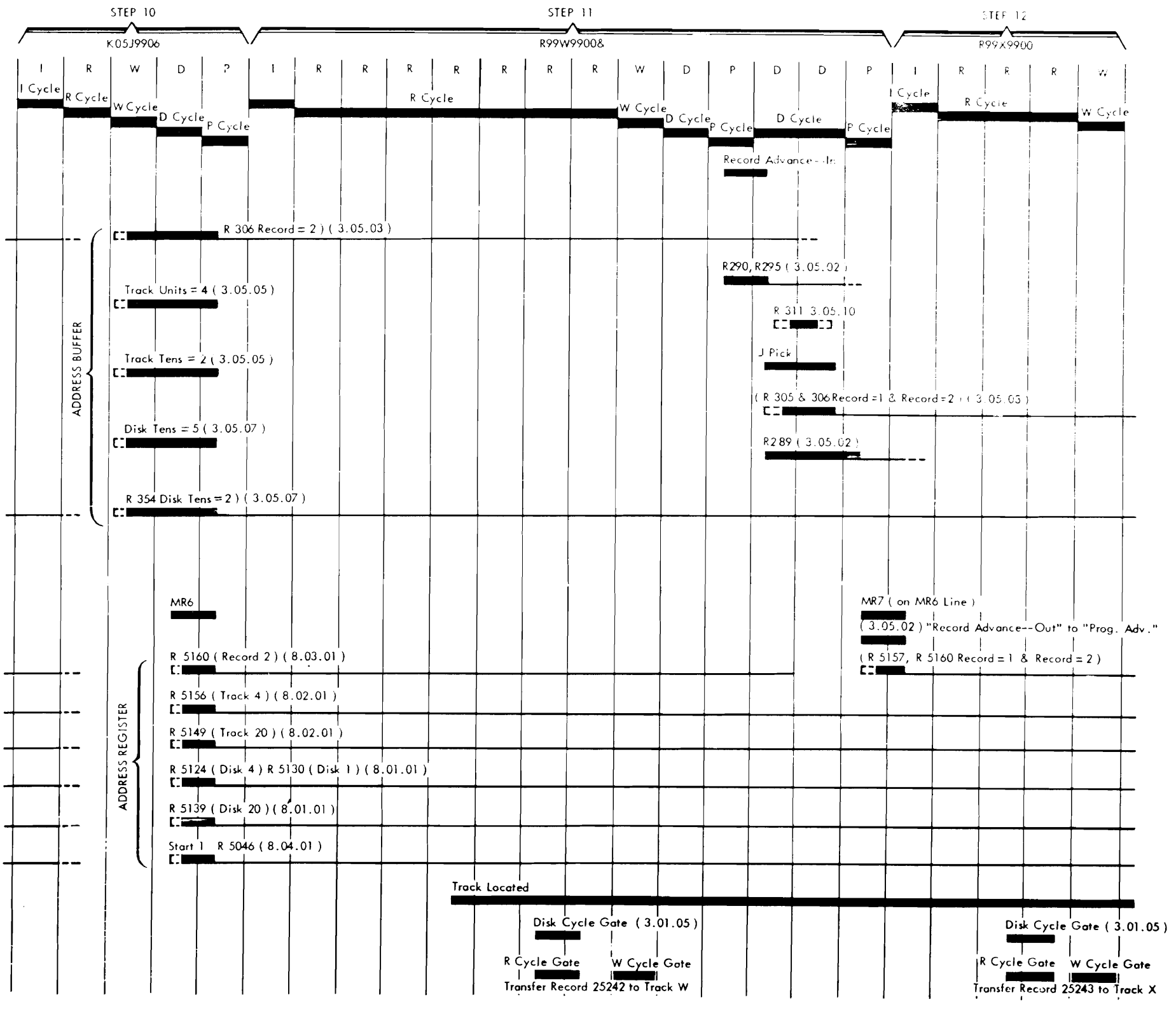


Figure 91. Record Advance

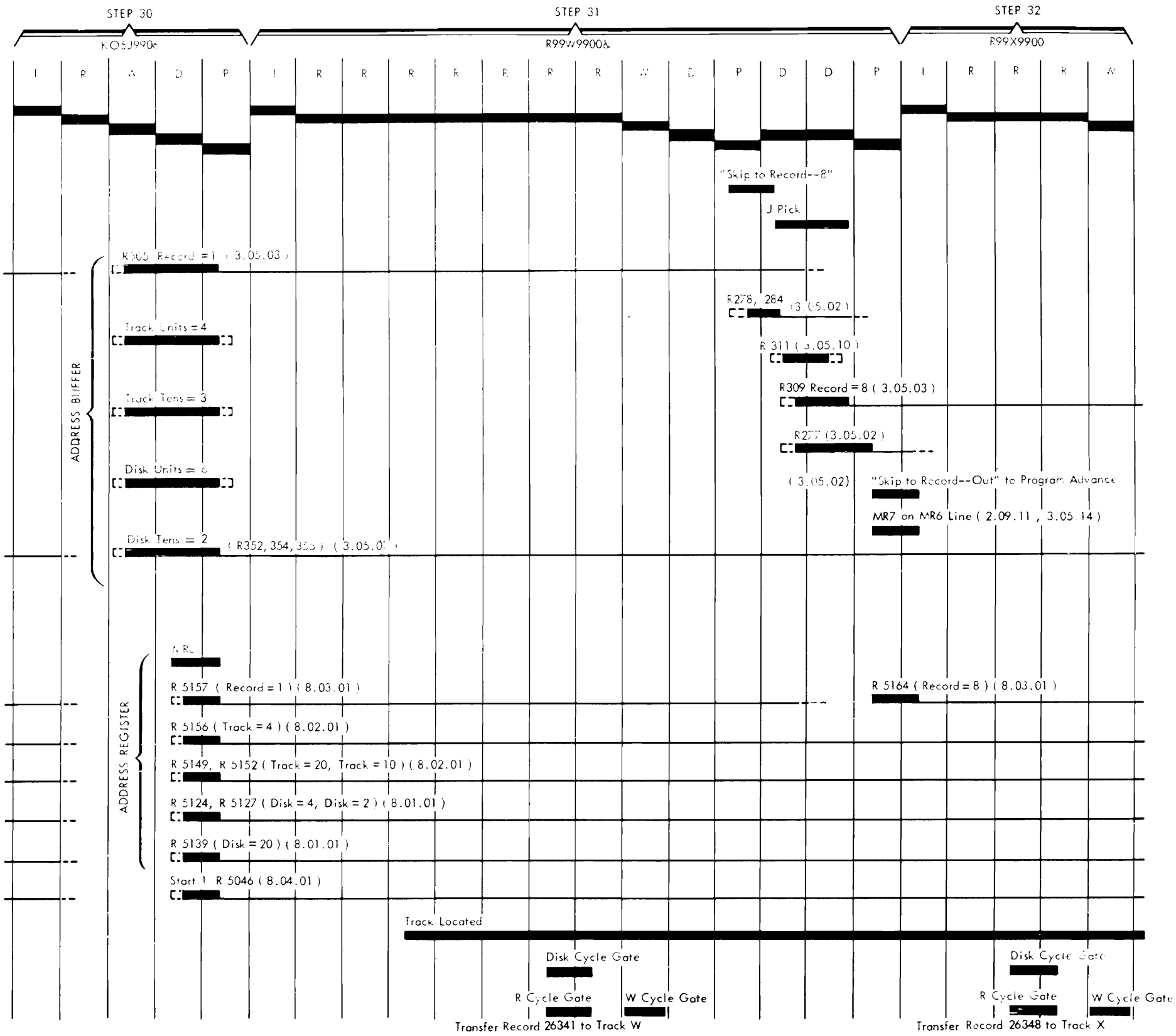


Figure 92. Skip To Record

can be seen on 8.00.07. The SCE (M) on the first file goes to the 305. Dual access can also be included on a dual file system using access 2 through the same cable arrangement.

A dual file system as well as the 10 million character file will augment the standard file addresses. For a dual file the second file will use addresses 5000 to 99999. With a 10 million character file the addresses will run from 00000 to 99999 for one file. If a 10 million and a 5 million character file are used on a dual file system the 10 million character file uses addresses 00000 to 99999 and the 5 million character file will use 100000 to 149999. Two 10 million character files use 00000 to 99999 and 100000 to 199999.

It is important to note that all operational information and control panel hubs refer to access 0 and access 1 on a dual access system. In the system diagrams access 0 and 3 correspond to the control panel access 0 while access 2 and 5 correspond to the control panel access 1.

Dual Access

To reduce the time required for servo operations and to allow processing to begin sooner, two access arms may be installed on a single file. Mechanically, the second access operates like the first and is located in position 2 (Figure 93). All circuits in the file are duplicated for the second access. These are mounted in a second relay gate below the first with identical numbering for the relays and pluggable units. The input, output and control lines to the 305 from access

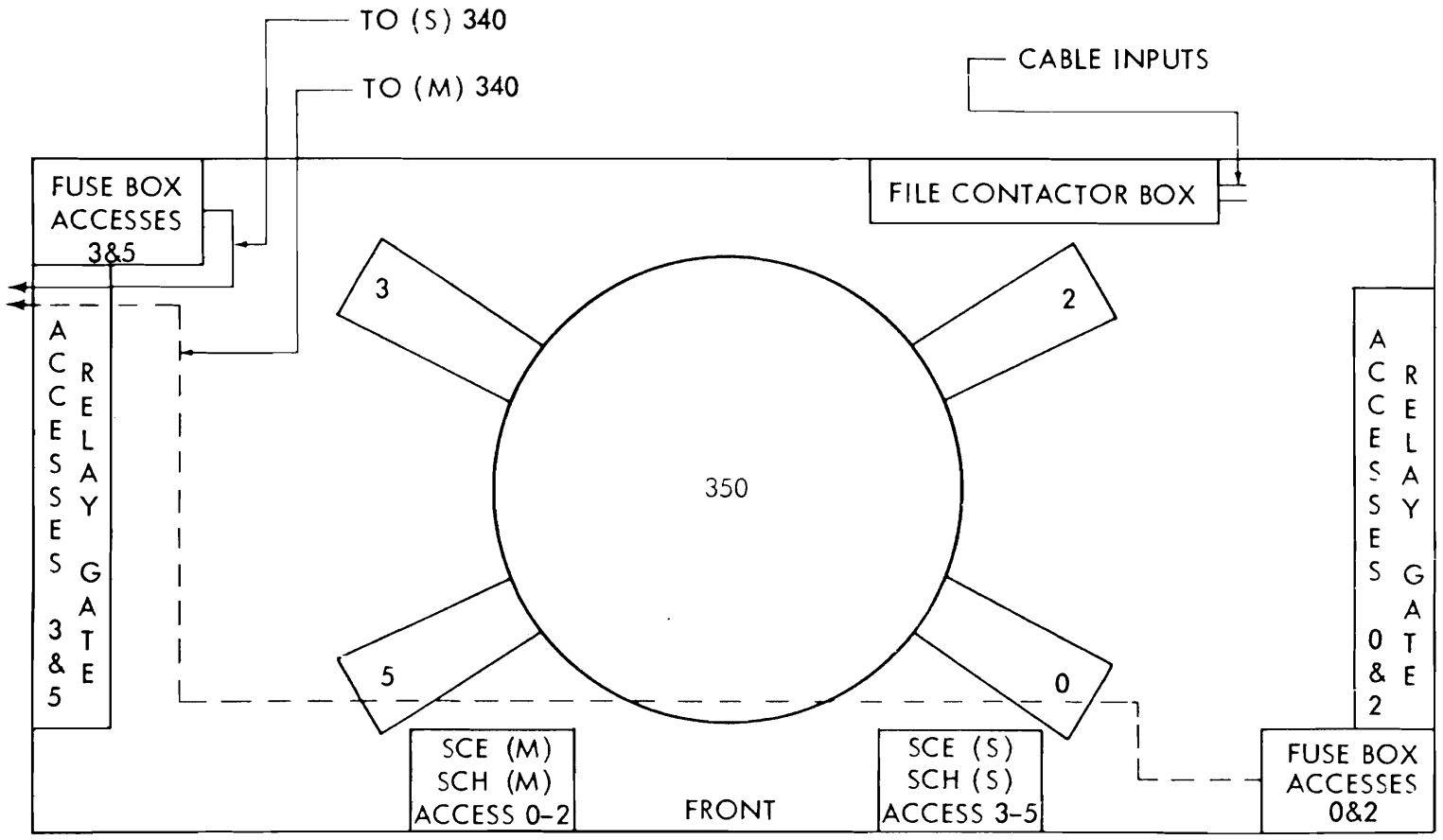


Figure 93. Models 3 and 4 Relay Gate File

2 circuits pass through SCE along with lines from access 0. To trace these lines physically the System Diagrams contain small charts showing the plug connections in shoe connector E for access 0/3 and access 2/5.

Functional Operation

There are two modes of operation for a dual access file:

1. Automatic sequencing.
2. Select Mode.
   A. Using one access only.
   B. Using either access, selected through the control panel.

Automatic sequencing occurs without any special control panel wiring. Following a machine reset, a $T_2 = J$ instruction will cause access 0 to servo. This same instruction switches all file input and output circuits to access 2. Any later instructions or commands to the file will be directed to access 2. This includes another $T_2 = J$, a $T = R$, or an inquiry. A second $T_2 = J$ will activate access 2 and at the same time alert access 0 to any file commands following. This means all programs using automatic sequencing will begin with two $T_2 = J$ instructions conditioning access 0 for the first file read or write operation.

The switch of the control circuits, when in automatic sequencing, may be prevented by including a Q of 4 in the $T_2 = J$ instruction. The following file commands will refer to the access which received this servo instruction. Another $T_2 = J$ without a $Q = 4$ will resume the sequencing.

In the select mode of operation the operator must choose the active access with control panel wiring. Five hubs, shown in Figure 94, have been added to the 305 control panel. A wire from the dual access common hub to SEL places the machine in the select mode. Program exits may be wired to either the dual access 1 or 0 hubs, through selectors if desired, to alert access 2 or 0. The selected access remains so until a new selection takes place. To use only one access for the entire program, a wire from the common hub to the 1 or 0 hub can be used.

Dual Access Logic

In Figure 95 the control of the two access arms as well as the data flow is illustrated. The condition of three relays, R426, R429, and R432 determines which access will be active. Let's assume these relays are all picked, conditioning access 2. During W cycle of a $T_2 = J$ operation the file address (data to J) picks the access 2 buffer relays, disk tens and record, through the N/O points of R432. The other buffer relays are common to both accesses. Pick common is directed to access 2 address relays through R426-1 N/O. This line also initiates the pick of the start relays for access 2.

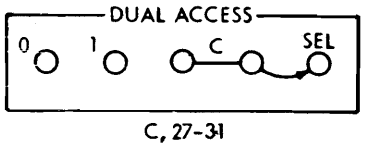


Figure 94. Dual Access Hubs

The result is a servo of access 2. The address relays and start relays will hold through N/C MR5.

This same operation will drop out (Figure 95) the 3 selection relays at the end of P cycle. R426-5 N/C conditions the 0 access write amplifier, while R426-6 N/C conditions the 0 read amplifier. Another $T_2 = J$ instruction will pick the access 0 address and start relays through the R432 N/C and R426-1 N/C points. Notice that during this $T_2 = J$ operation MR5 will open to drop the old access 0 address and start relays. The access 2 address and start relays will hold through R429-8 N/C points at this time.

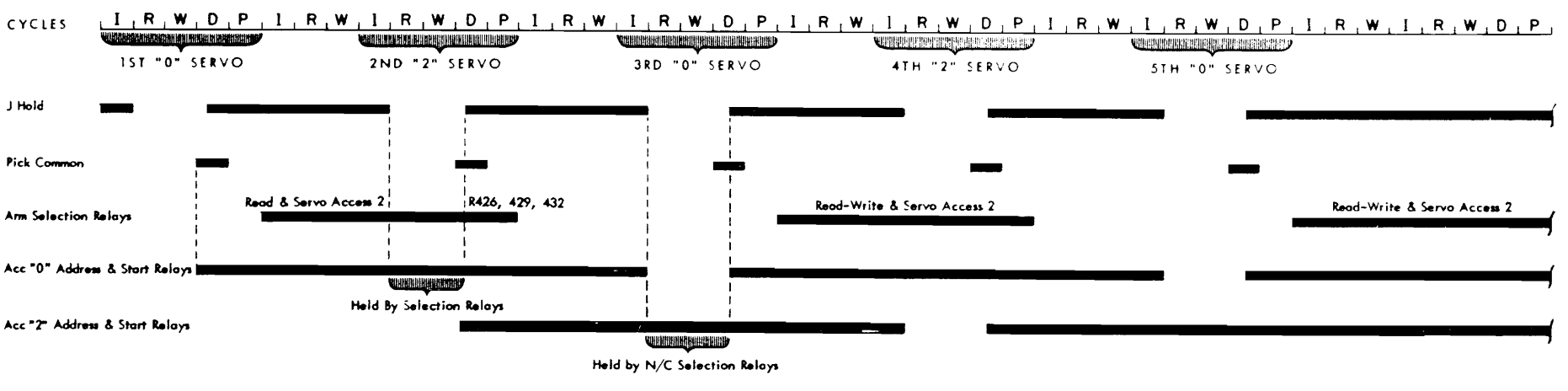
Circuit Description

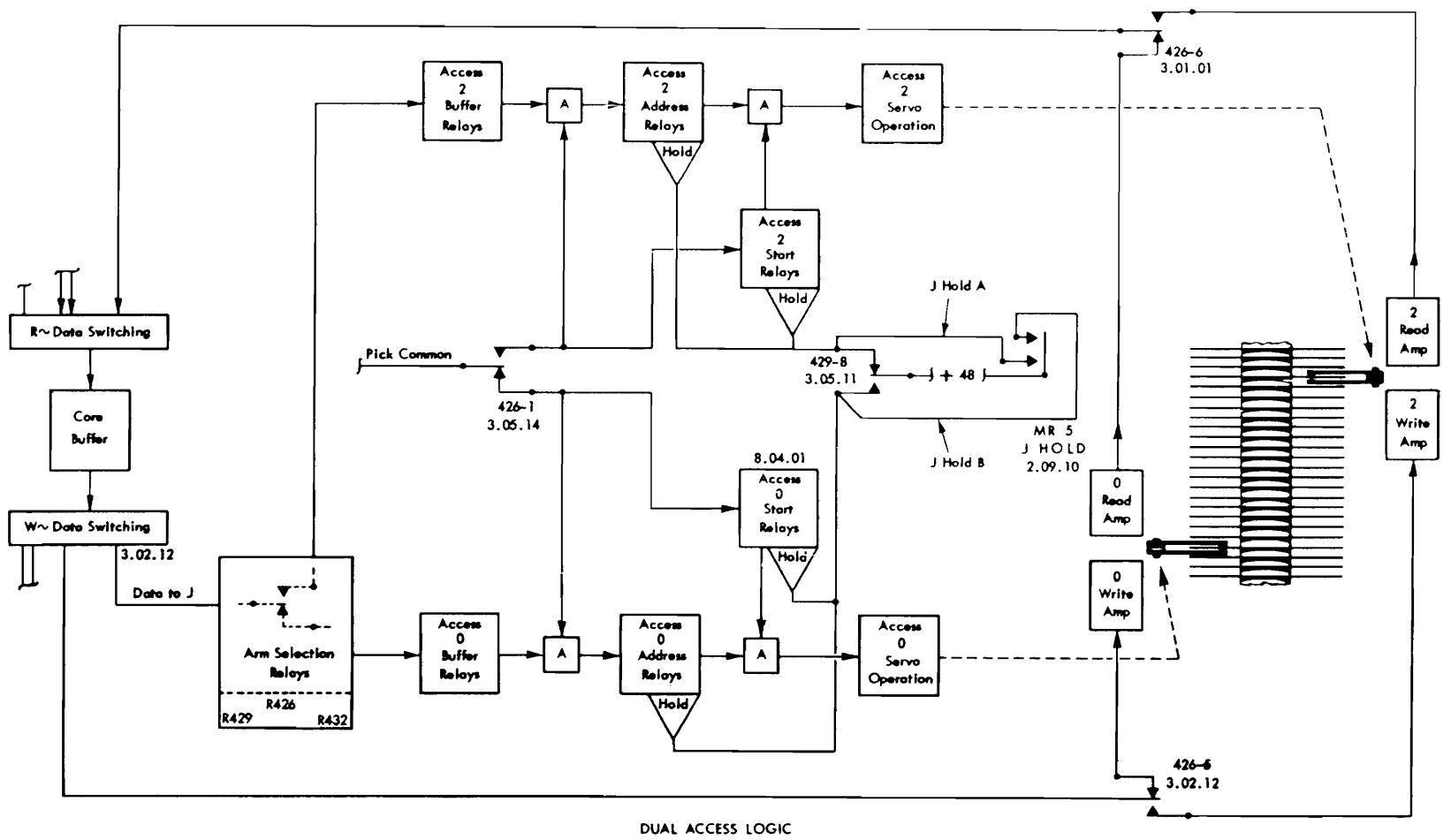
Access Selection: An "X" reset will set the alternate access trigger (3Y8-3.05.09) 10 pin low. This allows the manual reset line to fire the three blowout thyratrons and drop the three access selection relays. This trigger will be flipped from one state to the other every W cycle during $T_2 = J$ and $Q = \overline{1}$. Its output alternately conditions the relay pick thyratrons, then the blow out thyratrons which will be fired at P cycle end.

In the select mode a control panel wire from DUAL ACCESS C to SEL blocks the binary input to the alternate access trigger. It can be flipped only by an impulse to the 0 hub or the 1 hub.

Servo: The servo operation on dual access is performed in the same manner as on a single access file. When tracing circuits the condition of the three select relays must be known.

A modification in dual access interlocking does exist on 1.02.10. Normally a servo operation cannot begin if the access arm is still engaged in a previous servo, i.e., track located is low. An exception to this is following an "S" or "X" reset. Any time DC is turned OFF the file address relays will drop. This means the first servo must be made with track located down. On a dual access system the first two servos will be made





DUAL ACCESS LOGIC

Figure 95. Dual Access Logic

with track not located. On the first servo the R cycle control trigger (1R11-1.02.10) will be 3 pin high allowing a start R cycle. P cycle of $T_2 = J$ will pull 1R11 3 pin low, but the next $T_2 = J$ instruction for access 2 will turn trigger 1K9 3 pin low. This returns the R cycle control trigger 3 pin high, allowing another start R cycle without a track located gate. Both triggers will remain 3 pin low for the remainder of the operation requiring a track located signal for an R cycle start during $T_2 = J$.

Dual File

Functional Operation

There is no change in the operation or programming of a RAMAC when a second 350 Disk Storage Unit is added to the system. The 305 Process Unit automatically decides which 350 will servo, this action depending upon the tens value of the disk address. When performing an instruction in which T = R, the system will read or write at the last servo address. The file which contains this address will be referred to as the active file in this discussion. The 5 million character file added to a basic system is referred to as file 2. It will contain records whose addresses range from 50000 to 99999. A 10 million character file in a dual file system becomes file 1 with addresses from 00000 to 99999. The 5 million character file contains addresses 100000 to 149999. This requires an additional character position in the disk address circuits (3.05.07) which is analyzed for a 1 bit to select file 2 as the active file.

A separate set of system diagrams will show the circuits for file 2. Input and output signal lines go from SCE on file 2 to SCH on file 1. From there many terminals on SCE and SCH of file 1 are common. AC power to both files comes from the remote compressor. The "power on" sequence is controlled by a timer in the remote compressor cabinet and is covered in the "340 Power Supply" section of this manual.

Circuit Operation

The block diagram of Figure 96 shows the modification to the circuits when two files are used. During any $T_2 = J$ command, the J hold B line opens and drops any address relays and start relays in either file. The file address is entered into the common address buffer relays. To select the active file, the high order position of the file address is analyzed and the pick common line is directed to file 1 or 2. The pick common also picks the start relays for the active file. The start relays will hold until the next servo, alerting the active file's read/write circuitry for a T = R operation. Notice that the inactive file's start and address relays will be down. The only neons indicating on an inactive file are logic safety, bias safety, head relay and disk solenoid.

On 3.05.14 there are 4 pick common lines available for a dual file system with single accesses. Two of these will be used, determined by the file configurations (5 or 10 million character files). The address buffer relays in the 305 will direct the MR6 pick common line to one or the other. On an inquiry operation the first digit of the address keyed at the console will select one of the four common lines coming from 6.05.02.

Dual Process

Functional Operation

Dual system control allows two RAMAC systems to share the same disk storage unit or units. To enable each system to operate independently, an access mechanism is provided for each in the shared file (s). Each system may use dual access in the shared file. The master system uses accesses 0 and 2 while the slave system uses accesses 3 and 5. Figure 93 shows the arrangement of accesses within a shared file. Each access has its own relay gate, with 0 and 3 being the top gate in the left and right end of the file, respectively. Two additional shoe connectors, E and H, are added for accesses 3 and 5. The symbol (s) signifies slave components and the symbol (M) master.

The only reason to prevent the two systems from operating completely independently would be an attempt of both systems to process the same record simultaneously. No restriction is placed on both files servoing to the same address; however, dual process interlock circuits prevent a track located signal to the second file to servo to a common address. The first file to reach an address has precedence. Whenever a file servos it compares the contents of its address relays to the contents of the other file's address relays. With dual access, two comparisons must be made. If both comparisons are unequal, a track located signal is allowed. These same checks are made following a record advance or a skip-to-record operation.

Dual process interlock can be suppressed by control panel wiring on either or both of the 305's. However, when a system picks interlock suppression it cannot write on the file. When dual process interlock suppression is active a neon glows on the originating system's console, just above the file check light (8.25.01).

With dual accesses on a shared file a double interlock condition can arise preventing either file from receiving a track located signal. For example:

Access 0 to address A
Access 3 to address B
Access 2 to address B with a Q of 4
Access 5 to address A with a Q of 4

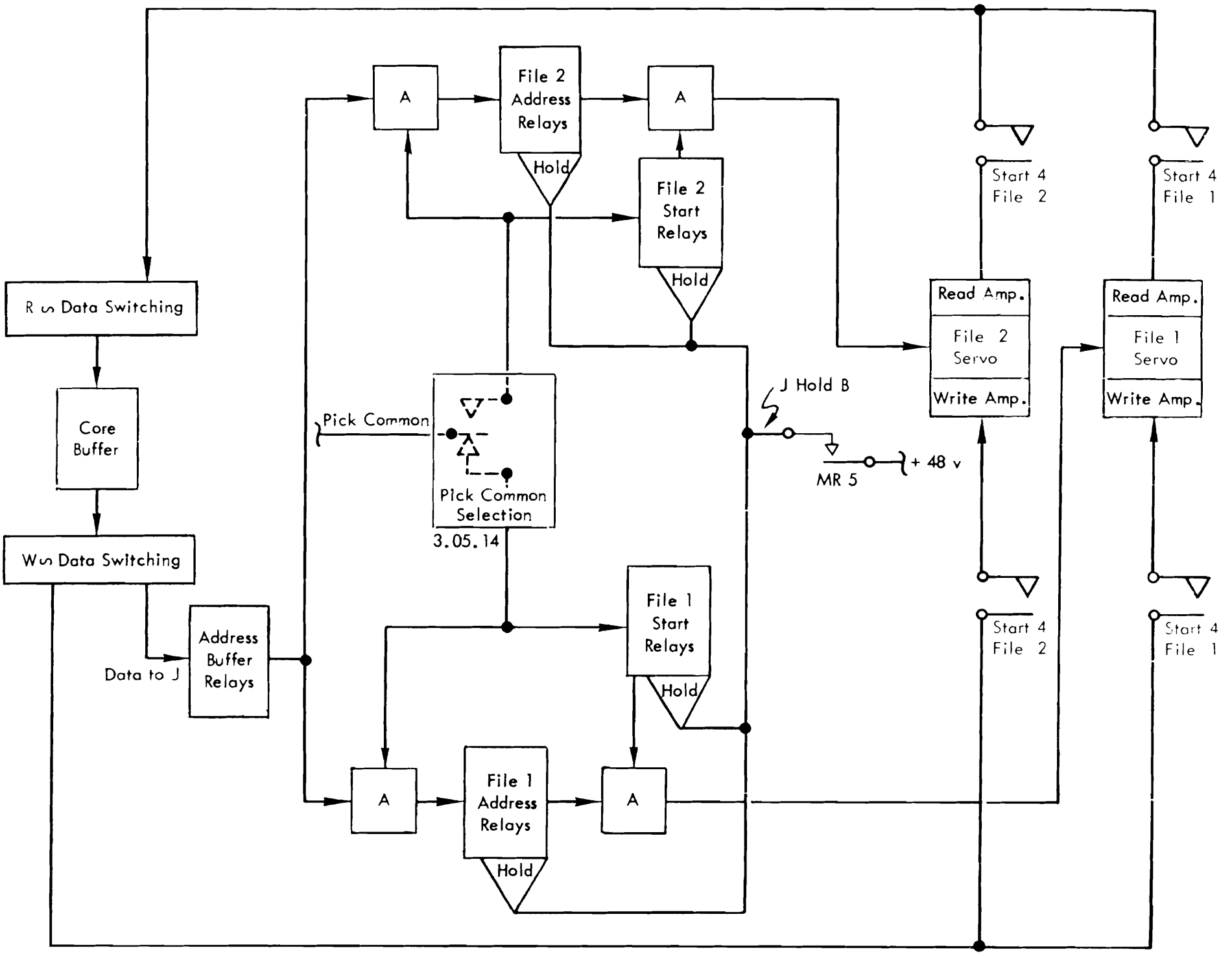


Figure 96. Dual File Logic

Dual process double interlock release circuits will allow the master system to receive a track located signal in this case.

Either system can operate with the other off. Depressing the power on switch on either console will cause the timer motor in the master compressor cabinet to sequence the file (s) power on (8.40.03). A slave compressor cabinet will be used only if the capacity of the two compressors in the master cabinet are insufficient. The slave cabinet will have only additional compressors in it. The control of file power is still in the master cabinet. When using a slave cabinet, the air supplies are in parallel. With dual access, dual file, dual process systems, connect master cabinet file 2 hose vent valve to the slave cabinet file 1 hose vent valve. The master cabinet file 1 hose vent valve supplies file 1 and the slave cabinet file 2 hose vent valve supplies file 2.

Circuit Operation

The dual process interlock circuits for access 0 checking the addresses at which arms 3 and 5 (on a dual access file) are located, are on diagrams 8.25.01 and 8.25.05. Each of the other three accesses will have similar circuits. A number 3 or 5 in parenthesis following a relay point indicates a relay in one of the other gates. All other relays and points are in access 0 gate. The objective is to develop a track located signal on 8.10.01 as soon as the access 0 servo is completed if access 3 and 5 are not at the same address. Plus 48 volts will be placed on the track located line through R5034-2 N/O and R5067-2 N/O on 8.25.01. These relays are picked by the J hold B line when an unequal condition exists in the compare circuits on 8.25.05. They will hold through their own 1 points until J hold B is broken by another servo instruction.

An impulse to the dual process interlock suppress pick (DPISP) hub on the master 305 control panel (3.05.11) will latch pick relays R5093 and R5094 bypassing the compare points in the track located signal line. File writing cannot occur from the system which has suspended interlocking because R5057 cannot pick (8.10.01). The interlock suppress will exist until the drop out hub on the master 305 is impulsed, latch tripping R5093 and R5094.

On a record advance or skip-to-record operation the J hold B line itself does not drop, however, it is modified before reaching 8.25.01 and 8.25.05. On 3.05.11 R289 or R277 points will open dropping the compare relays and allow a retest of the comparing circuits. The dual process double interlock release circuit is on diagram 8.25.09. All four arrival relays (R5071) must be picked. If there is no track located signal in either the slave or master 305 at this time, a double interlock exists. A high from 2Z1b in the master system will force a record start for the master system on 3.01.04.

In the event both systems servo to the same address simultaneously, preventing an access 3 clear signal (3.25.05) and an access 0 clear signal (8.25.06), the master system clear relay, R5034 on 8.25.01, will pick through R5034-3 (3) N/C points on 8.25.01 with J hold B. The slave system clear relay, R5034 on 8.25.02, will be unable to pick.

10 Million Character File

The track density has been doubled on this file increasing the addressable locations to 99999. Fifty single thickness disks are used which means 4 disk addresses per disk. This can be seen in Figure 6. All even disk addresses servo to the outer 100 tracks while odd disk addresses move the arm to the inner 100 tracks. There is an outer and one inner CE track, separated by 200 processing tracks.

The track detent assembly is shown in Figure 97. There are four detents numbered 1, 2, 3, 0 from outside to inside. Detent 0 operates for track addresses 00, 04, 08, 12, etc., detent 1 for addresses 01, 05, 09, 13,

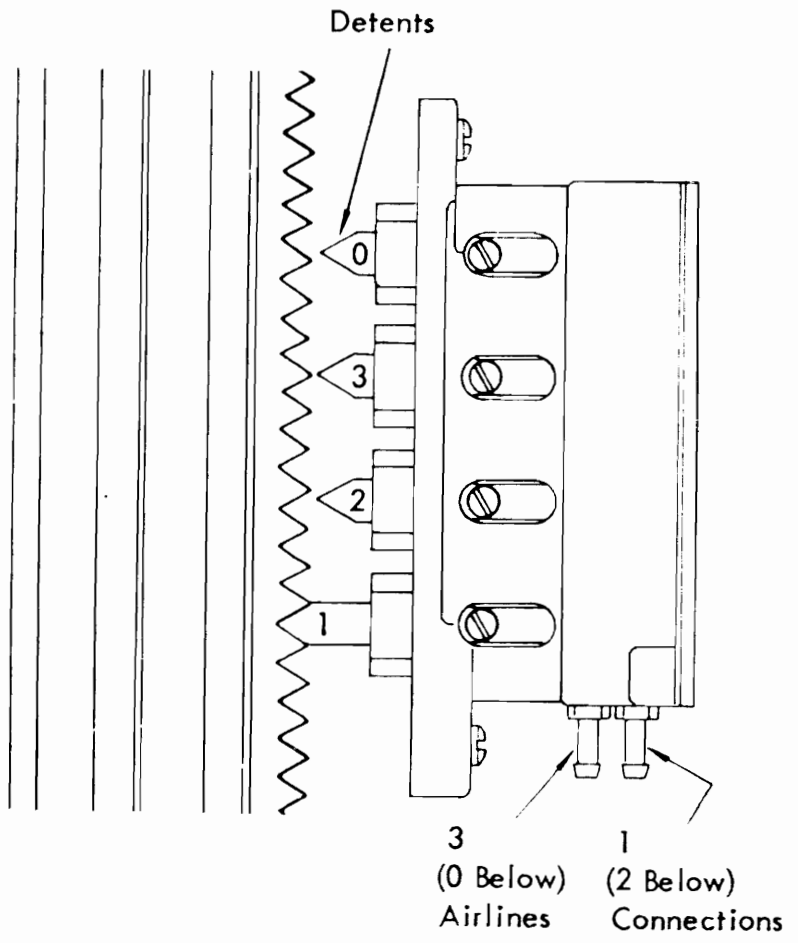


Figure 97. Track Detent, 10 Million Character File

etc., detent 2 for 02, 06, 10, etc., and detent 3 for 03, 07, 11, etc.

The address register for a single 10 million character file is not changed. However, the bit 1 relay of the units position of the disk address is now used in the track address relay tree to determine whether the track address is for an odd or even disk. For the disk markite all we need is the disk 10's relays and the 2, 4, and 8 bit relays of the disk units position. This can be seen on diagrams 8.01.02 and 8.02.02 for a 10 million character file.

The 5 and 10 million character gate files are identical in most areas. Any area that is different is easily identified. Each System Diagram covering a changed circuit has the title "10 million character file."

The single thickness disks used on this file require a different access arm, head spreader, read/write head, and head air pistons.